Design Challenges in High Performance Three-Dimensional Circuits

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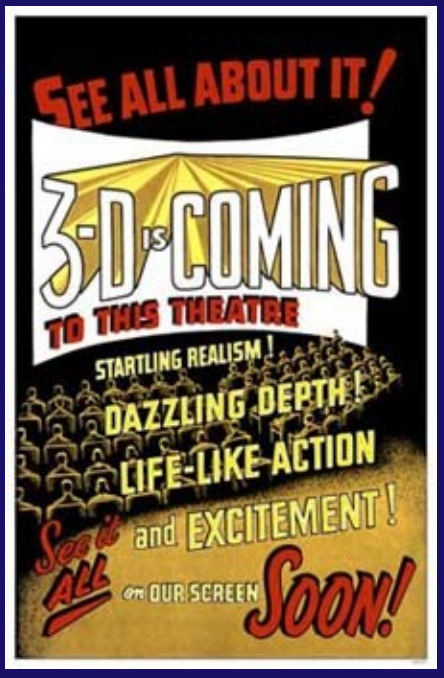
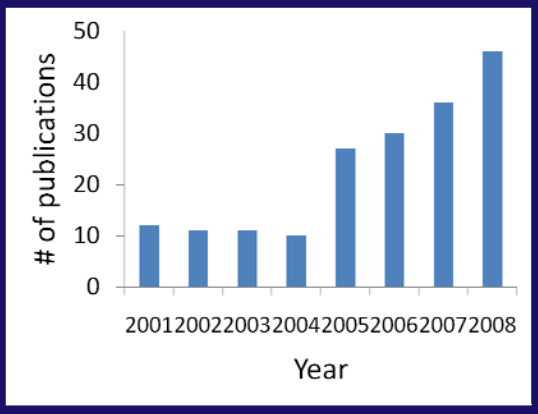
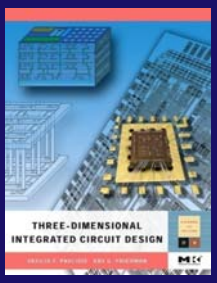
D43D: System **Design for 3D** Silicon Integration Workshop

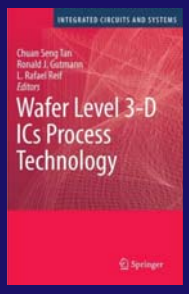


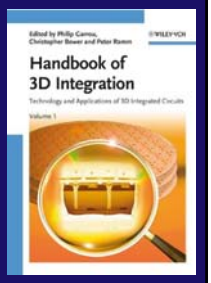
An Increasing Interest in 3-D ICs



- *Source: IEEEXplore*



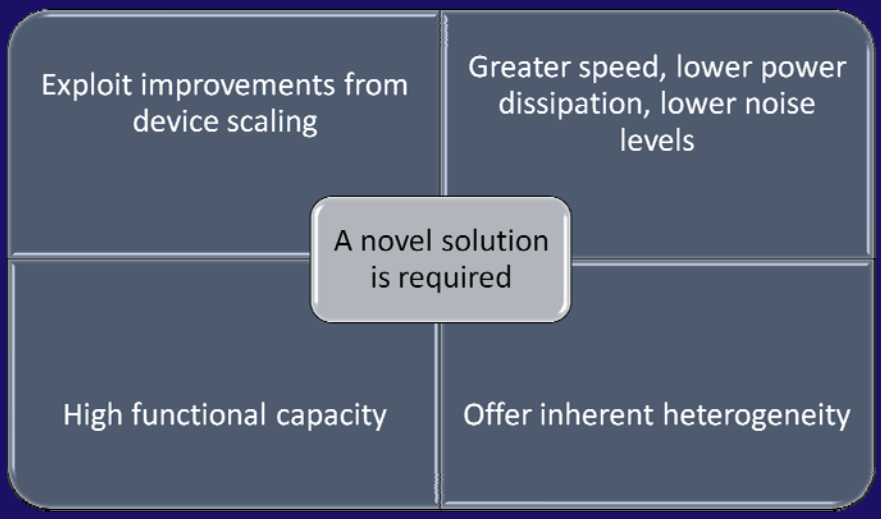




Presentation Outline

- Three-dimensional (3-D) integration
- MIT Lincoln Laboratories 3-D Technology
- Physical design issues in 3-D integration
- 3-D networks-on-chip
- The Rochester cube
- Near and long-term research problems
- Conclusions

Break Through the Interconnect Wall



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  - Forms of 3-D integration
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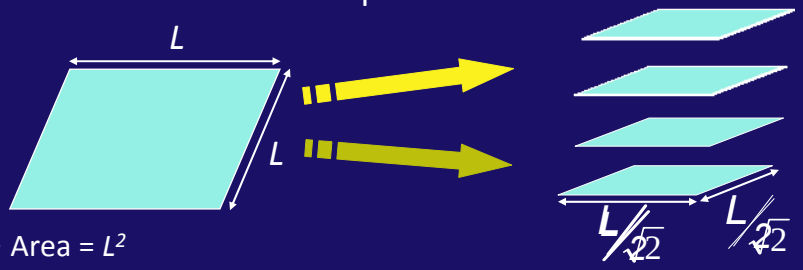
3-D Integration

Maximum wirelength reduction
2 planes ~30%
4 planes ~50%

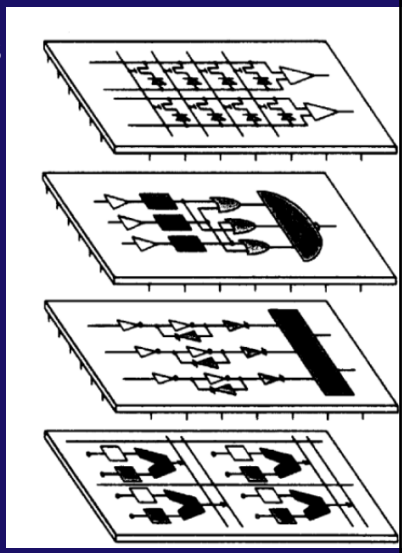


- Area = L^2
- *Corner to corner distance = 2L*

- Area = L^2
- *Corner to corner distance* $\approx \sqrt{2}L$

Advantages of 3-D Integration

- Integration of disparate technologies
  - No yield compromise
  - Greater functionality
- Number and length of global interconnects are reduced
  - Reduction in interconnect power
- Dedicated NoC plane for IP block level communication



M. Koyanagi, *et al.*, "Future System-on-Silicon LSI Chips," *IEEE Micro*, Vol. 18, No. 4, pp. 17-22, July/August1998.

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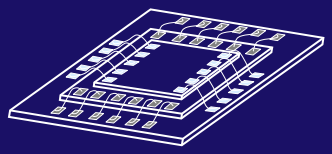
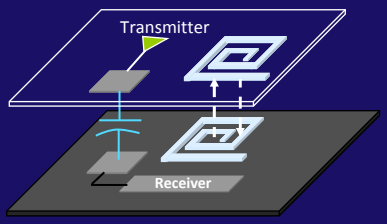
Forms of 3-D Integration

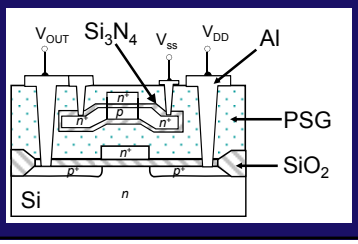
- Wire bonded die



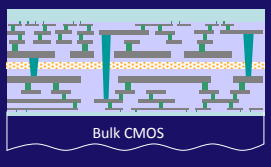
- Contactless 3-D circuits



- Stacked 3-D circuits

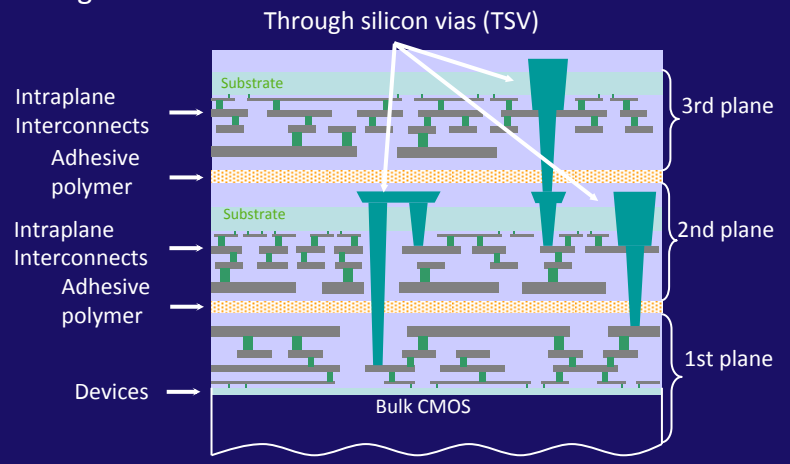


- 3-D ICs – Fine grain interconnects



Cross-Section of a 3-D Integrated Circuit

- Different plane bonding styles
- Bonding materials
- Bonding process involves
  - Wafer thinning



*R. J. Gutmann *et al.*, "Three-Dimensional (3D) ICs: A Technology Platform for Integrated Systems and Opportunities for New Polymeric Adhesives," *Proceedings of the Conference on Polymers and Adhesives in Microelectronics and Photonics*, pp. 173-180, October 2001

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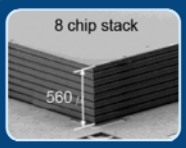
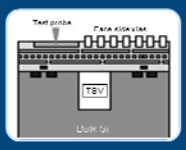
Spectrum of Challenges in 3-D ICs



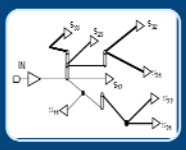
Manufacturing

- Plane alignment and bonding
- Through silicon vias



Testing

- Pre-bond testing
- Post-bond testing



Design

- Interconnect design techniques
- Thermal management techniques
- Physical design techniques

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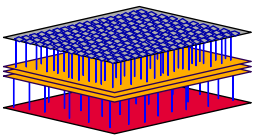
3D Integration for Integrated Circuits and Advanced Focal Planes

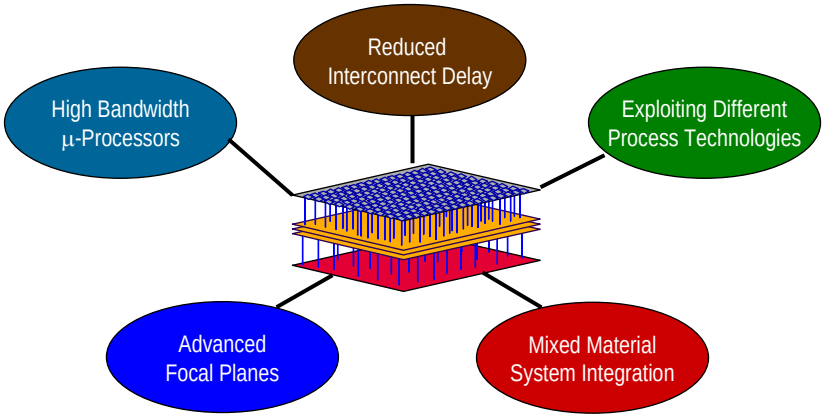
Craig Keast, Brian Aull, Jim Burns, Nisha Checka, Chang-Lee Chen, Chenson Chen, Jeff Knecht, Brian Tyrrell, Keith Warner, Bruce Wheeler, Vyshi Suntharlingam, Donna Yost

keast@LL.mit.edu
MIT Lincoln Laboratory



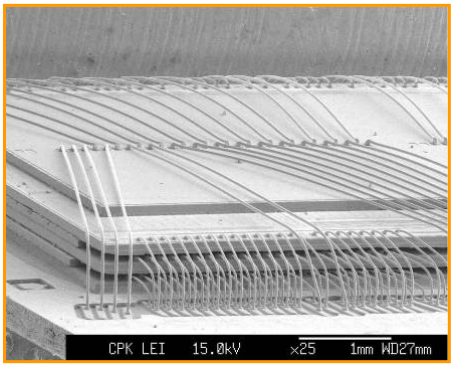
*This work was sponsored by the Defense Advanced Research Projects Agency under Air Force contract #FA8721-05-C0002. Opinions, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the United States Government .

Motivation for 3-D Circuit Technology



Pad-Level "3D Integration"
Die Stacking

Stacked-Die Wire Bonding



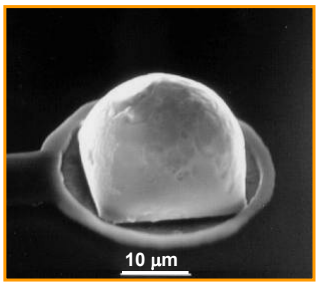
ChipPAC, Inc.

Stacked Chip-Scale Packages

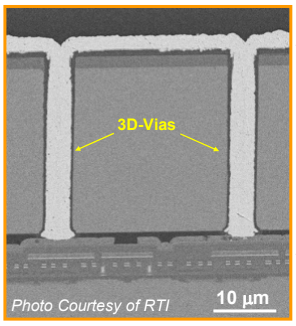
Tessera, Inc.

In Production!

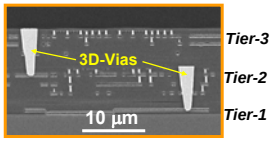
Approaches to High-Density 3D Integration
(Photos Shown to Scale)



Bump Bond used to flip-chip interconnect two circuit layers



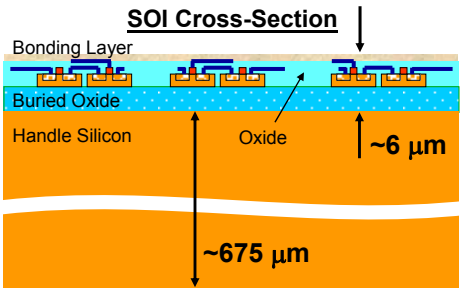
Two-layer stack with insulated vias through thinned *bulk* Si



Three-layer circuit using MIT-LL's SOI-based vias

Advantages of Silicon-on-Insulator (SOI) for 3-D Circuit Integration

- The electrically active portion of an integrated circuit wafer is < 1% of the total wafer thickness
- Buried oxide layer in SOI provides ideal etch stop for wafer thinning operation prior to 3D integration

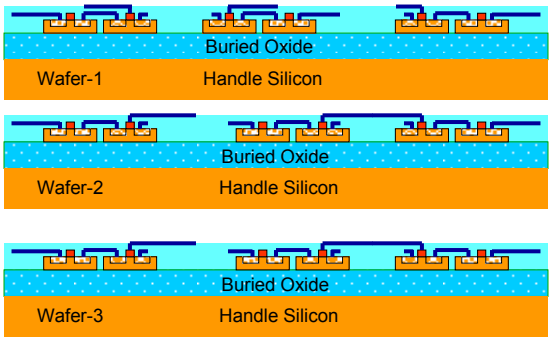


- Full oxide isolation between transistors allows direct 3D via formation without the added complexity of a via isolation layer
- SOI's enhanced low-power operation (compared to bulk CMOS) reduces circuit stack heat load

3-D Circuit Integration Flow-1

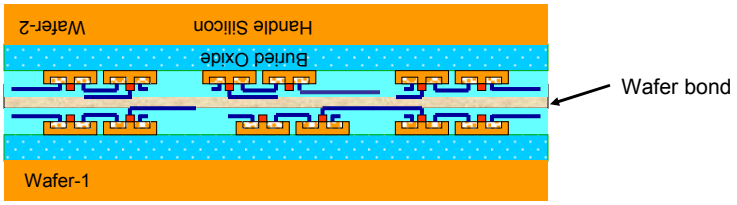
- Fabricate circuits on SOI wafers
  - SOI wafers greatly simplify 3D integration
- 3-D circuits of two or more active silicon layers can be assembled

Wafer-1 can be either Bulk or SOI

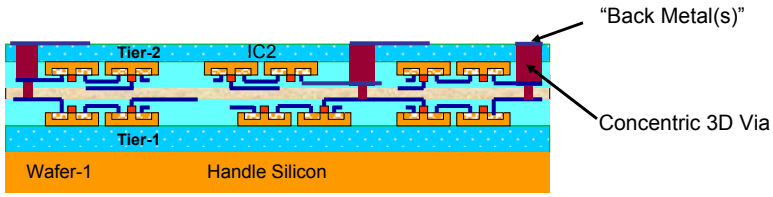


3-D Circuit Integration Flow-2

- **Invert, align, and bond Wafer-2 to Wafer-1**

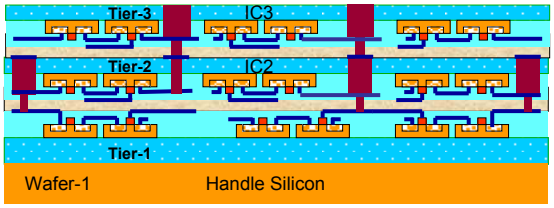


- **Remove handle silicon from Wafer-2, etch 3D vias, deposit and CMP damascene tungsten interconnect metal**

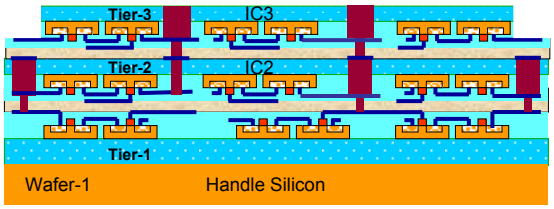


3-D Circuit Integration Flow-3

- **Invert, align, and bond Wafer-3 to Wafer-2/1-assembly, remove Wafer-3 handle wafer, form 3D vias**

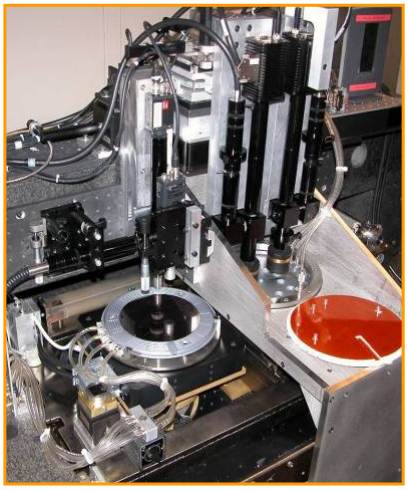


- **Etch Bond Pads**

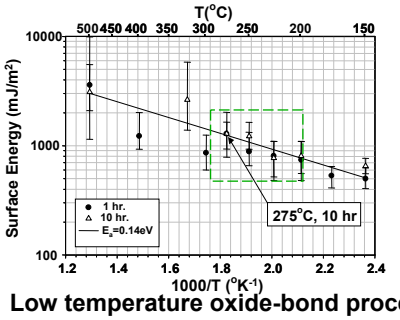


IEEE Trans. on Electron Devices, Vol. 53, No. 10, October 2006

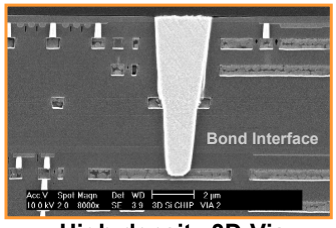
3D-Specific Enabling Technologies



Precision wafer-wafer alignment



Low temperature oxide-bond process

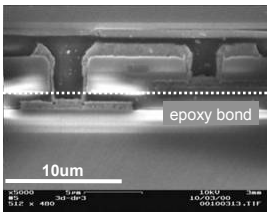


High-density 3D-Via

MIT-LL 3D Via History

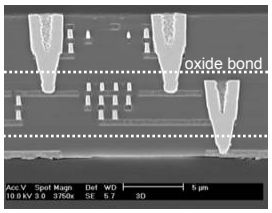
(Photos Shown with Same Scale and Drawn 3D Via Size)

3 µm
Oct 2000



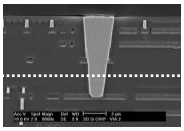
64 x 64, 12-µm active-pixel sensor[1]

2 µm
Dec 2004



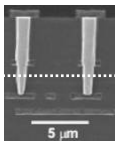
1024×1024, 8-µm pixel visible image sensor[2]

1.75 µm
May 2005



64 x 64, 50-µm pixel LADAR[3]

1.0 µm
Sept 2006



Scaled 3D via

[1] J. Burns, et al., "Three-dimensional integrated circuits for low-power high-bandwidth systems on a chip," in *Proc. Papers IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2001, pp. 268-269.

[2] V. Suntharalingam, et al., "Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology," in *Proc. Papers IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2005, pp. 356-357.

[3] B. Aull, et al., "Laser radar imager based on three-dimensional integration of Geiger-mode avalanche photodiodes with two SOI timing-circuit layers," in *Proc. Papers IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2006, pp. 304-305.

First 3-D IC *Multiproject Run*

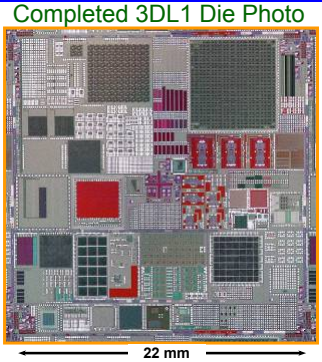
(Three 180-nm, 1.5 volt FDSOI CMOS Tiers)

- Leverages MIT-LL's established 3D circuit integration technology
  - Low temperature oxide bonding, precision wafer-to-wafer overlay, high-density 3D interconnect
- Preliminary 3D design kits developed
  - Mentor Graphics – *MIT-LL*, Cadence – *NCSU*, Thermal Models – *CFRDC*
- Design guide release 11/04, fab start 6/05, 3D-integration complete 3/06

Concepts being explored in run:

- 3D FPGAs, digital, and digital/mixed-signal/RF
- ASICs exploiting parallelism of 3D-interconnects
- 3D analog continuous-time processor
- 3D-integrated S-band digital beam former
- Stacked memory (SRAM, Flash, and CAM)
- Self-powered CMOS logic (scavenging)
- Integrated 3D Nano-radio and RF tags
- Intelligent 3D-interconnect evaluation circuits
- DC and RF-coupled interconnect devices
- Low Power Multi-gigabit 3D data links
- Noise coupling/cross-talk test structures and circuits
- Thermal 3D test structures and circuits

Completed 3DL1 Die Photo



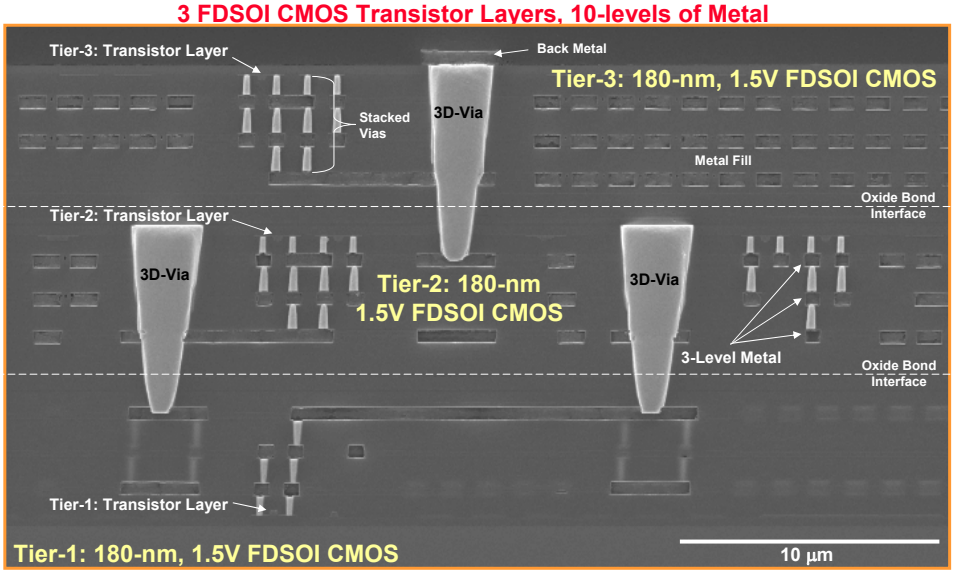
3DL1 Participants (Industry, Universities, Laboratories)

BAE	Lincoln Laboratory	Purdue
Cornell	Maryland	RPI
Delaware	Minnesota	Stanford
HRL	MIT	Tennessee
Idaho	North Carolina State	UCLA
Johns Hopkins	NRL	Washington
LPS	Pennsylvania	Yale

Cross-Section of 3-Tier 3D-integrated Circuit

(DARPA 3DL1 *Multiproject Run*)

3 FDSOI CMOS Transistor Layers, 10-levels of Metal



Second 3D IC Multiproject Run (3DM2)

(Three Tiers of 180-nm 1.5-volt FDSOI CMOS)

- **3DM2 run announced** (March 2006)
- **3D design kits released** (April 2006)
  - Mentor Graphics (*MIT-LL)*
  - Cadence (*NCSU)*
  - Tanner Tools

3DM2 Submissions (October 2006)

3D Circuits

FPGA, stacked memory (SRAM & CAM), asynchronous microprocessor, FFT with on-chip memory, multi-processor chip with high-speed RF interconnect, ASIC with DC-DC converter, reconfigurable ΔΣ modulator, decoder with 3-cube torus network, self-powered and mixed-signal RF chips

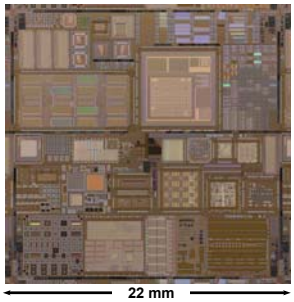
3D Imaging Applications

ILC pixel readout, high-speed imaging FPA, 3D adaptive image processor, artificial bio-optical sensor array, 3D retina, 3D-integrated MEMS biosensor, sensor lock-in-amplifier

3D Technology Characterization

3D signal distribution, 3D interconnect methods, parasitic RF & 3D radiation test structures

3DM2 Die Photo



3DM2 Participants (Industry, Universities, Laboratories)

Cornell	Minnesota	SUNY
Fermi Lab	NCSU	Tanner
Idaho	NRL	Tennessee
Intel	Pittsburgh	UCLA
Johns Hopkins	RPI	Washington
Lincoln Lab	Rochester	Yale
Maryland	Sandia	

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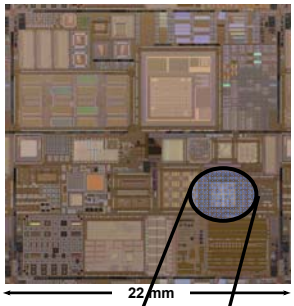

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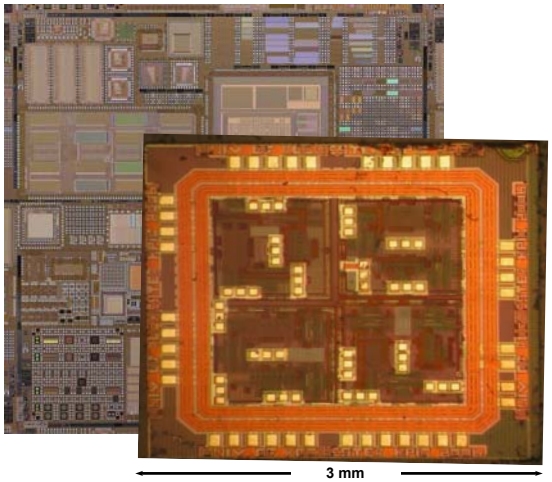
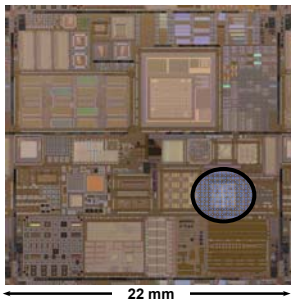
Johns Hopkins	RPI	Washington
Lincoln Lab	Rochester	Yale
Maryland	Sandia	

MIT Lincoln Laboratory

Second 3D IC Multiproject Run (3DM2)

(Three Tiers of 180-nm 1.5-volt FDSOI CMOS)

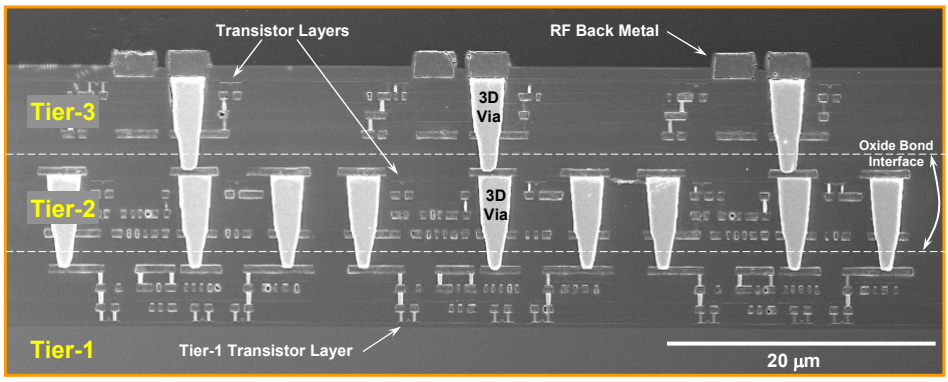




3-Tier 3DIC Cross-Section

Second DARPA *Multiproject Run* (3DM2)

Two Digital & One RF 180-nm 1.5V FDSOI CMOS Tiers



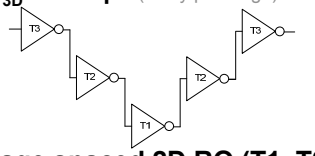
3DM2 Process Highlights

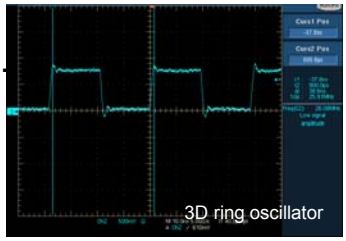
- 11 metal interconnect levels
- 1.75-µm 3D via tier interconnect
- Stacked 3D vias allowed
- Tier-2 back-metal/back-via process
- 2-µm-thick RF back metal
- Tier-3 W gate shunt
- Tier-3 silicide block

3D Ring Oscillators (3DM2)

Measuring 3D-Via Parasitics

- **93-stage optimized 3D ring oscillator**
  - **Devices in all three tiers; T3,T2,T1,T2,T3 ..**
  - **τ_{3D} = 40.6 ps** (delay per stage)



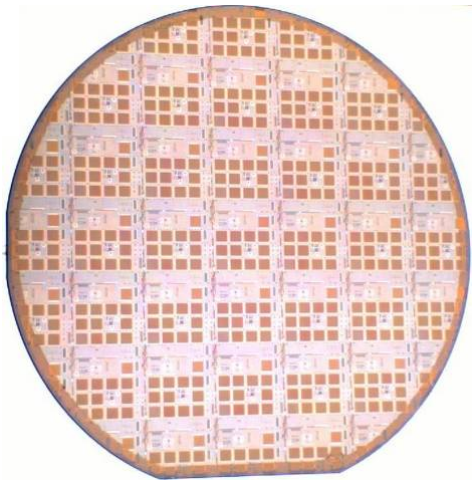


- **93-stage spaced 2D RO (T1, T2, & T3)**
  - **τ_{2D} = 31.6 ps**
- **93-stage optimized 2D RO (T1, T2, & T3)**
  - **τ_{2D} = 26.9 ps**
- **3D via characteristics**
  - **Resistance ~1 ohm**
  - **Capacitance ~2 fF** (roughly equivalent to 10-μm long x 0.5-μm wide metal interconnect)

3D-Integration with III-V Detectors

Presented at 2006 IPRM

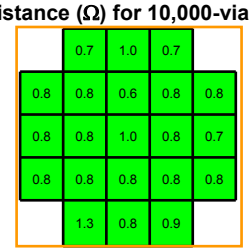
- **Enables extension of 3D-integration technology to higher density, longer wavelength focal plane detectors**
  - **Tight pixel-pitch IR focal planes and APD arrays**
  - **InGaAsP (1.06-μm), InGaAs (1.55-μm)**

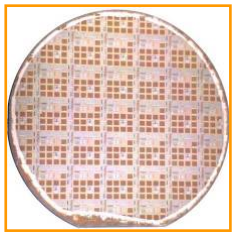


150-mm-diameter InP wafer with oxide-bonded circuit layer transferred from silicon wafer

Transferred CMOS-to-InP Integration
(Via-Chain Test Results)

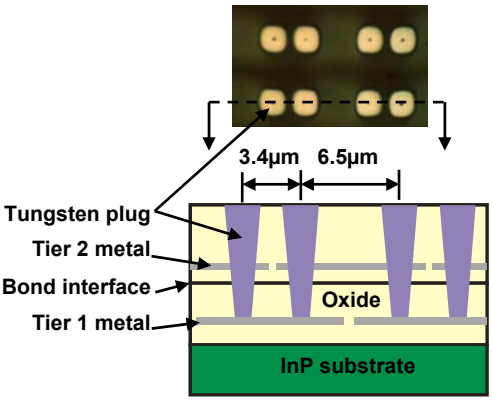
Wafer Die Map of Average 3D-Via Resistance (Ω) for 10,000-via Chains



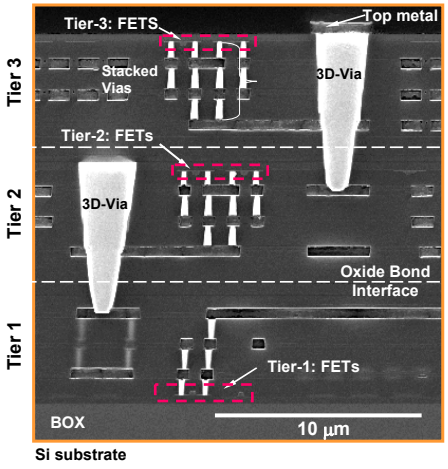


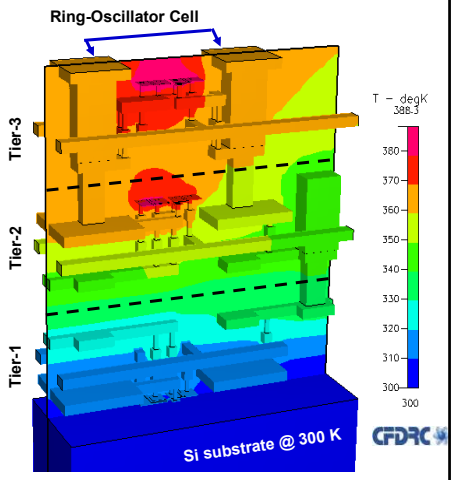
Photograph of 150-mm InP Wafer with Aligned and Bonded Tier

- **MIT-LL 3D integration and via processes successfully demonstrated on 150-mm InP wafers**



SEM Cross Section and Thermal Simulation of 3D Circuit Stack





Simulation of temperature distribution of ring oscillator in 3D circuit

2007 SOI Conference Papers 6.2 and 6.3 by T.W. Chen, et. al., and C.L. Chen, et. al.

Closing Remarks…

- **3D Integration *(at least as implemented by MIT-LL)* is not cheap… Application/benefit-gained better justify the cost**
  - **Issues: Alignment, Compounded yield loss, Heat dissipation in the stack**
- **Initial technology demonstrations (at MIT-LL) are centered around advanced focal plane architectures**
  - **This is the "low hanging fruit"**
- **Full impact of 3D integration is far from being realized, but has the potential of revolutionizing the design architecture of future circuits and systems**
- **Potential application areas include: High-end focal planes, FPGAs, Dense memory, memory on processor, mixed signal systems, mixed material systems**
  - **Need to design for 3D from ground-up for maximum benefit**
    - **Will need the CAD tools to support the design effort**

Presentation Outline

- Three-dimensional (3-D) integration
- MIT Lincoln Laboratories 3-D Technology
- Physical design issues in 3-D integration
- 3-D networks-on-chip
- The Rochester cube
- Near and long-term research problems
- Conclusions

Objectives for 3-D CAD Tools

"New design tools will be required to optimize interlayer connections for maximized circuit performance…"

TSVs
- Density / consume silicon area
- Impedance characteristics

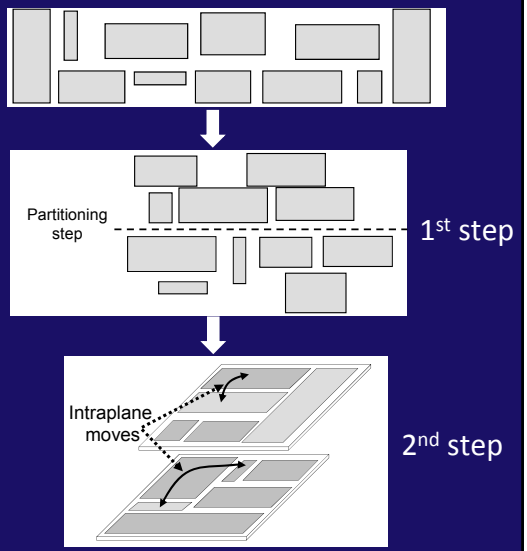
Heterogeneity
- Interdie process variations
- Disparate technologies

Interconnect length
- Longest nets in a 3-D system

*M. Ieong *et al.*, "Three Dimensional CMOS Devices and Integrated Circuits," *Proceedings of the IEEE International Custom Integrated Circuits Conference,* pp. 207-213, September 2003

3-D Floorplanning and Placement

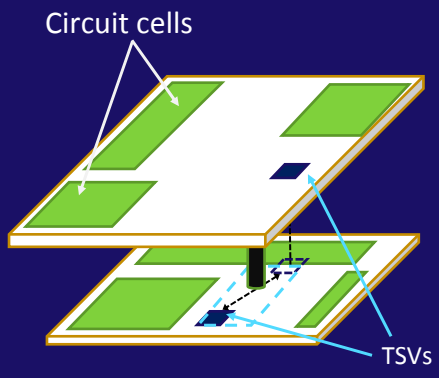
- Third dimension greatly increases the solution space
- Adopt a two-step solution



*T. Yan, Q. Dong, Y. Takashima, and Y. Kajitani, "How Does Partitioning Matter for 3D Floorplanning," *Proceedings of the ACM International Great Lakes Symposium on VLSI,* pp. 73-76, April-May 2006

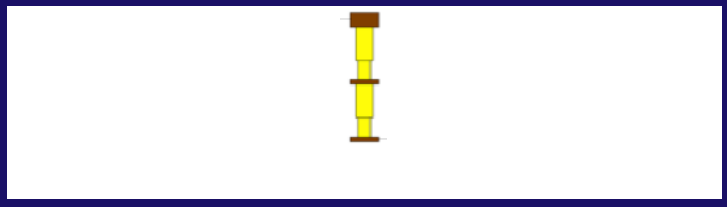
Through Silicon Via (TSV) Placement

- Treat TSVs as circuit cells
  - Use weighted average distance to determine final via location
- Place the cells of each plane separately
  - Including vias



[*]W. R. Davis *et al.*, "Demystifying 3D ICs: The Pros and Cons of Going Vertical," *IEEE Design and Test of Computers Magazine*, Vol. 22, No. 6 , pp. 498-510, November/December 2005

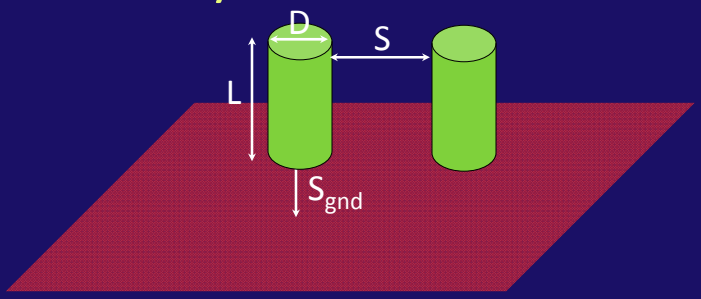
TSV Characterization / Design



- Impedance characterization of TSV
- Physical models of TSVs
  - Distributed vs. lumped models
  - Closed-form expressions
- Circuit design techniques
  - Repeater insertion before and after via
  - Return path requirements to minimize loop inductance
- Inductive and capacitive coupling noise between TSVs
  - TSV-to-TSV shielding methodologies

I. Savidis and E. G. Friedman, " Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices* (in press).

TSV Physical Parameters



- Equations model TSV electrical characteristics
  - TSV diameter *D* and length *L*
    - 0.5 < Aspect ratio < 9
  - Distance of TSV from ground plane S_{gnd}
  - Spacing *S* to neighboring TSVs
    - Capacitive coupling
    - Loop inductance

TSV Impedance Models

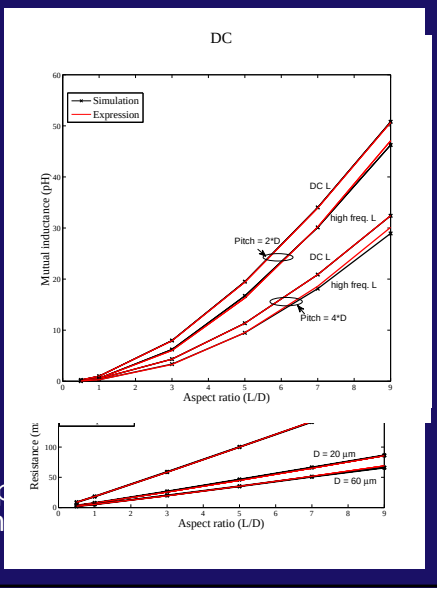
I. Savidis and E. G. Friedman, " Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices* (in press).

- DC Resistance: < 2%
- 1 GHz Resistance: < 4.5%
- 2 GHz Resistance: < 5.5%

- Self Inductance L_{11}: ≤ 8%
- Mutual Inductance L_{21}: ≤ 8%*

- Capacitance to ground: ≤ 8%
- Coupling Capacitance: ≤ 15%*

* Error in mutual inductance and coup
for smaller aspect ratios and distan
produce small L_{21} and C_c values



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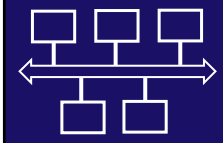
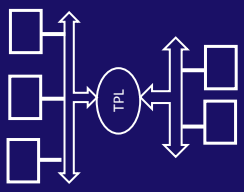
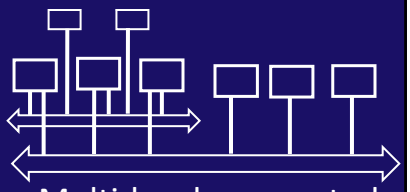
Evolution of Interconnect Architectures



- Shared buss

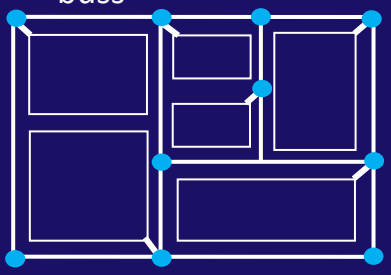


- Segmented buss



- Multi-level segmented buss

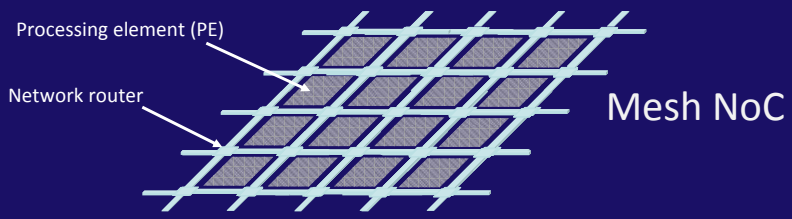
- Buss architecture limitations
  - Large buss delays
  - Data contention for resources
  - Signal integrity



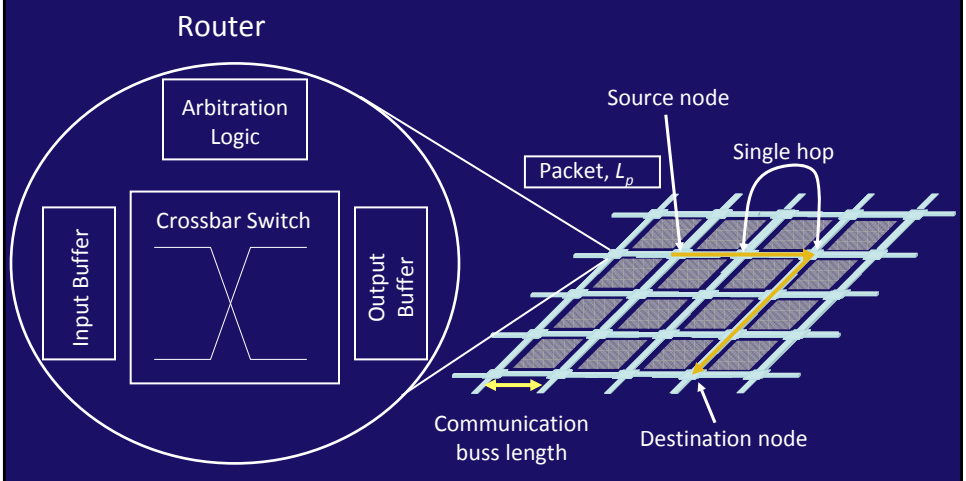
- Network-on-chip

Network-on-Chip (NoC)

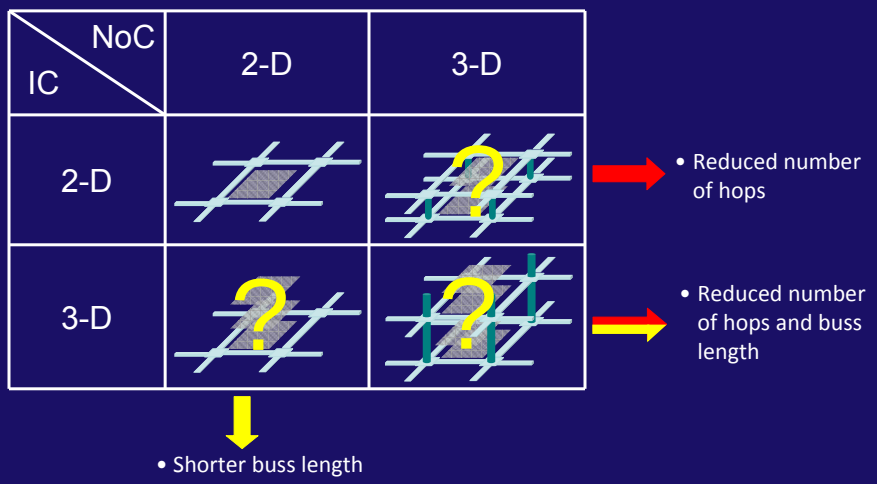
- Network-on-chip is another approach to mitigate the interconnect bottleneck in modern IC design
  - Canonical interconnect structure
  - Shared interconnect bandwidth
  - Increased flexibility
- PEs exchange data packets through the network in an internet-like manner
- Network routers transfer data within the network similar to computer networks



NoC Mesh Structure



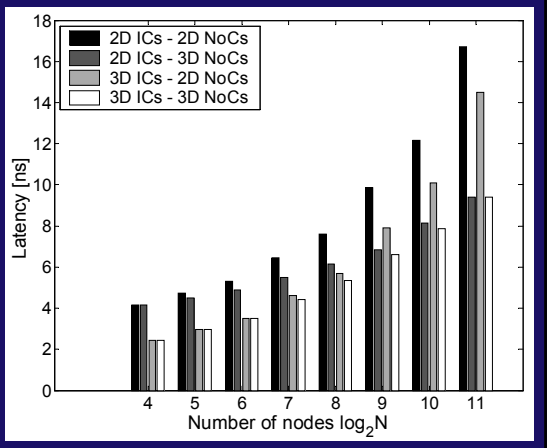
Various Topologies for 3-D Mesh IC-NoC



*V. F. Pavlidis and E. G. Friedman, "3-D Topologies for Networks-on-Chip," *IEEE Transactions on Very Large Integration (VLSI) Systems,* Vol. 15, No. 10, pp. 1081-1090, October 2007

Performance Comparison for 3-D NoC Topologies

- Dense networks with small PE areas favor 3-D NoCs and 2-D ICs
  - Due to large number of hops and short busses
- Small networks with large PE areas favor 3-D IC and 2-D networks
  - Due to small number of hops and long busses



- A_{PE} = 4 mm^2
- Improvement = 36.2%, N = 256

*V. F. Pavlidis and E. G. Friedman, "3-D Topologies for Networks-on-Chip," *Proceedings of the IEEE International SOC Conference*, pp. 285-288, September 2006

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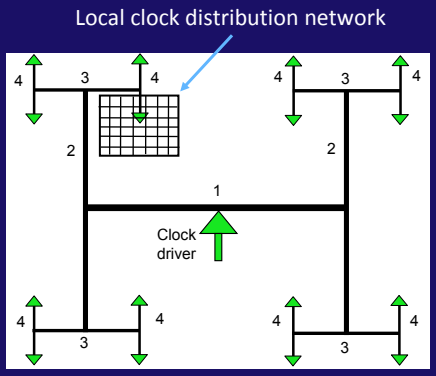
"15 Minutes of Fame"

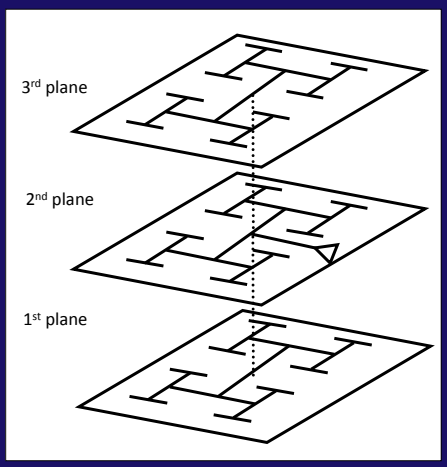
Clock Distribution Networks

- Clock signal is the "heart" of synchronous circuits
- VDSM technologies
  - Increasing frequencies
  - Greater process variations
  - Clock skew, jitter should be carefully managed
- Hierarchical clock distribution networks
  - Global networks
    - H-tree, X-tree
  - Local networks
    - Meshes



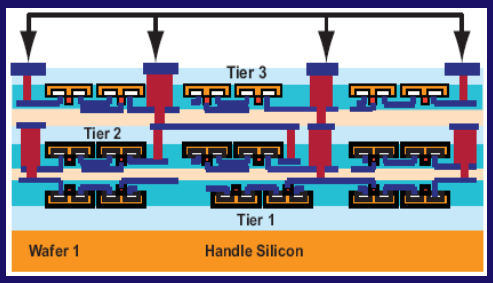
Clock Signal Distribution for 3-D ICs

- Multiplane system
  - Process variations
- Different forms of 3-D integration
  - System-in-Package (SiP)
  - 3-D ICs (high density vias)
- Clock signal distribution under pronounced thermal effects



MIT Lincoln Laboratories 3-D IC Fabrication Process

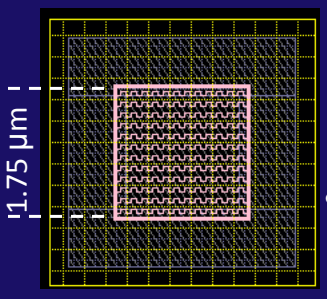
- FDSOI 180 nm CMOS process
  - Three plane process
  - Three metal layers for each plane
  - Back side metal layer for planes 2 and 3
  - One polysilicon layer
- 1.75 µm × 1.75 µm cross section of TSVs
  - For the 2nd 3-D multiproject



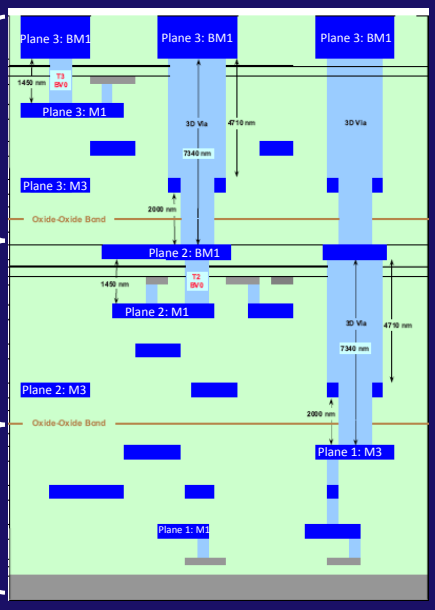
- Planes one and two
  - Face to face bonding
- Planes two and three
  - Back to face bonding

*Massachusetts Institute of Technology Lincoln Laboratory, *FDSOI Design Guide*

Cross-Section of 3-D Interconnect



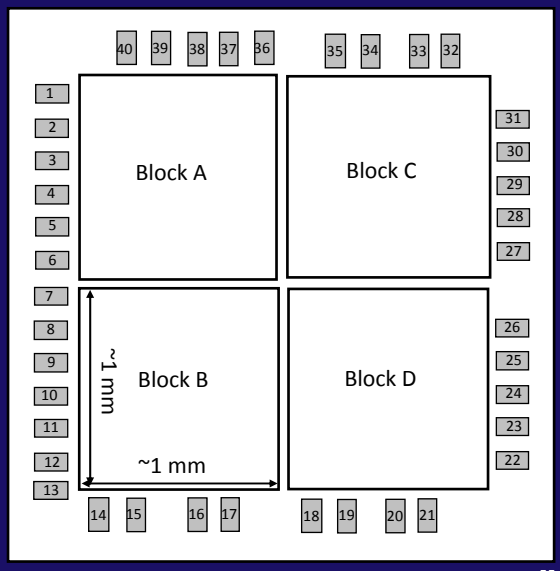
- Interplane via



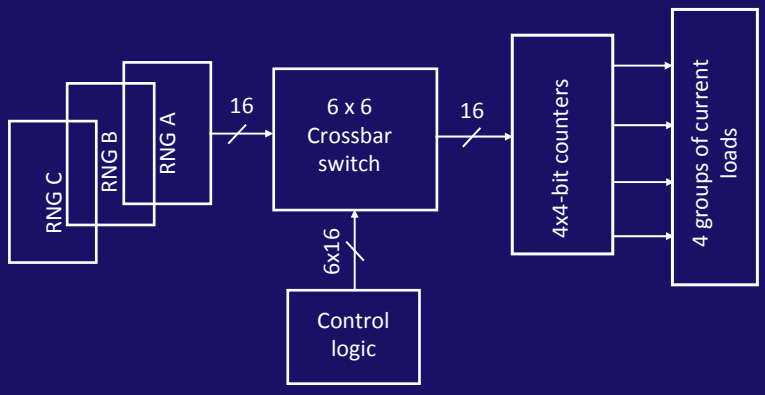
- Plane 3
- Plane 2
- Plane 1

Block Diagram of the 3-D Test Circuit

- Each block includes
  - Identical logic
  - Different clock distribution network
- Objectives
  - Evaluate clock skew
  - Measure power consumption
- Area - 3 mm × 3 mm

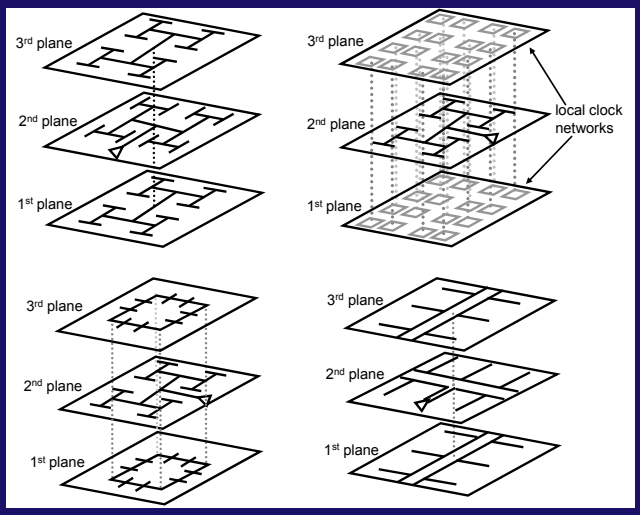


Logic Circuitry



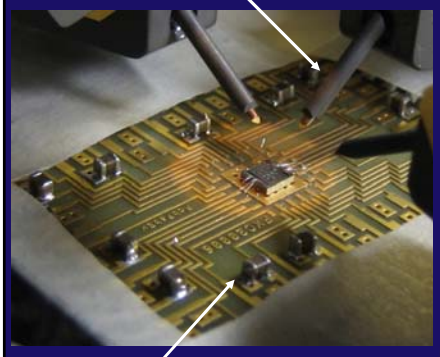
- Current loads mimic various switching patterns
- Control logic periodically changes the connectivity among the input and output ports

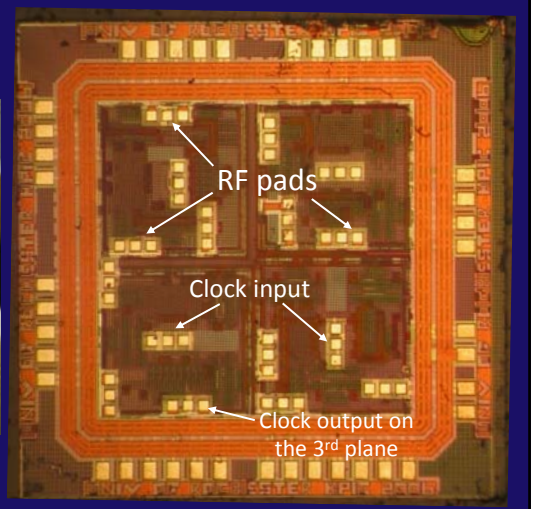
3-D Clock Distribution Networks



- The clock network on the 2nd plane is rotated by 90° to eliminate inductive coupling

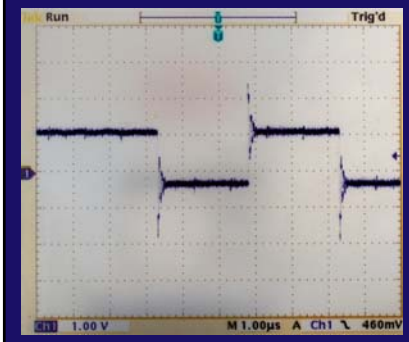
Fabricated 3-D Test Circuit

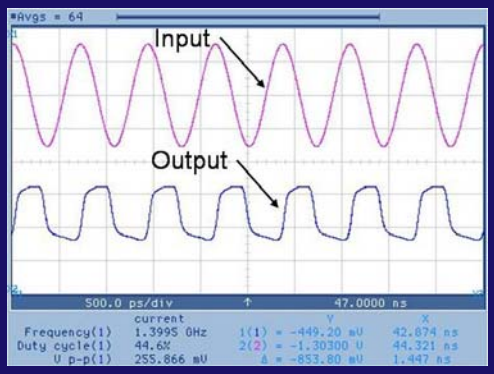




- Full custom design
- ~ 120K transistors

Clock and Data Waveforms

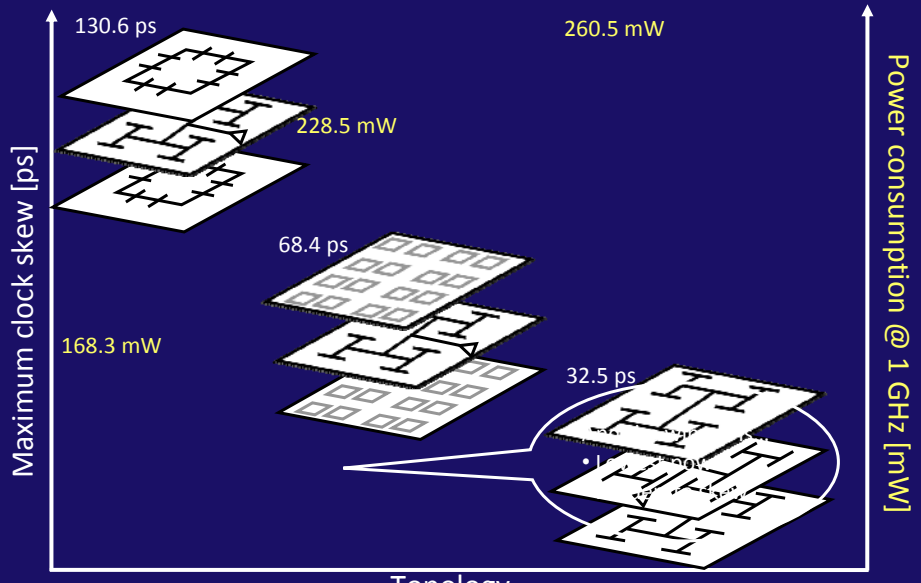




- Output bit at 1 MHz
- Clock output at 1.4 GHz from the 3rd plane

*V. F. Pavlidis and E. G. Friedman, "Interconnect-Based Design Methodologies for Three-Dimensional Integrated Circuits," *Proceedings of the IEEE,* January 2009 (in press).

Clock Skew and Power Measurements



*V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks for 3-D ICs," *Proceedings of the IEEE International Custom Integrated Circuits Conference,* September 2008

Design Issues Related to the 3-D MITLL Fabrication Process

- CAD support from NCSU
  - Cadence design framework
  - Design rule checking
  - Automated synthesis and place and route
- Limitations
  - Electrical rule checking
  - Full 3-D visualization
  - Impedance extraction
    - Particularly for 3-D vias
  - Bugs included!!! ☺

- Sophisticated CAD tools for 3-D ICs remain an important challenge

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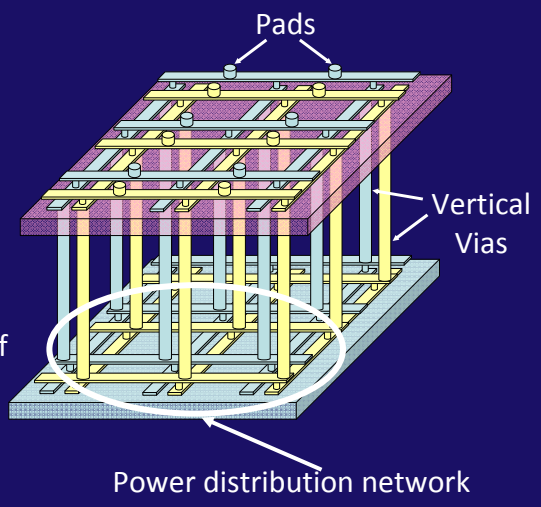
3-D Interconnect Design Issues

- Global signaling
  - Clock and power distribution networks
  - Long distance signaling
- Noise aware design methodologies
  - Due to the adjacency of the physical planes



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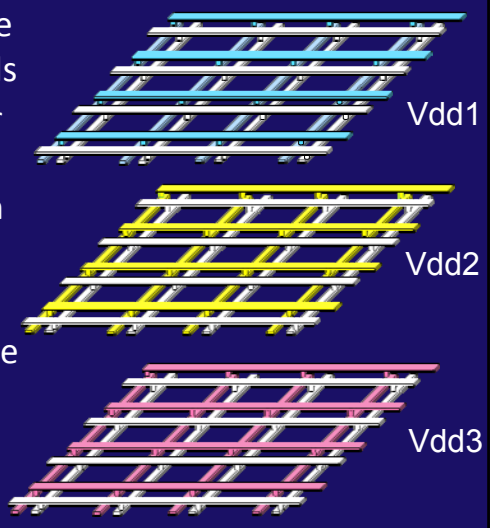
  - 3-D power delivery
  - Heterogeneity / optical interconnect
- Conclusions

Effective Power Distribution and Delivery Will be Essential

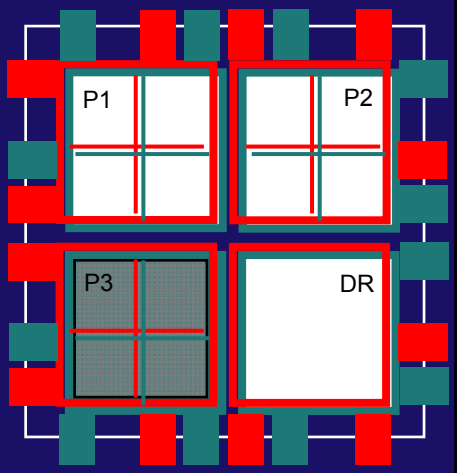
- All but one of the planes are located next to the P/G pads
  - TSVs convey current to other planes
- Decoupling capacitance can be placed within or on a nearby plane
- Multiple power levels will be a necessity
  - Due to thermal issues
  - Heterogeneous technologies
  - Lower power consumption



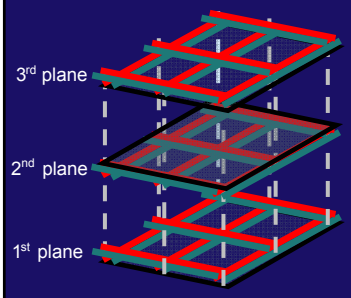
Power Delivery Test Chip

Design Objectives

- Blocks P1 - P3
  - Three different power distribution networks
  - Investigate variations in noise for each power network
- Block DR
  - Distributed rectifier circuit for application to DC-to-DC buck converters



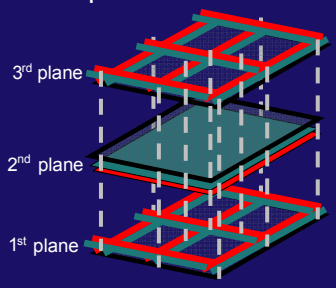
Power Distribution Network Topologies for 3-D ICs

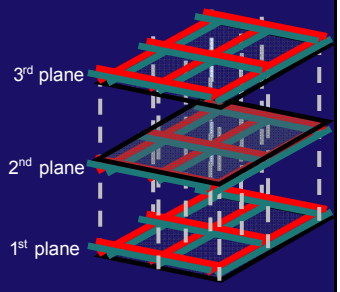


P1: interdigitated

- 3-D vias on periphery

P3: gnd planes on plane 2, interdigitated on planes 1 and 3

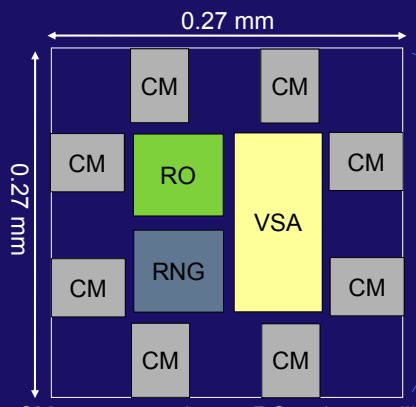


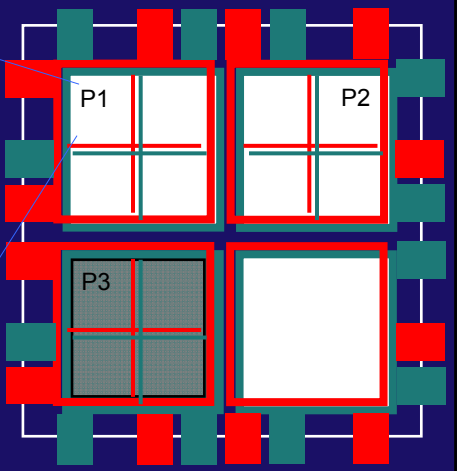


P2: interdigitated

- 3-D vias on periphery and through middle

Noise Detection Circuitry

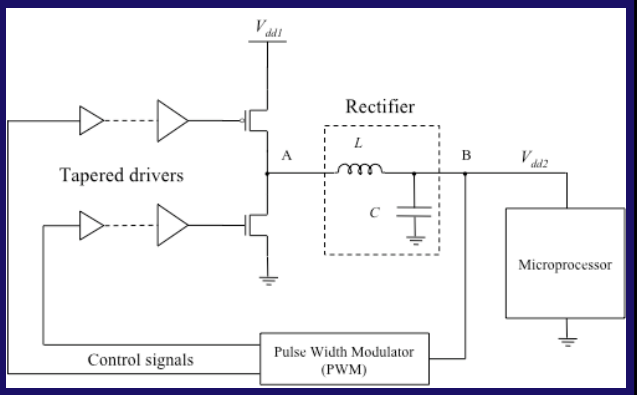




- Voltage sense amps are used to detect and measure noise on each plane for each power distribution topology
  - Noise analyzed on both V_{DD} and ground lines

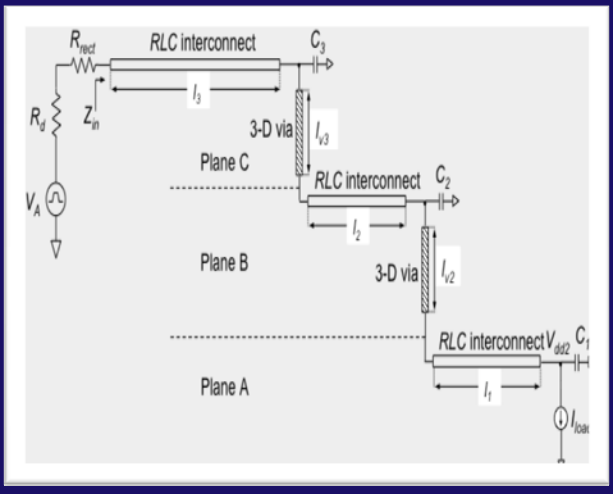
Standard Buck Converter

- Generates an output supply voltage
  - Smaller than the input supply
- Power MOSFETs produce an AC signal at node A
- AC signal is filtered by rectifier
  - Second order low pass band *LC* filter
- Filter passes the DC component of the signal and a residue
  - Composed of high frequency harmonics
- Buck converter produces an output DC voltage at node B
  - Equal to product DV_{dd1}



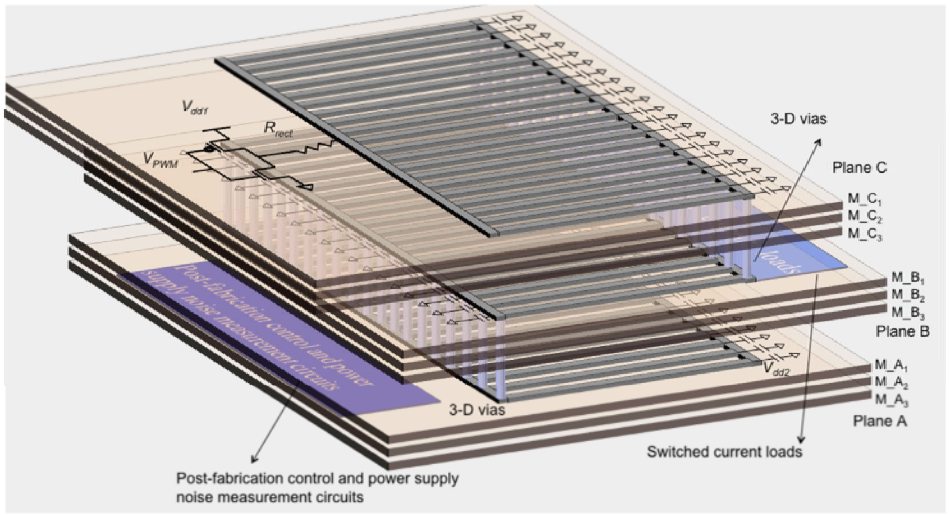
Distributed On-Chip Rectifier

- Exploits rectifier portion of buck converter
  - Generates and distributes power supplies in 3-D integrated circuits
  - Eliminates need for on-chip inductors
- Rectifier is composed of transmission lines
  - Terminated with lumped capacitances
- Inter-plane structure is connected by 3-D TSVs
- Low pass behavior
  - *RC*-like characteristics
  - Sharp roll-off
    - Due to distributed nature

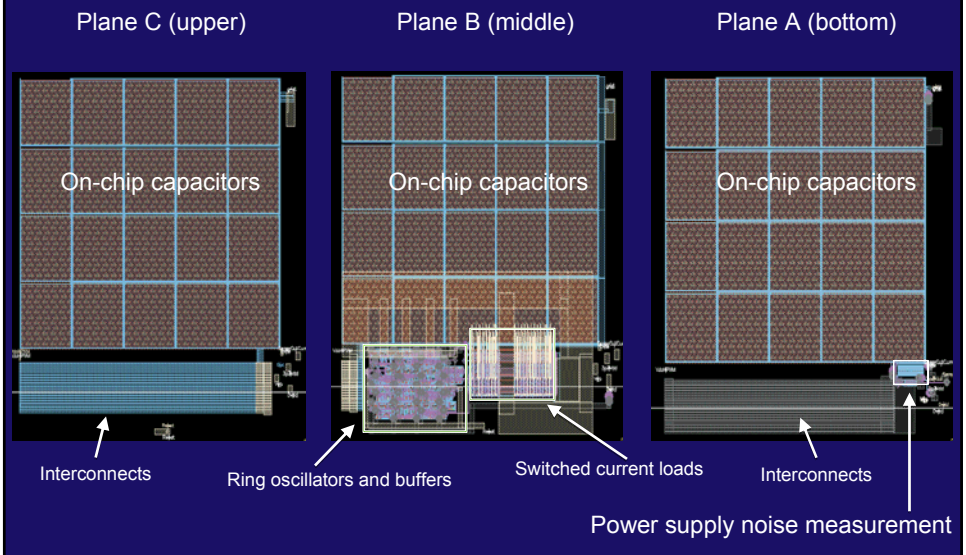


J. Rosenfeld and E. G. Friedman, "'On-Chip DC-DC Converters for Three-Dimensional ICs," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, March 2009.

Schematic Structure of the 3-D Rectifier

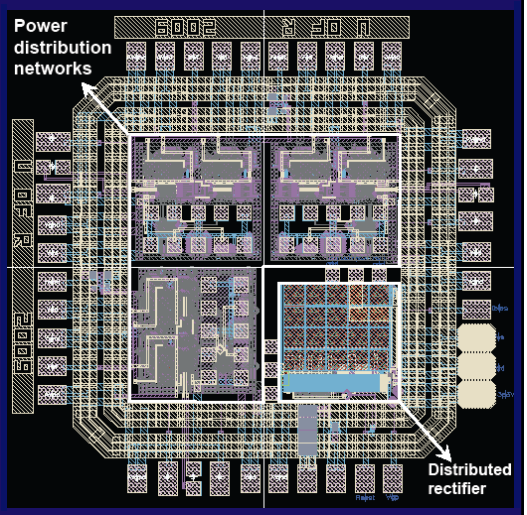


Physical Layout of the Distributed Rectifier



Power Delivery Test Circuit

- Lincoln Lab 3-D CMOS process
  - 150 nm FDSOI
  - Three physical planes
  - Three metal layers per plane
  - Back side metal on top two planes
  - Each wafer is separately processed

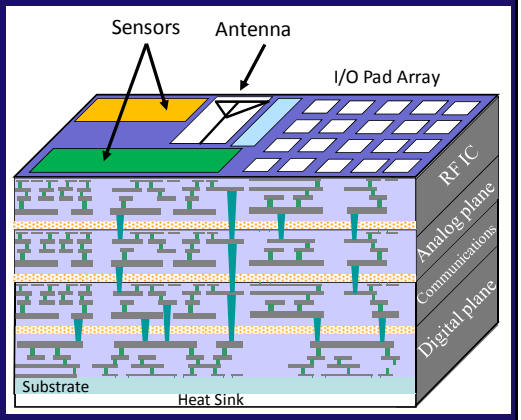


Presentation Outline

- Three-dimensional (3-D) integration
- MIT Lincoln Laboratories 3-D Technology
- Physical design issues in 3-D integration
- 3-D networks-on-chip
- The Rochester cube
- Near and long-term research problems
  - 3-D power delivery
  - Heterogeneity / optical interconnect
- Conclusions

Design Methodologies for Heterogeneous 3-D Integrated Systems

- Integrate processing and sensing within a multi-plane system
- Develop design methodologies to prevent processing planes disturb sensor planes
- Develop general purpose processing planes
  - Compatible with
    - Different types of sensors
    - Disparate communication schemes



Presentation Outline

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Conclusions

- Three-dimensional integration is a promising solution to expected limits of scaling
- Interplane through silicon vias (TSVs) are the key
- Advanced and novel 3-D architectures are now possible
- We've demonstrated a 3-D circuit operating at 1.4 GHz
  - 3-D power delivery test circuit currently in manufacture
  - More to come from many sources
- 3-D integration is a likely next step in the evolution of semiconductor technology

Thank you for your attention!