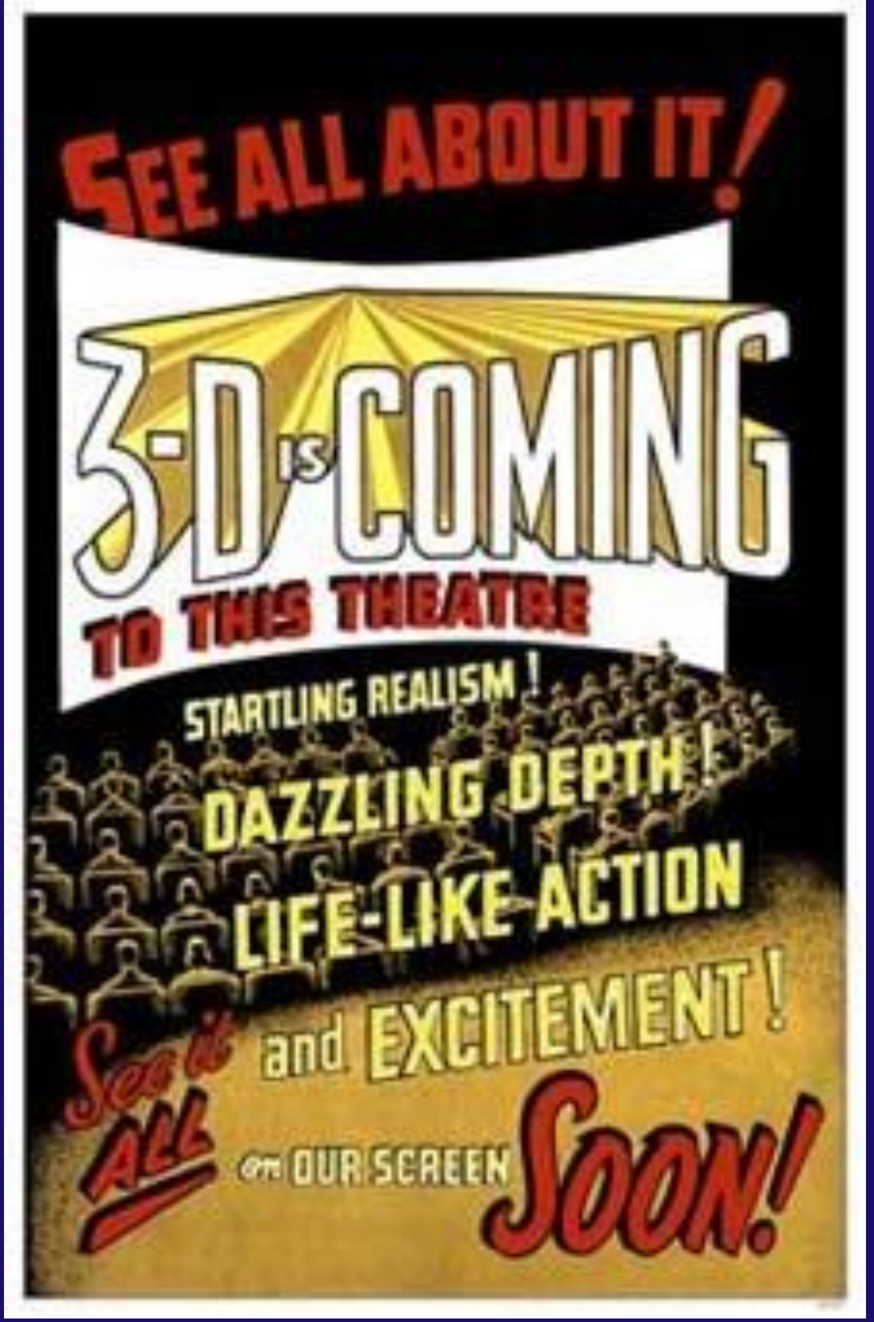
3-D Design: Architectures, Methodologies, and Test Circuits

Eby G. Friedman
University of Rochester

www.ece.rochester.edu/~friedman

June 11, 2010

2nd Design for 3-D Silicon Integration Workshop


SEE ALL ABOUT IT!
3-D IS COMING
TO THIS THEATRE
STARTLING REALISM!
DAZZLING DEPTH!
LIFE-LIKE ACTION
and EXCITEMENT!
See it ALL
on OUR SCREEN
SOON!

Presentation Outline

- Three-dimensional (3-D) integration
- Physical design techniques
- TSV modeling
- Design methodologies and flow
- 3-D architectures
- Rochester test chips – past, present, and future
- Conclusions

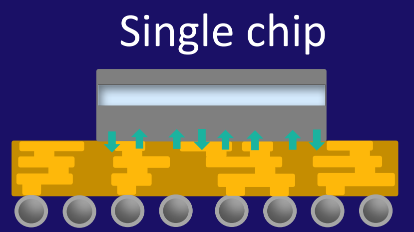
Presentation Outline

- ***Three-dimensional (3-D) integration***
- Physical design techniques
- TSV modeling
- Design methodologies and flow
- 3-D architectures
- Rochester test chips – past, present and future
- Conclusions

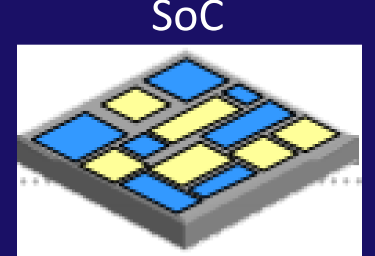
Evolution of 3-D Integration

In the beginning...

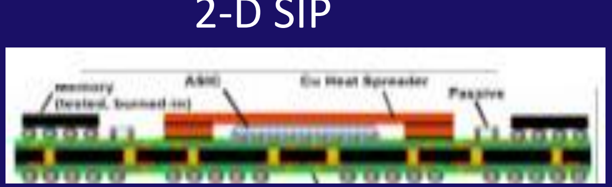
Single chip



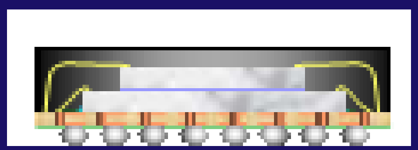
SoC

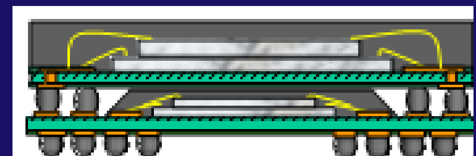


2-D SIP

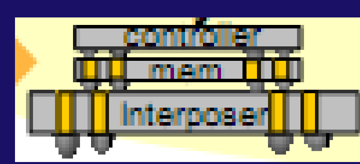


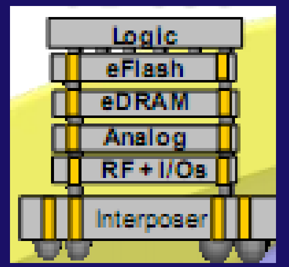
then came wire bonding



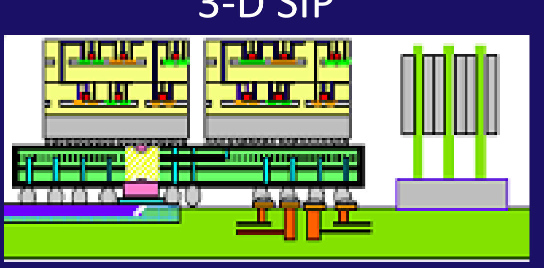


and finally through silicon vias

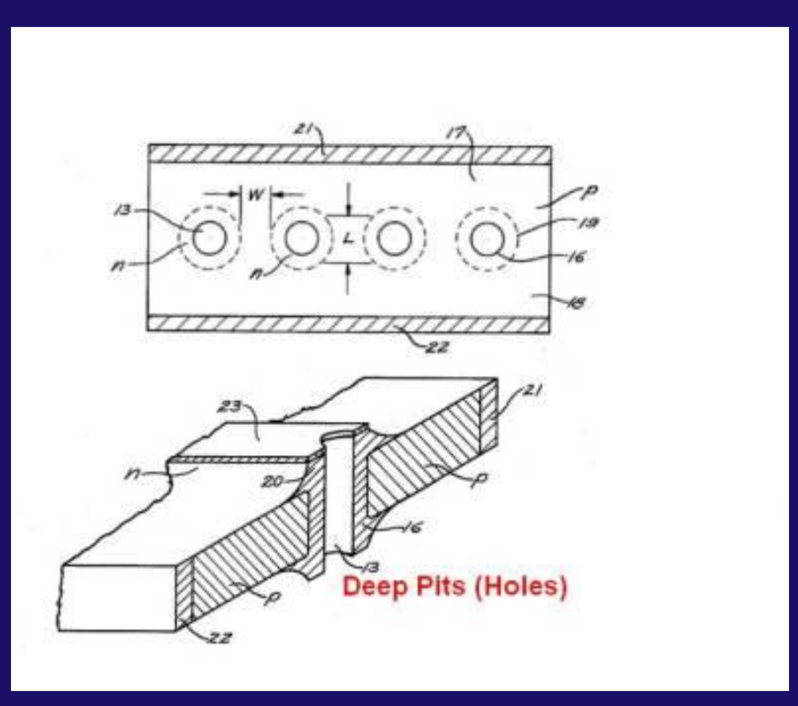


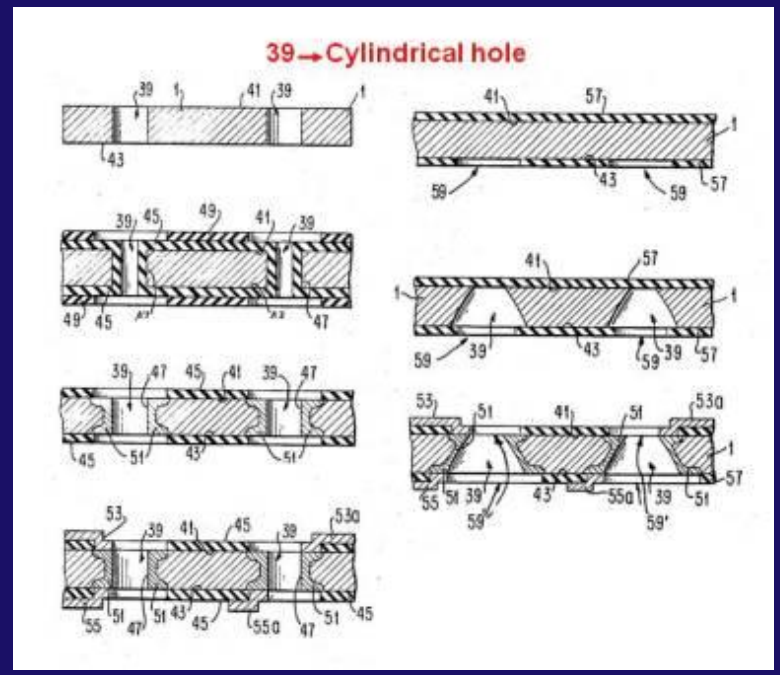


3-D SIP



First Through Silicon Vias





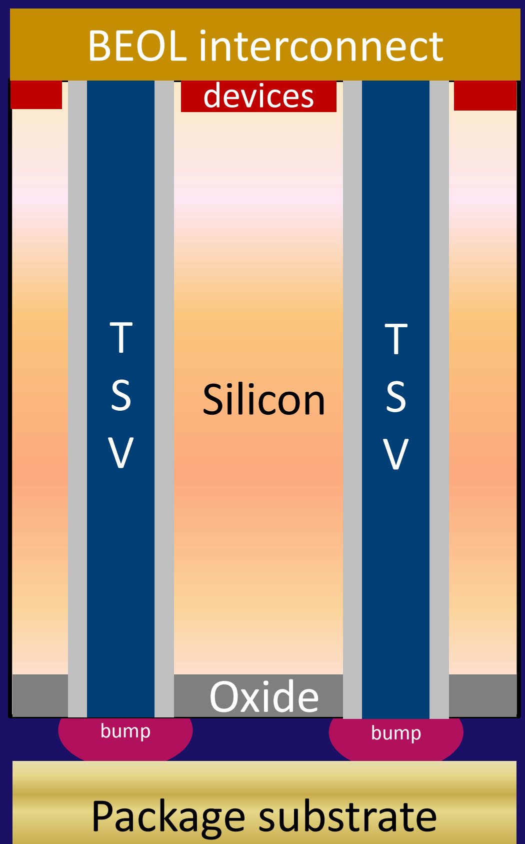
William Shockley

Patent - “Semiconductive Wafer and Method of Making the Same”
Filed: October 23, 1958
Granted: July 17, 1962

Merlin Smith and Emanuel Stern

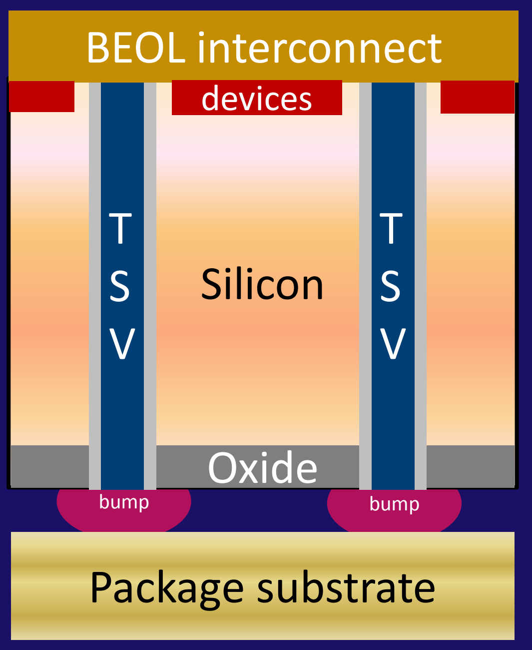
Patent - “Methods of Making Thru-Connections in Semiconductor Wafers”
Filed: December 28, 1964
Granted: September 26, 1967

Evolution of the 3-D Via



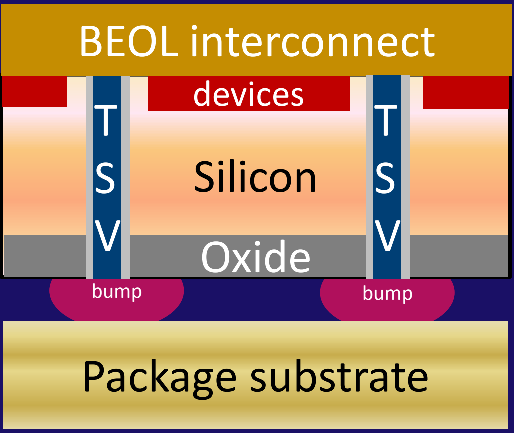
~ 2000 - 2005

- TSV length
  - 125 to 250 µm
- TSV diameter
  - 40 to 70 µm



~ 2004 - 2007

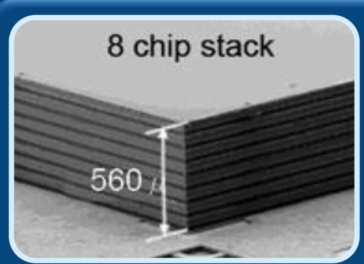
- TSV length
  - 50 to 100 µm
- TSV diameter
  - 10 to 50 µm



~ 2006 - ongoing

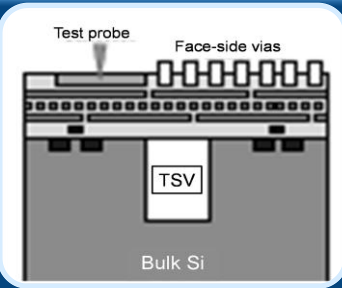
- TSV length
  - 10 to 20 µm
- TSV diameter
  - 1 to 5 µm

Spectrum of Challenges in 3-D ICs



Manufacturing

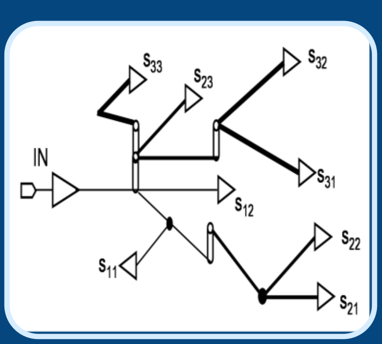
- Plane alignment and bonding
- Through silicon vias



Testing

- Pre-bond testing
- Post-bond testing
- Built-in-self-test

Design



- Interconnect design techniques
- Thermal management techniques
- Physical design techniques
- Routing
- Electrical and thermal characterization
- Floorplanning
- Heterogeneous system design
  - Memory on processor
  - MEMS/NEMS
  - RF/Analog/Mixed Signal
- EDA tool development
  - DRC, LVS, place & route

Presentation Outline

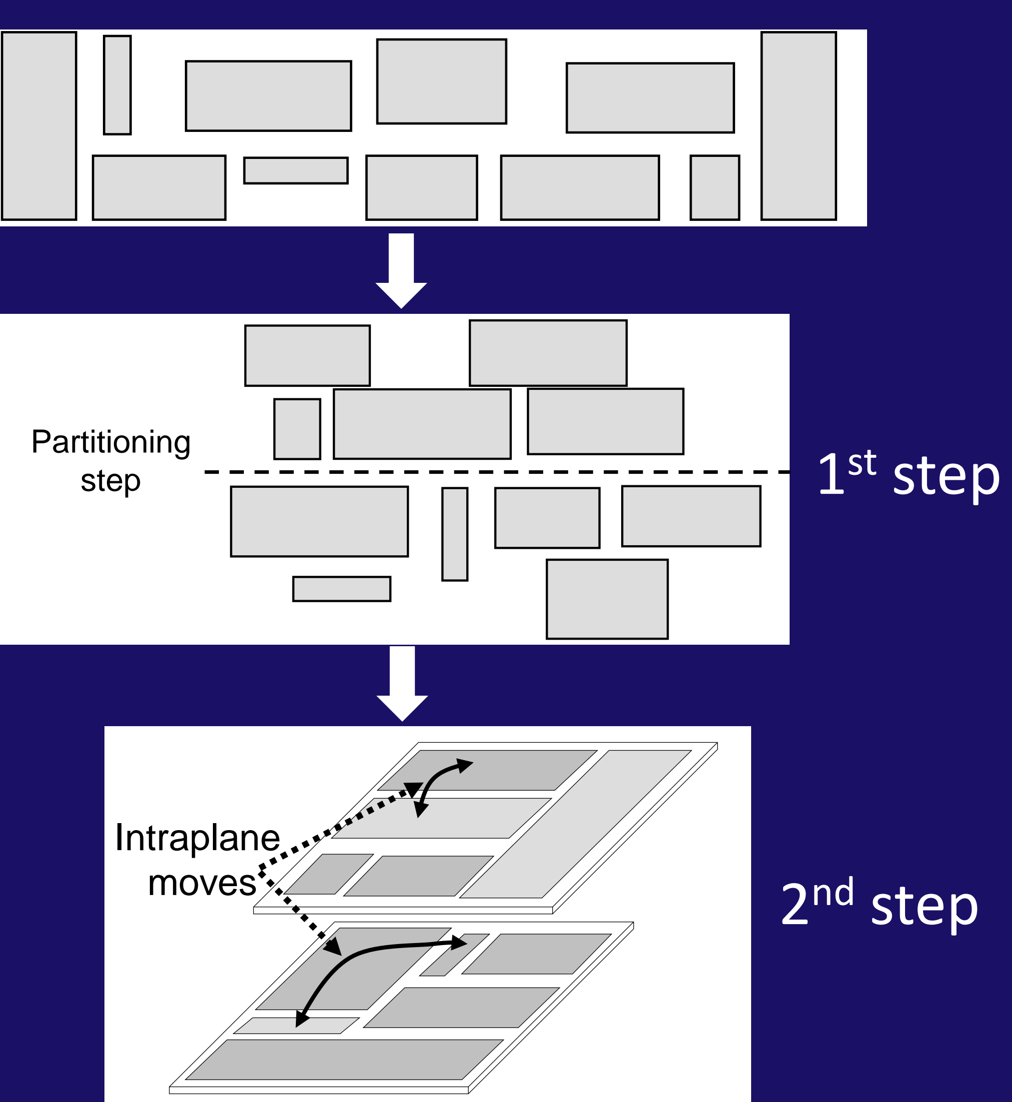
- Three-dimensional (3-D) integration
- ***Physical design techniques***
- TSV modeling
- Design methodologies and flow
- 3-D architectures
- Rochester test chips – past, present, and future
- Conclusions

Physical Design Techniques

- ***Floorplanning***
- TSV placement
- Placement techniques
- Routing techniques
- Thermal management

Floorplanning and Placement for 3-D ICs

- Third dimension greatly increases the solution space
- Adopt a two-step solution



*T. Yan, Q. Dong, Y. Takashima, and Y. Kajitani, "How Does Partitioning Matter for 3D Floorplanning," *Proceedings of the ACM International Great Lakes Symposium on VLSI,* pp. 73-76, April-May 2006

Floorplanning in 3-D

Address two important issues

Representation of 3rd dimension

Increase in solution space

With algorithms incorporating 3-D nature of circuits

3-D transition closure graph (TCG)

Sequence *k*-tuple

3-D slicing tree

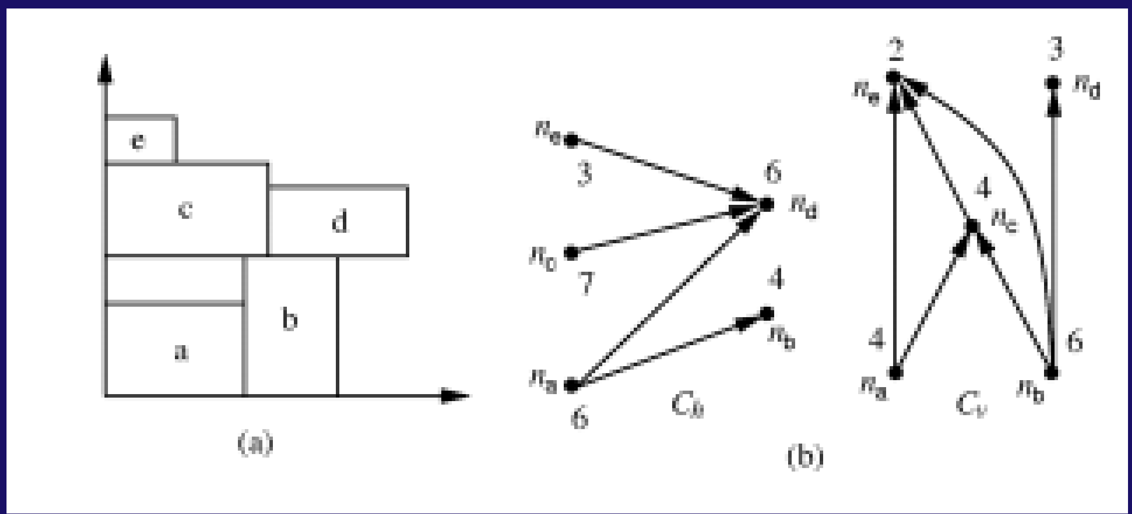
That optimize for circuit area by

Intraplane and interplane block swapping

Successively bisecting volume of 3-D system

Minimizing total wire length

3-D Transition Closure Graph (TCG)

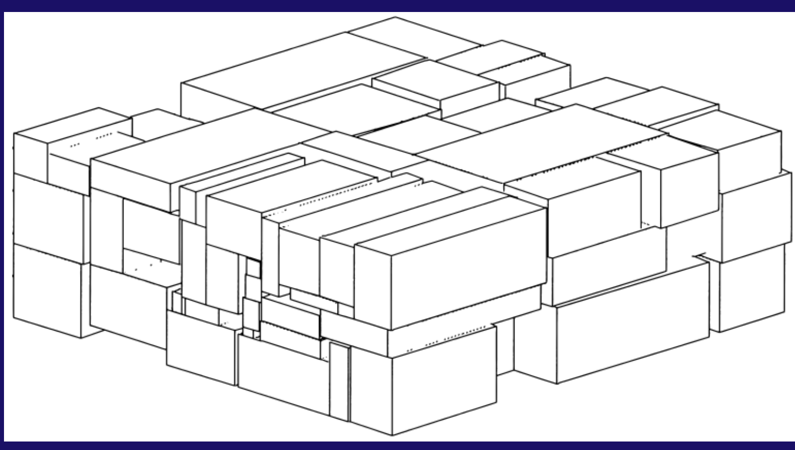


- Transitive closure graph-based representation for general floorplans
- No additional constraint graphs for cost evaluation
- Supports incremental update of boundary information, shapes, and relative positions
- Independent of physical location

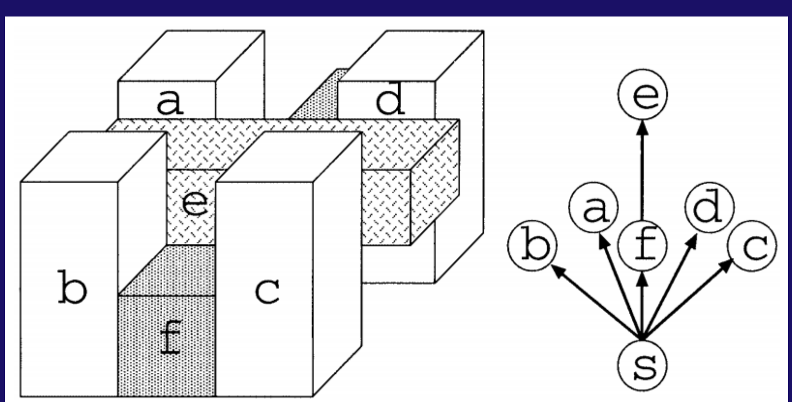
J.-M. Lin and Y.-W. Chang, "TCG: A Transitive Closure Graph-Based Representation for General Floorplans," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 13, No. 2, pp. 288-292, February 2005.

Sequence *k*-tuple

- Arrange rectangular boxes into a rectangular box of minimum volume
- Sequence-triple (three sequences of labels) encodes topology of 3-D packing
- Tractable 3-D packing with order of boxes sequentially extracted in fixed direction
- Can be extended from three sequences to five sequences



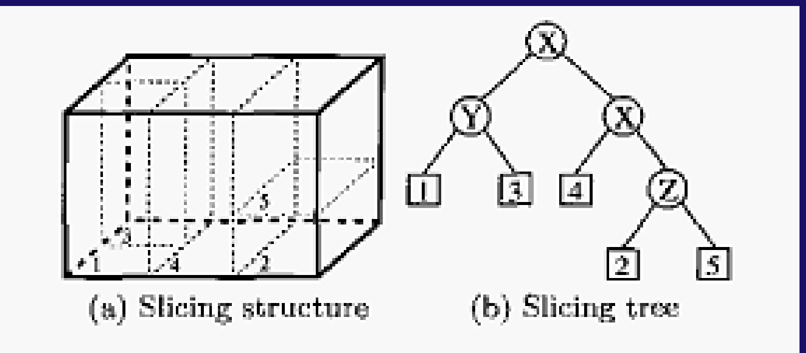
3-D packing of 100 boxes



H. Yamazaki, K. Sakanushi, S. Nakatake, and Y. Kajitani, "The 3D-Packing by Meta Data Structure and Packing Heuristics," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences,* Vol. E83-A, No. 4, pp. 639-645, April 2000.

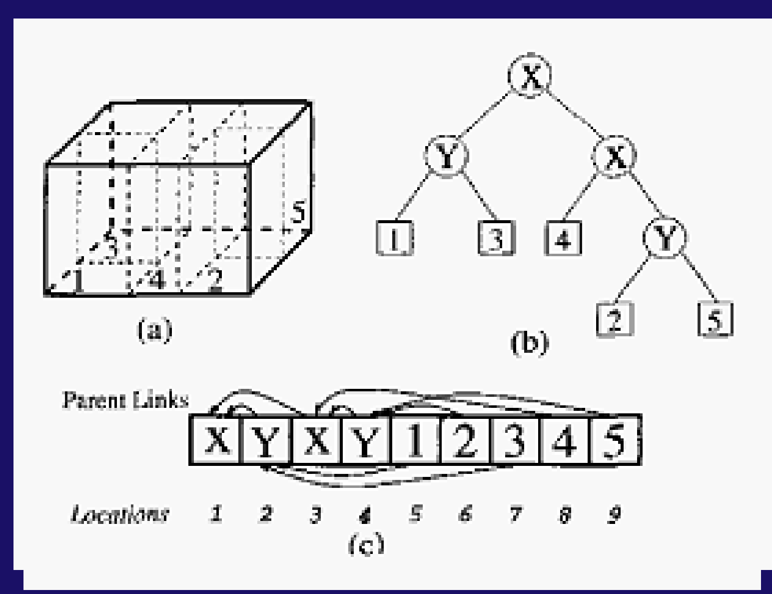
3-D Slicing Tree

- Slicing trees represent different floorplans
- Simulated annealing used to search good slicing floorplan
- Slicing tree is full binary tree
- If n basic modules, then
  - $2n - 1$ nodes
  - $n - 1$ internal nodes
- Neighborhood movements
  - Exchange: two subtrees in array
  - Rotation: in x, y, z directions



Exchange

Rotation



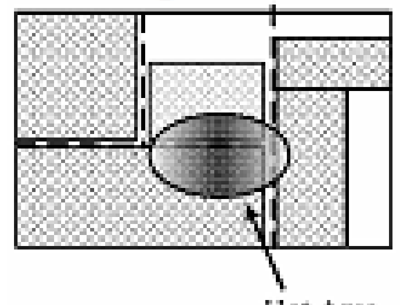
L. Cheng, L. Deng, and M. D.F. Wong, "Floorplanning for 3-D VLSI Design"
Proceedings of the 2005 Asia and South Pacific Design Automation Conference (ASP-DAC), Vol. 13, No. 2, pp. 405-411, January 2005.

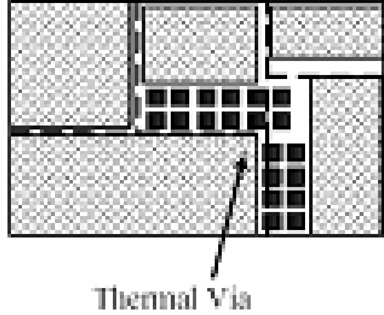
3D FP with T-Via Planning

- Inter-layer partitioning: determine desired temperature on each layer.
- Floorplanning using SA engine based on CBL representation
  - Cost function:

$$\Psi = A + w_1 W + w_2 (T_{max} - T_0)$$

  - Thermal resistances are updated after horizontal thermal via planning and the maximal temperature is calculated by solving linear equations.
- Thermal vias should be arranged in the white space between blocks.
  - White space resources may be not enough for thermal via insertion in hot area.

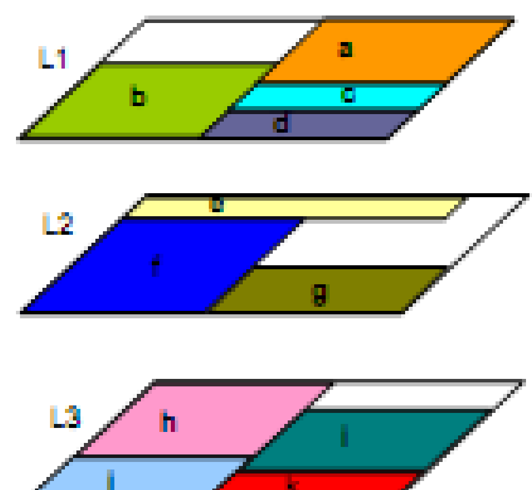




- A fast and simple white space redistribution method is proposed to deal with it during floorplanning process.

Z. Li, X. Hong, Q. Zhou, S. Zeng, J. Bian, H. Yang, V. Pitchumani, and C.-K. Cheng, "Integrating Dynamic Thermal Via Planning With 3D Floorplanning."

Thermal-Aware 3D Floorplanning [ICCAD04]



- First work in this field
- Simulated Annealing (SA) Engine
  - New local z-neighbor operations
  - Cost function

$$cost = \alpha \cdot nwl + \beta \cdot narea + \gamma \cdot nvc + \eta \cdot c_T$$

    - *nwl* — normalized wirelength
    - *narea* — normalized chip area
    - *nvc* — normalized interlayer via number
    - c_T — temperature cost

- Hybrid Thermal Evaluation
  - At each move — uses simplified chain model
  - At each SA temperature drop — the resistive network model

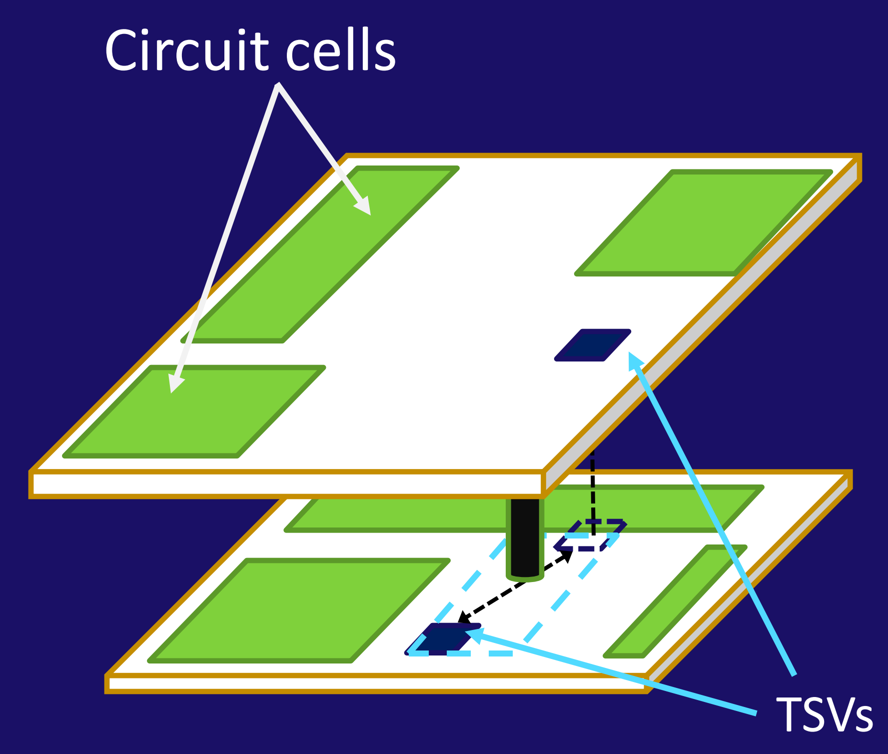
W.-L. Hung, G.M. Link, Y. Xie, N. Vijaykrishnan, and M. J. Irwin, "Interconnect and Thermal-aware Floorplanning for 3D Microprocessors," *Proceedings of the 7th International Symposium on Quality Electronic Design (ISQED '06)*, pp. 98-104, March 2006.

Physical Design Techniques

- Floorplanning
- ***<u>TSV placement</u>***
- Placement techniques
- Routing techniques
- Thermal management

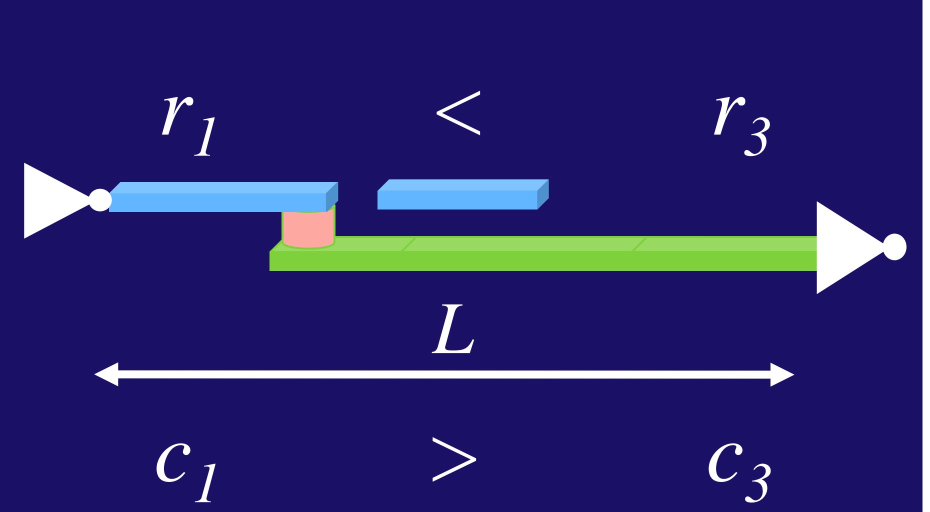
Through Silicon Via Placement

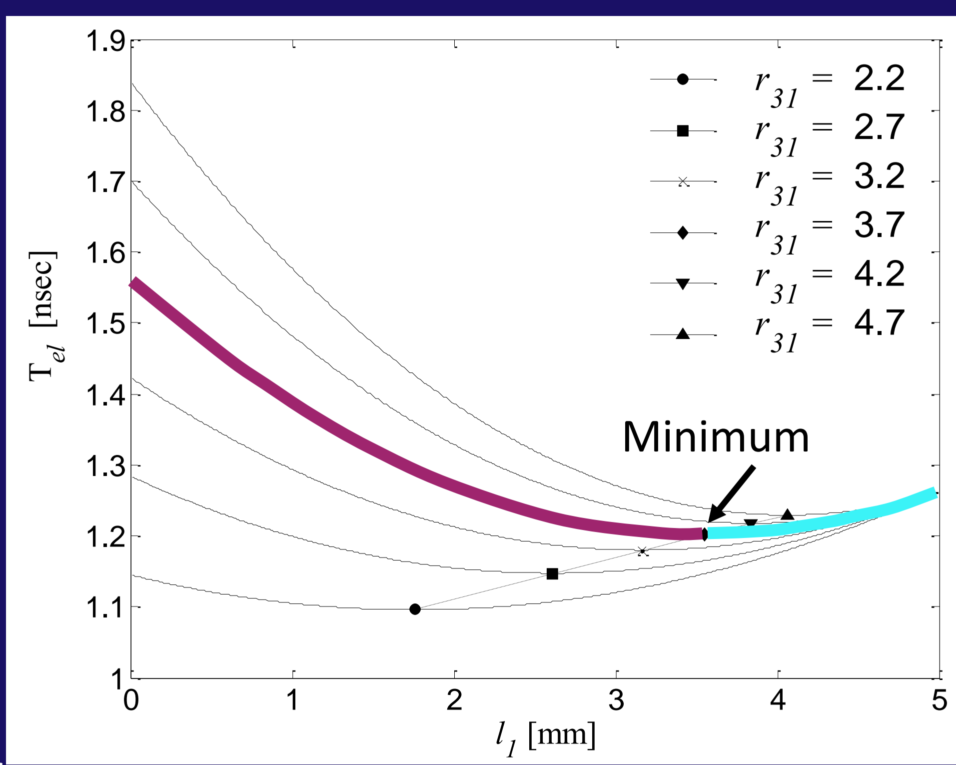
- Treat TSVs as circuit cells
  - Use weighted average distance to determine final via location
- Place the cells of each plane separately
  - Including vias



W. R. Davis *et al.,* "Demystifying 3D ICs: The Pros and Cons of Going Vertical," *IEEE Design and Test of Computers Magazine*, Vol. 22, No. 6 , pp. 498-510, November/December 2005

Delay Dependence on TSV Location



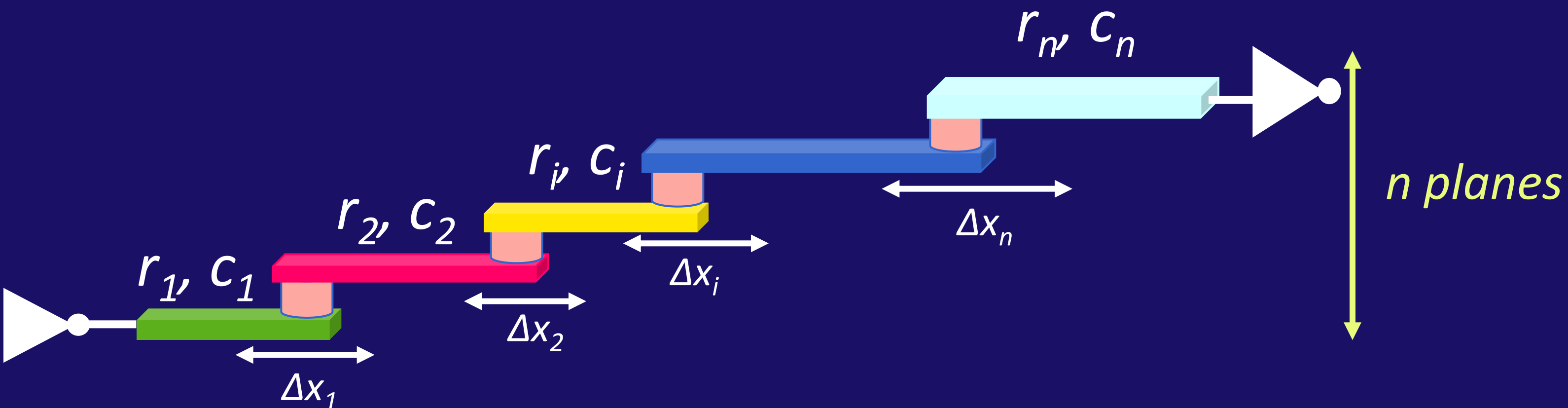


- Determine the via location that minimizes Elmore delay
  - Closed-form solution

- Interconnect parameters
  - r_1 = 76 Ω/mm
  - r_2 = 53 Ω/mm
  - c_2 = 223 fF/mm
  - c_3 = 279 fF/mm
  - c_{13} = 1.674
  - l_v = 20 μm
  - n = 2
  - R_S = 410 Ω
  - C_L = 180 fF

*V. F. Pavlidis and E. G. Friedman, "Interconnect Delay Minimization through Interlayer Via Placement," *Proceedings of the ACM Great Lakes Symposium on VLSI*, pp. 20-25, April 2005

Two-Terminal Nets, Multiple TSVs

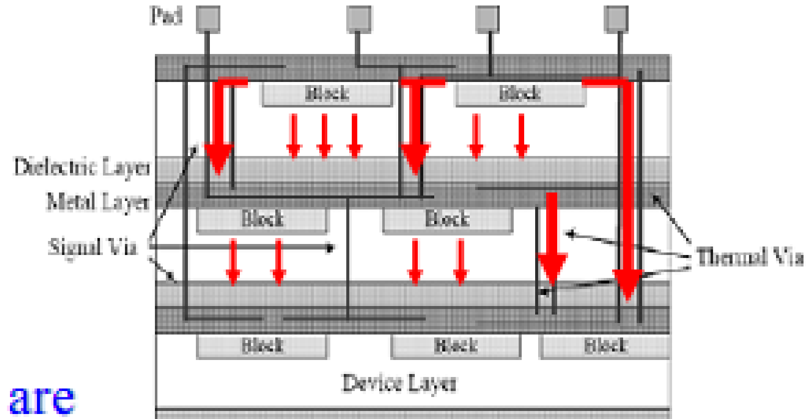


- Determine via location to minimize Elmore delay
  - Δx_i's: available region for via placement between the *i* and *i*+1 physical plane
  - Obstacles are considered
  - No closed form solution
  - $X_i^* = f(R_u, C_d)$
- Heuristic based approach
  - Solution primarily depends upon Δx_i's and not on the exact via locations

[*]V. F. Pavlidis and E. G. Friedman, "Timing Driven Via Placement Heuristics in 3-D ICs," *Integration, the VLSI Journal,* Vol. 41, No. 4, pp. 489 - 508, July 2008.

Thermal Via Planning

- Thermal Vias
  - Lowering the thermal resistance between different layers
  - Thermal resistance: $\frac{1}{R_e} = \frac{1}{R_{layer}} + \frac{1}{R_{via}}$

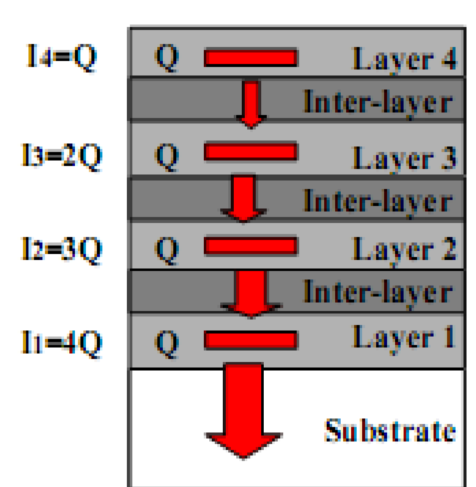


- T-Via number should be minimized and they are placed to hot areas to make the greatest impact.
- Heuristic Method for T-Via Planning
  - Thermal via number is in proportional to the heat flow inside that tile

$$n_j : n_k = I_j : I_k$$

  - Thermal via number in the figure is

$$n_4 : n_3 : n_2 = 1 : 2 : 3$$

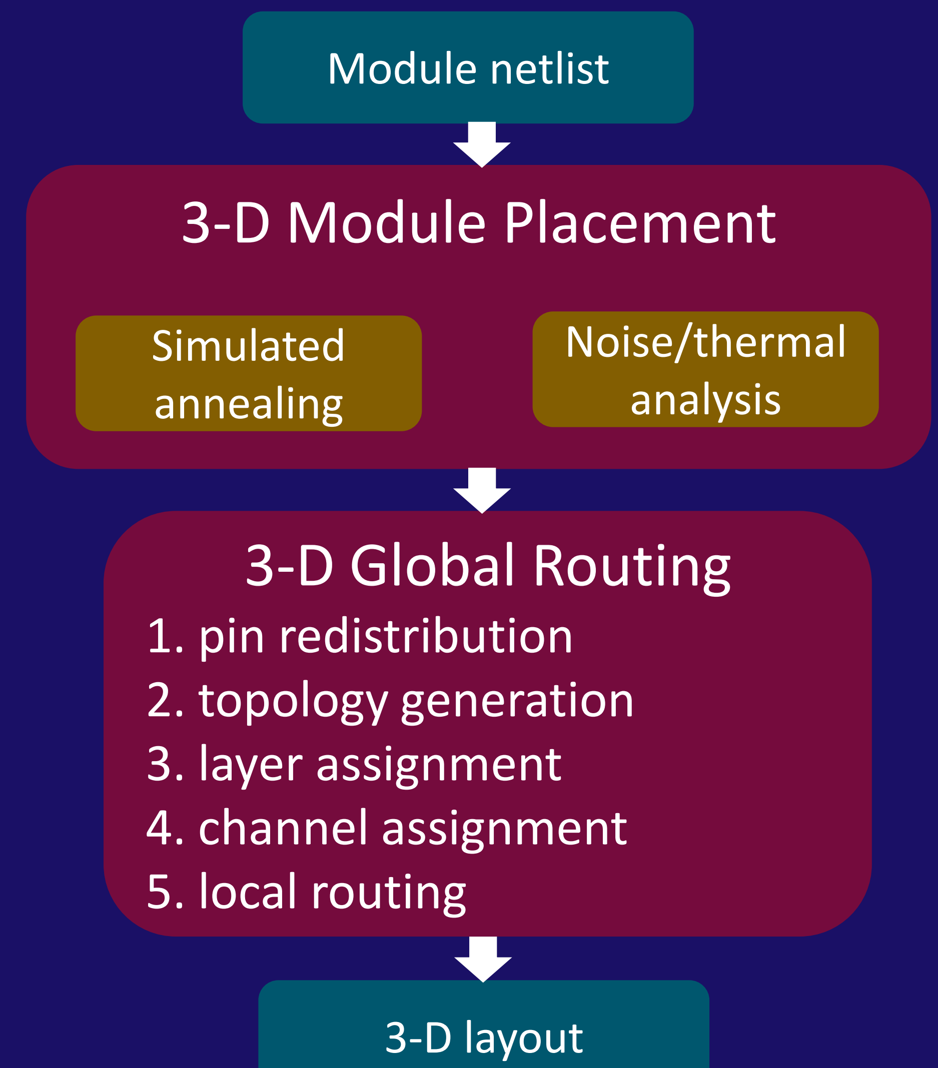


Z. Li, X. Hong, Q. Zhou, S. Zeng, J. Bian, H. Yang, V. Pitchumani, and C.-K. Cheng, “Integrating Dynamic Thermal Via Planning With 3D Floorplanning.”

Physical Design Techniques

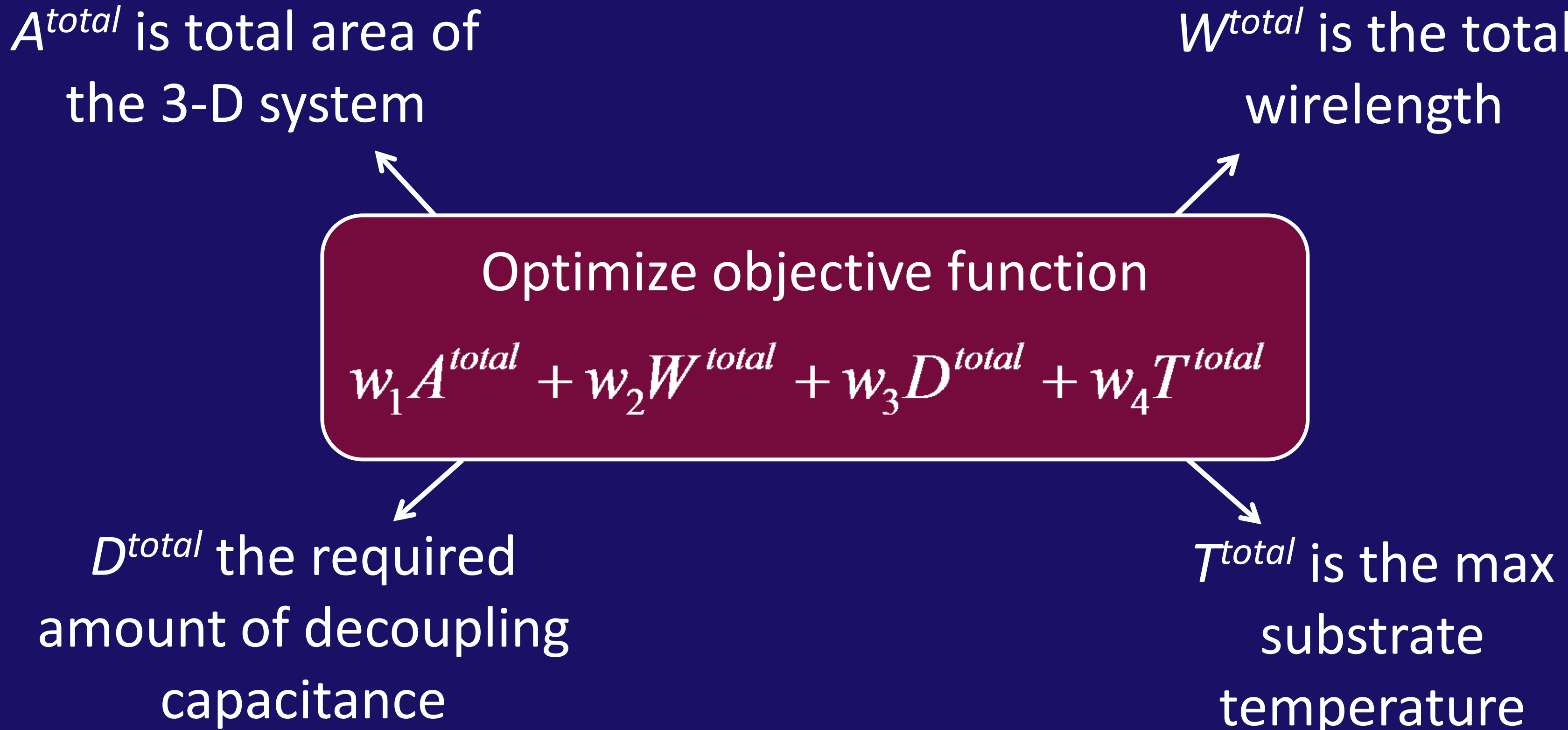
- Floorplanning
- TSV placement
- ***Placement techniques***
- Routing techniques
- Thermal management

Design Flow for 3-D Place and Route



J. Rajkumar, E. Wong, M. Pathak, and S. K. Lim, "Placement and Routing for 3-D System-On-Package Designs," *IEEE Transactions on Components and Packaging Technologies*, Vol. 29, No. 3, pp. 644 – 657, September 2006.

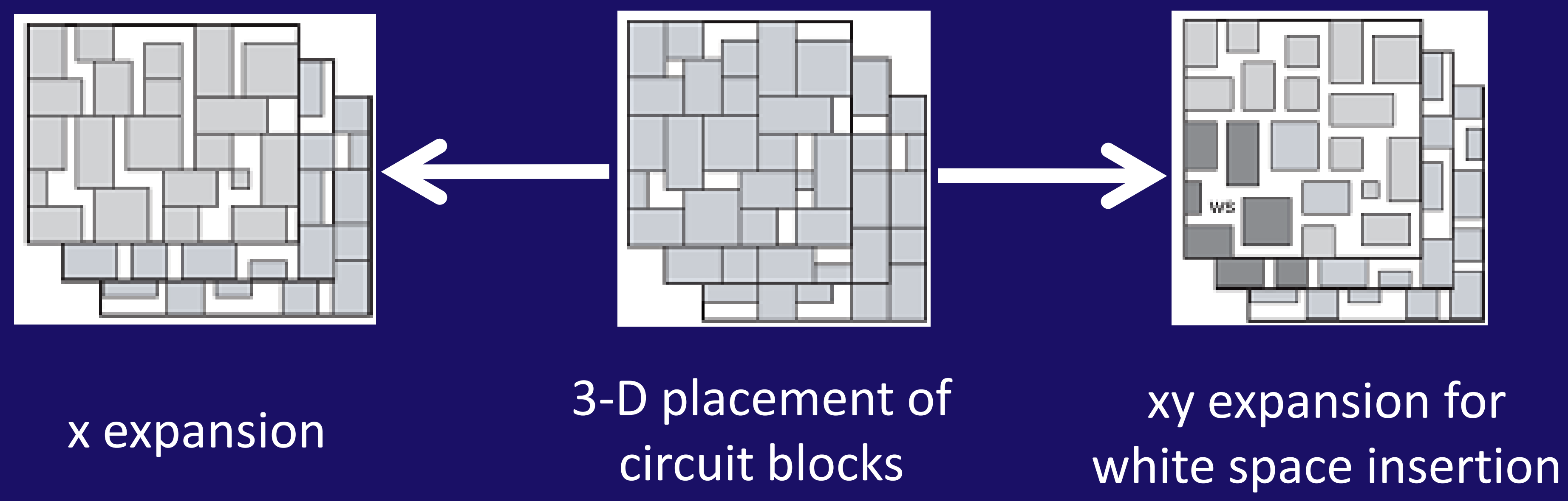
Multi-Objective Placement



w1, w2, w3, and w4 are user defined weights to control importance of each objective

E. Wong, J. Minz, and S. K. Lim, "Multi-Objective Module Placement For 3-D System-On-Package," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 14, No. 5, pp. 553 – 557, May 2006.

General Placement Flow

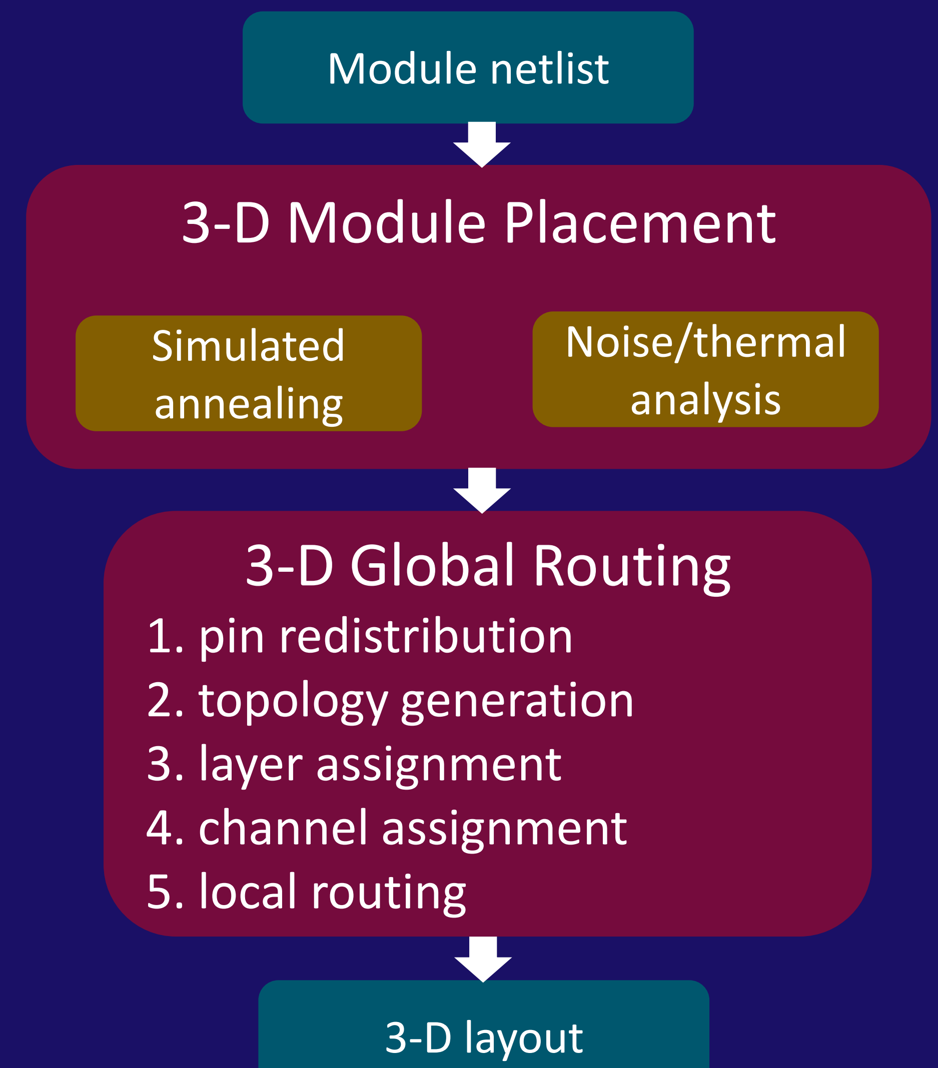


- Simulated annealing to optimize 3-D placement of blocks
- Expansion method depends on user objectives
  - Expand area (white space) to fit wiring, decaps, and thermal vias
  - Decaps (white space) may be shared between planes

Physical Design Techniques

- Floorplanning
- TSV placement
- Placement techniques
- ***Routing techniques***
- Thermal management

Design Flow for 3-D Place and Route



J. Rajkumar, E. Wong, M. Pathak, and S. K. Lim, "Placement and Routing for 3-D System-On-Package Designs," *IEEE Transactions on Components and Packaging Technologies*, Vol. 29, No. 3, pp. 644 – 657, September 2006.

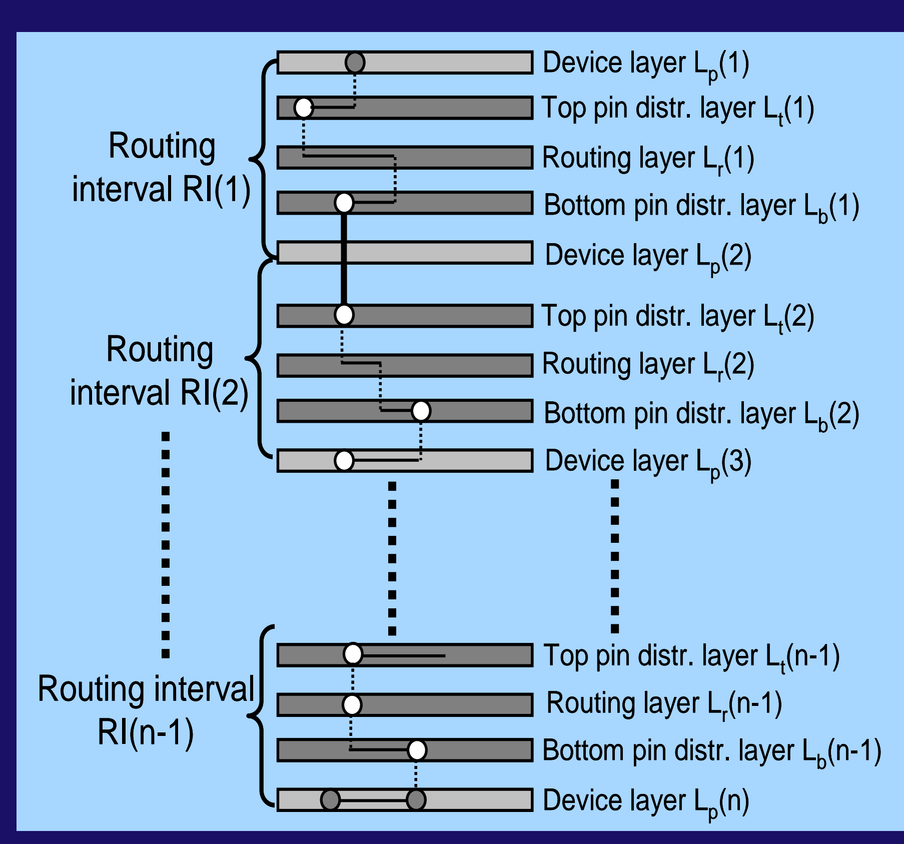
Multi-Objective Routing

- Multi-objective approach considers
  - Wirelength
  - Crosstalk
  - Congestion
  - Routing resources
- Wirelength described by total Manhattan distance in x, y, and z
- Crosstalk noise

$$xtn = \sum_{s \in NL, s \neq r} \frac{cl(r,s)}{|z(r) - z(s)|}$$

- Total number of layers to route SoP

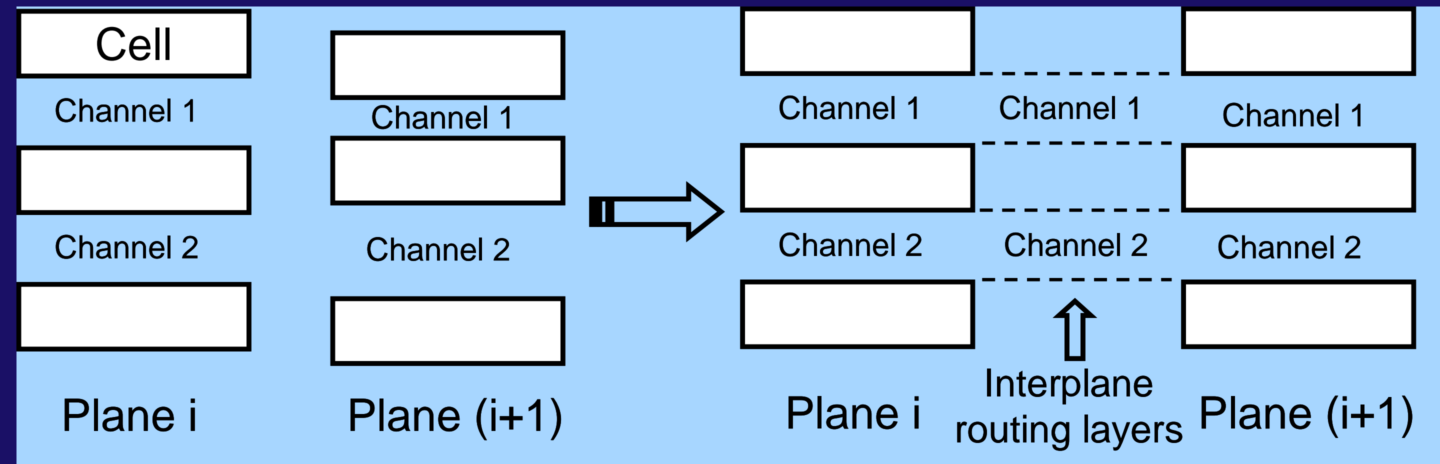
$$L^{tot} = \sum_{1 \leq i \leq n} \left(|L_i(i)| + |L_r(i)| + |L_b(i)| \right)$$



J. Minz and S. K. Lim, "Block-Level 3-D Global Routing With an Application to 3-D Packaging," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 10, pp. 2248 – 2257, October 2006.

3-D Channel Routing Task

- Convert interplane interconnect into 2-D channel routing task
- Interplane routing implemented in five major stages
  - Interplane channel definition
  - Pseudo-terminal allocation
  - Interplane channel creation
  - Detailed routing
  - Channel alignment
- Additional stages to route 2-D channels: interplane and intraplane
  - Channel ordering determines wire routing order



C. C. Tong and C.-L. Wu, “Routing in a Three-Dimensional Chip,”
IEEE Transactions on Computers, Vol. 44, No. 1, pp. 106 – 117, January 1995.

3-D Pin Distribution

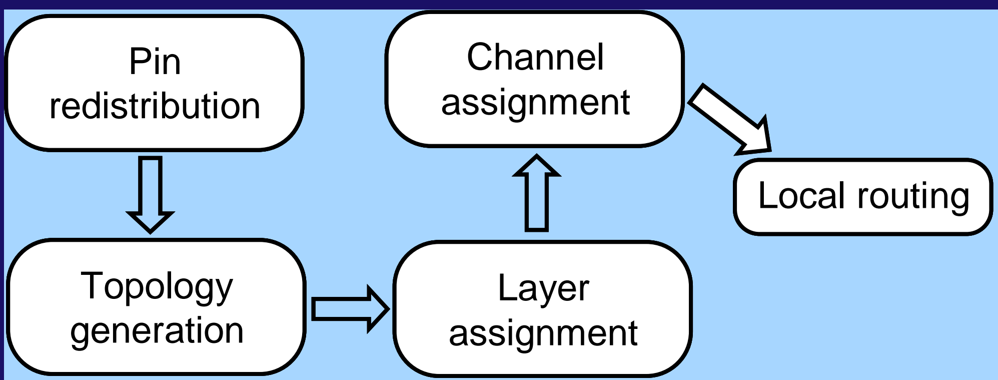
- Minimize objective function for global route

$$\alpha L^{tot} + \beta D^{\max} + \sum_{r \in NL} (\gamma xt_r + \delta wl_r + \varepsilon via_r)$$

- Based on global route
  - Distribute pins to each circuit block

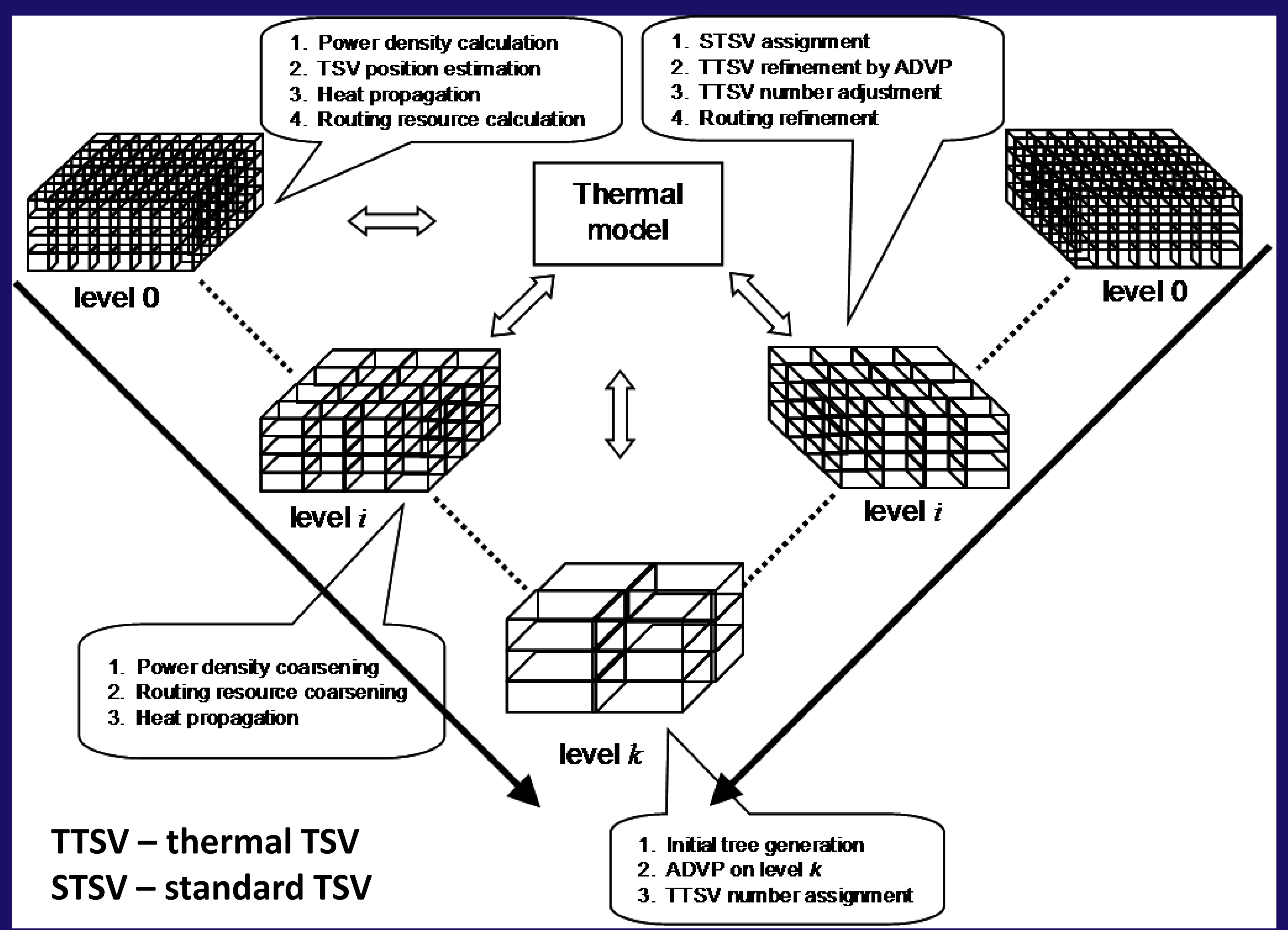
- Coarse pin distribution
  - $O(p \cdot u \cdot v)$

- Detailed pin Distribution
  - $O(p^2 \cdot \log p)$



J. Minz and S. K. Lim, "Block-Level 3-D Global Routing With an Application to 3-D Packaging," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 10, pp. 2248 – 2257, October 2006.

Routing with Thermal Via Planning

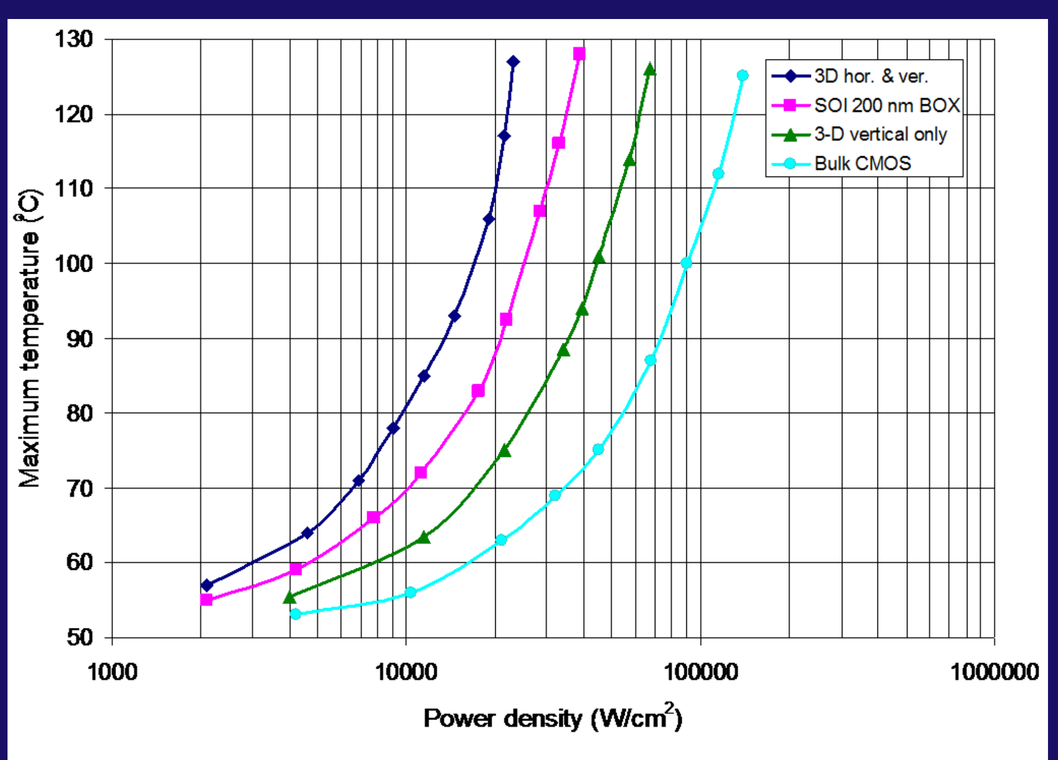


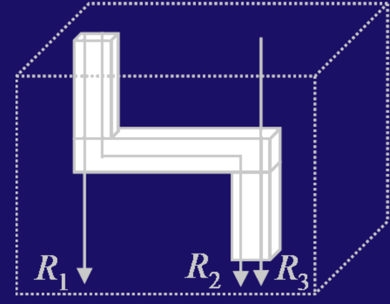
J. Cong and Y. Zhang, "Thermal Via Planning for 3-D ICs," *Proceedings of the IEEE/ACM International Conference on Computer Aided Design*, pp. 744 – 751, November 2005.

Physical Design Techniques

- Floorplanning
- TSV placement
- Placement techniques
- Routing techniques
- ***Thermal management***

Thermal Analysis of 3-D ICs





- Maximum temperature vs. power density for 3-D ICs, SOI, and bulk CMOS
- 3-D horizontal and vertical includes thermal paths with horizontal interconnect segment
- 3-D vertical only includes interplane vias in thermal path

C. C. Liu, J. Zhang, A. K. Datta, and S. Tiwari, "Heating Effects of Clock Drivers in Bulk, SOI, and 3-D CMOS," *IEEE Transactions on Electron Device Letters*, Vol. 23, No. 12, pp. 716 – 728, December 2002.

3D Performance Dependence on Stack Order

Scenario 1 – Core on Top

Composite = 1.004X Delay

Scenario 2 – Core on Bottom

Composite = 1.0076X Delay

- For Microprocessor / Memory 3D Subsystem applications - place microprocessor closest to heatsink (i.e. Scenario 1)

J. Li, "3D Integration-Opportunities and Challenges,"
International Symposium on Computer Architecture (ISCA '08), June 2008.

© 2008 IBM Corporation

Temperature Distribution and Power

Operating voltage as low as 0.6V will reduce chip temperature to about 70C

© 2008 IBM Corporation

Thermal Through Silicon Vias (TTSV)

STACKED DIES
SIGNAL LAYERS
INTERLAYER DIELECTRIC (ILD)
THERMAL THROUGH SILICON VIAS (TTSV)
C4 BUMPS
INTEGRATED HEAT SPREADER (IHS)
ENCAPSULATION
DIE-TO-DIE VIAS
THROUGH SILICON VIAS (TSV)
UNDERFILL

Need dedicated Thermal Through Silicon Vias

Large in size: ~100 microns diameter; ~200 microns deep

Filled with copper to provide adequate thermal paths

J. Bautista, “Tera-scale Computing and Interconnect Challenges – 3D Stacking Considerations,” *International Symposium on Computer Architecture (ISCA ‘08)*, June 2008.

Cooling 3D chips with H_2O

fluid containment top

IC 3

IC 2

IC 1

fluid containment bottom

C4

Solder functionality

sealing

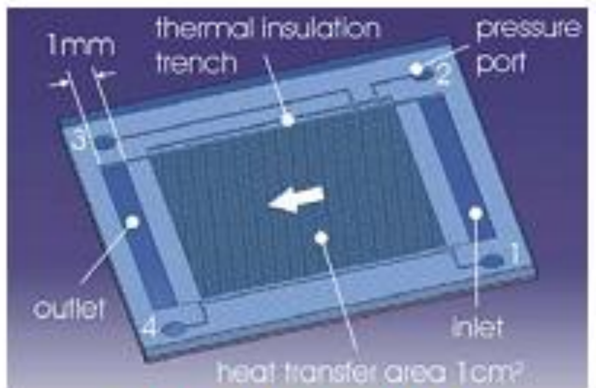
electrical

Thermo-mechanical

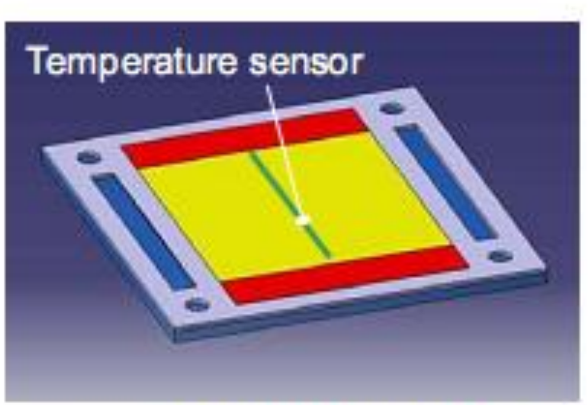
Through silicon via with bonding scheme

The complexity of such a system resembles that of a human brain, wherein millions of nerves and neurons for signal transmissions are intermixed but do not interfere with tens of thousands of blood vessels for cooling and energy supply, all within the same volume.

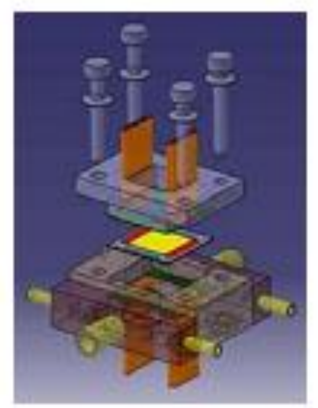
Brunschwiler, et al. IEEE ITherm'08



Test vehicle fluid structure



Test vehicle bottom with heater



Test setup

© 2008 IBM Corporation

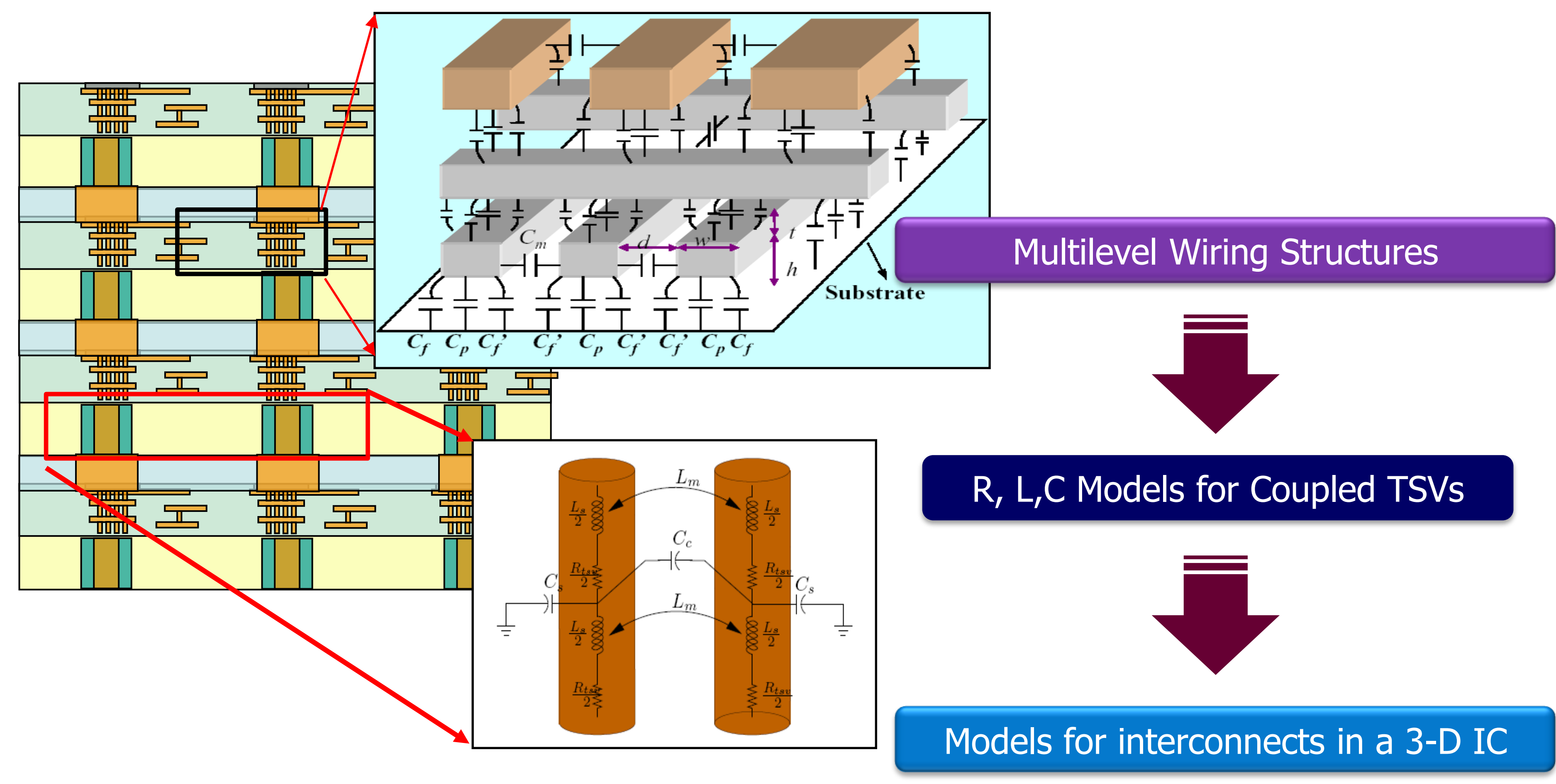
Presentation Outline

- Three-dimensional (3-D) integration
- Physical design techniques
- ***TSV modeling***
- Design methodologies and flow
- 3-D architectures
- Rochester test chips – past, present, and future
- Conclusions

TSV Modeling

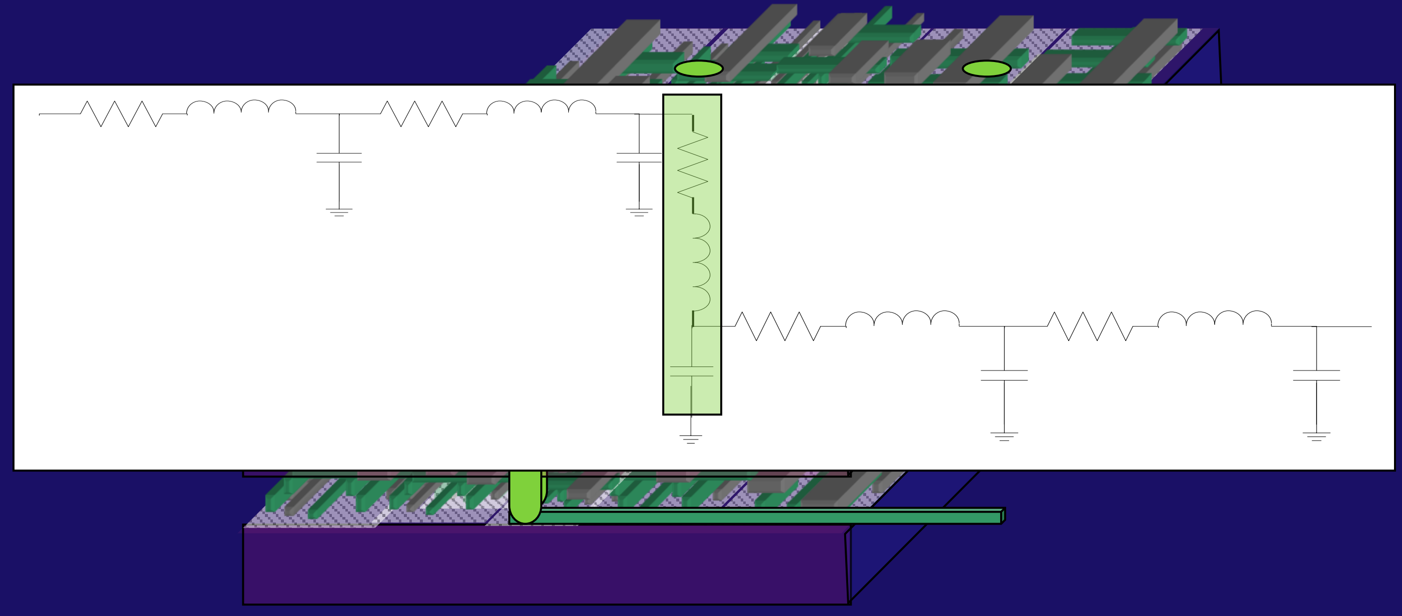
- ***Electrical modeling of 3-D via***
- Electrical modeling of bundled 3-D vias
- Thermal modeling of 3-D via
- Effect of 3-D via placement on transistor properties

Interconnects in 3-D ICs



R. Weerasekera, *System Interconnection Design Trade-offs in Three-Dimensional Integrated Circuits*, Ph.D. Thesis, KTH School of Information and Communication Technologies, Sweden, December 2008.

3-D TSV Impedance Modeling

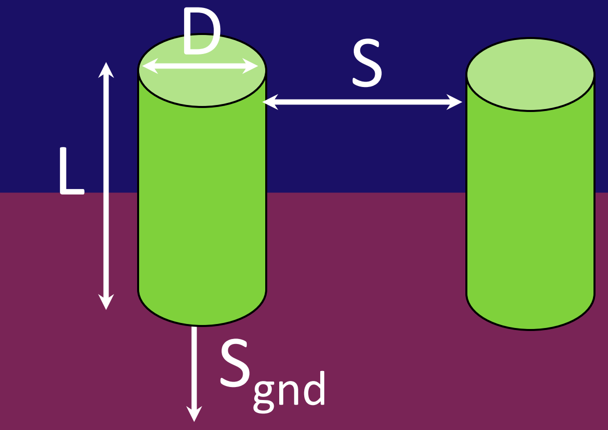


- TSV impedance impacts
  - Signal integrity
  - Propagation delay
  - Power network design
  - Interface design

Accurate TSV impedance models are necessary

I. Savidis and E. G. Friedman, “Electrical Characterization and Modeling of 3-D Vias,” *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 784 – 787, May 2008.

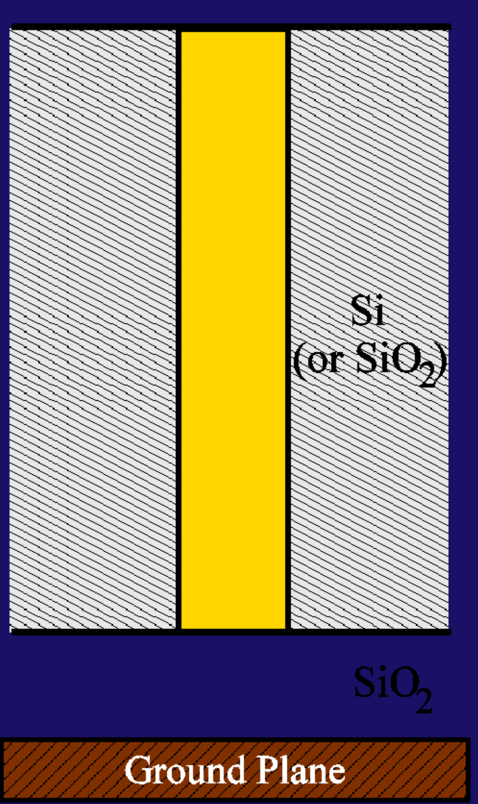
3-D TSV Physical Parameters



- Equations modeling TSV electrical characteristics account for
  - TSV diameter *D* and length *L*
    - Aspect ratio ranges from 0.5 to 9
  - TSV distance from ground plane S_{gnd}
  - Spacing *S* to neighboring TSVs for:
    - Capacitive coupling
    - Determining loop inductance

3-D Via Models

- SOI and bulk vias
- Model vias as cylinders
  - Diameter
  - Length
  - Dielectric liner thickness (bulk)
  - Via pitch
  - Distance to ground



3-D Via Resistance Models

- DC resistance

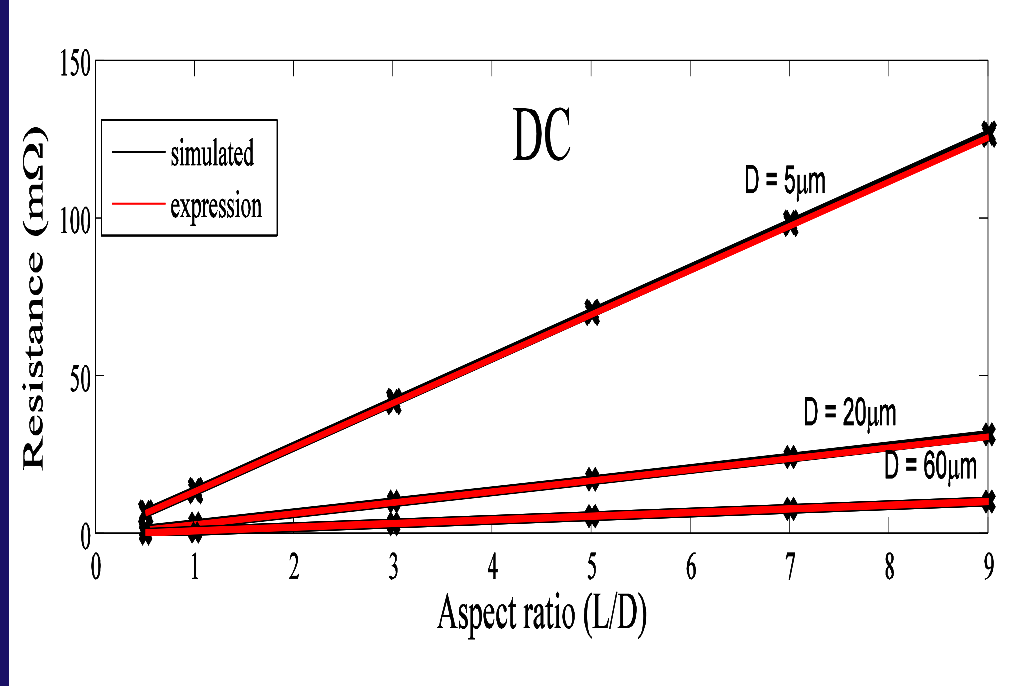
$$r_{DC} = \frac{1}{\sigma_W} \cdot \frac{L}{\pi R^2}$$

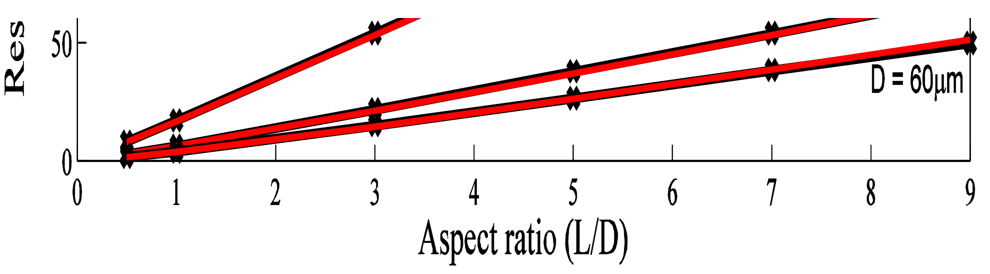
- 1 GHz resistance

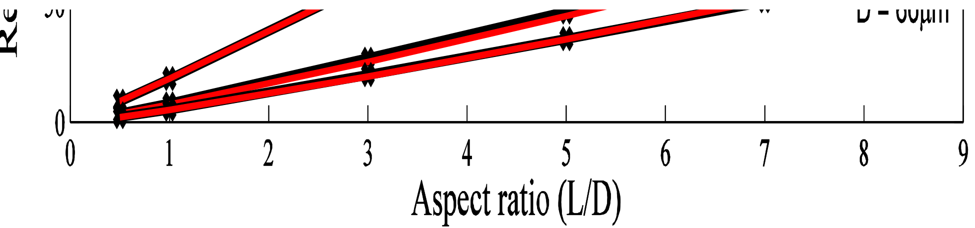
$$r_{1GHz} = \begin{cases} \alpha \cdot \frac{1}{\sigma_W} \frac{L}{\pi[R^2 - (R-\delta)^2]}, & if\, \delta < R \\ \alpha \cdot \frac{1}{\sigma_W} \frac{L}{\pi R^2}, & if\, \delta \geq R \end{cases}$$

- Resistance at different *f*

$$r_{f_{new}} = (r_{1GHz} - r_{DC})\sqrt{\frac{f_{new}}{f_{1GHz}}} + r_{DC}$$





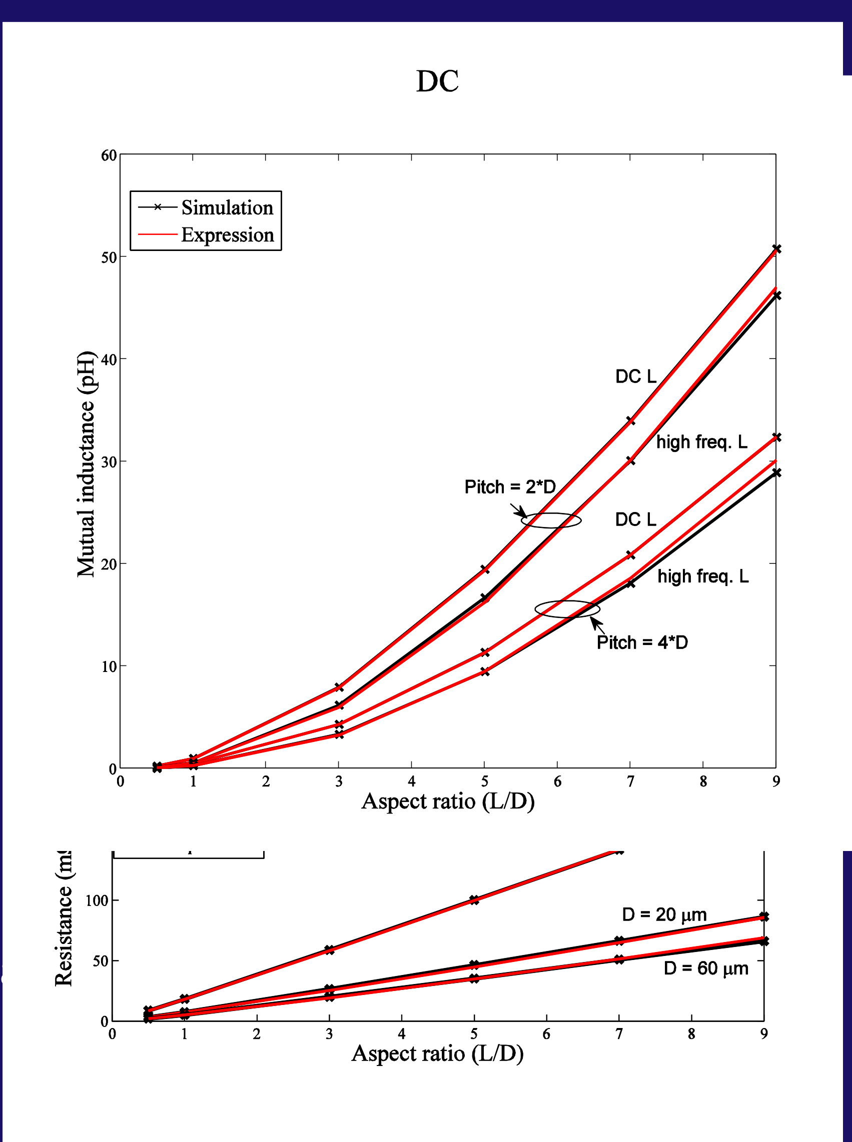


Maximum Error of 3-D Modeling Equations

- DC Resistance: < 2%
- 1 GHz Resistance: < 4.5%
- 2 GHz Resistance: < 5.5%

- Self Inductance L_{11}: ≤ 8%
- Mutual Inductance L_{21}: ≤ 8%*

- Capacitance to ground: ≤ 8%
- Coupling Capacitance: ≤ 15%*

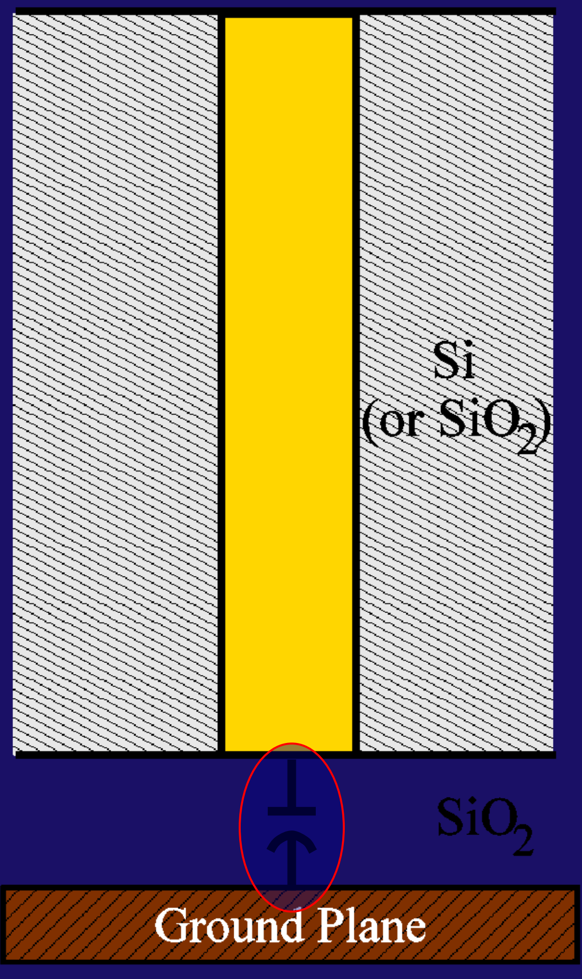


* Error in mutual inductance and coupling capacit ratios and for vias that are farther apart as both values

I. Savidis and E. G. Friedman, "Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices*, Vol. 56, No. 9, pp. 1873 – 1881, September 2009.

3-D Via Capacitance Model

Simulation
Expression
D = 60µm
D = 40µm
D = 20µm
Capacitance (fF)
Aspect ratio (L/D)

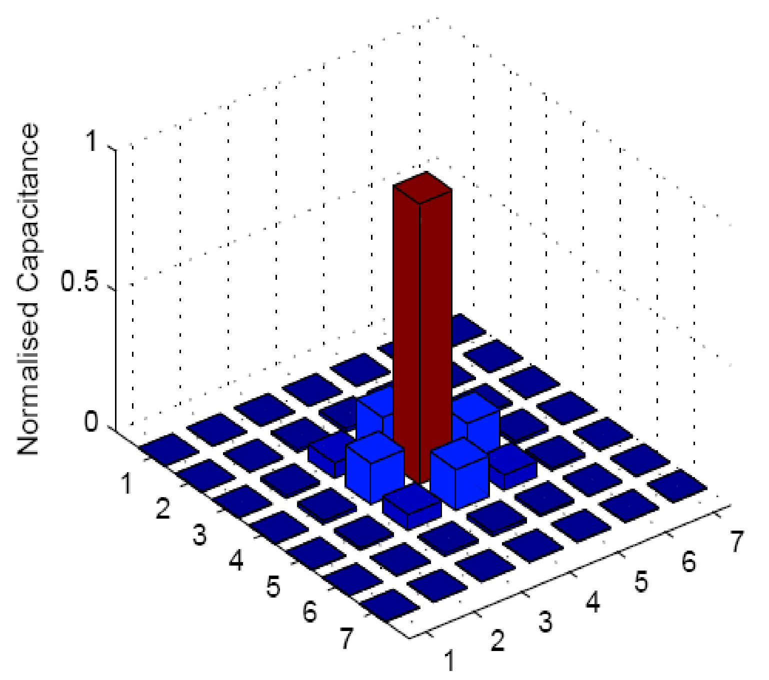


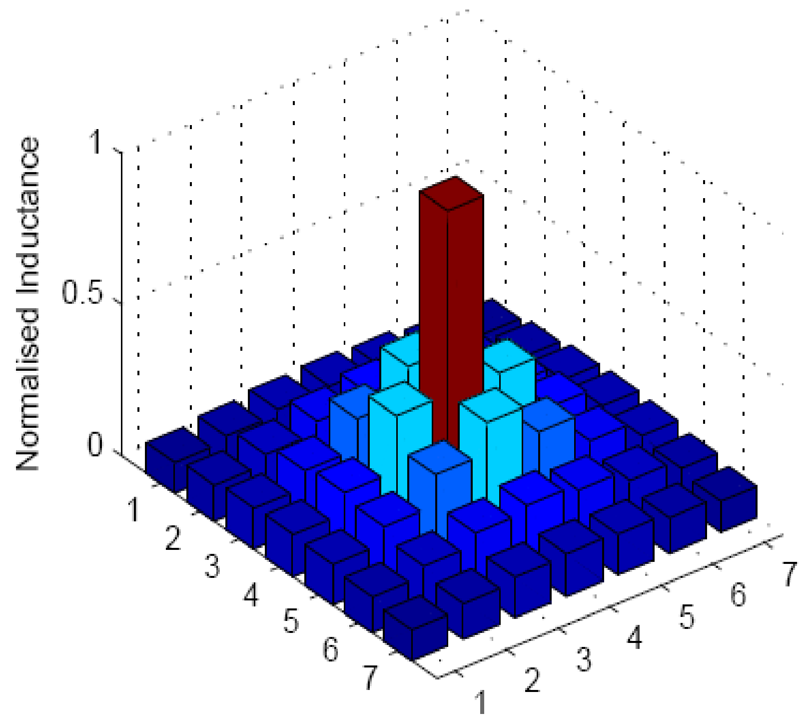
I. Savidis and E. G. Friedman, "Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices*, Vol. 56, No. 9, pp. 1873 – 1881, September 2009.

TSV Modeling

- Electrical modeling of 3-D via
- ***Electrical modeling of bundled 3-D vias***
- Thermal modeling of 3-D via
- Effect of 3-D via placement on transistor properties

Nature of Coupling in a TSV Bundle





- The capacitive coupling terms to nearest neighbors dominate
- Coupling terms to nonadjacent lines are mostly insignificant
- Within nearest neighbors the lateral terms are more significant than the diagonal terms.

- Inductive coupling is significant within the entire bundle

R. Weerasekera, *System Interconnection Design Trade-offs in Three-Dimensional Integrated Circuits*, Ph.D. Thesis, KTH School of Information and Communication Technologies, Sweden, December 2008.

TSV Parasitic Models

Capacitance

Self-Capacitance model is of the form:

$$C_s = C_{tsv}\left\{1 - k_1 e^{\left(k_2 \frac{p_v}{r_v} + k_3 \frac{p_v}{l_v}\right)}\left[k_4\left(\frac{l_v}{r_v}\right)^{k_5} + k_6\left(\frac{p_v}{r_v}\right)^{k_7} + k_8\right]\right\}$$

where Ctsv is the capacitance of an isolated TSV

$$C_{tsv} = \frac{63.34\varepsilon l_v}{\log\left(1 + 5.26\frac{l_v}{r_v}\right)}$$

Coupling-Capacitance model is of the form:

$$C_c = \frac{k_1 \varepsilon_0 l_v}{\ln\left(k_2 \frac{p_v}{r_v}\right)}\left[1 + k_3\left(\frac{p_v}{r_v}\right)^{k_4} + k_5\left(\frac{l_v}{r_v}\right)^{k_6} + k_7\left(\frac{p_v}{l_v}\right)^{k_8}\right]$$

Inductance

Self-Inductance model is of the form:

$$L_s = 0.16\mu l_v \ln\left(1 + 0.9\frac{l_v}{r_v}\right)$$

Mutual-Inductance model is of the form:

$$L_m = 0.199\mu l_v \ln\left(1 + 0.438\frac{lv}{d_v}\right)$$

	k_1	k_2	k_3	k_4	k_5	k_6	k_7	k_8	Max. % Error	Average % Error
C_{s_M}	0.1505	-0.0071	-0.091	0.1849	-1.9371	6.9577	-0.0131	-0.0354	48.0	7.8
C_{s_N}	0.6876	-0.0390	-0.0583	1.8076	-0.2229	11.3537	0.0402	-13.1813	10.2	1.9
C_{s_NE}	0.3406	-0.0345	-0.0686	5.0708	-0.1530	-5.6346	-0.3859	-0.7643	13.3	2.0
C_{c_l}	10.191	0.5490	-0.014	0.796	0.054	-1.157	-0.018	-0.600	8.7	1.9
C_{c_p}	3.180	0.5440	-0.199	0.586	0.122	0.540	2.176	0.110	10.9	1.8
C_{c_d}	18.117	28.457	-1.734	-2.178	0.600	-0.518	-0.470	0.188	8.0	1.4

R. Weerasekera, *System Interconnection Design Trade-offs in Three-Dimensional Integrated Circuits*, Ph.D. Thesis, KTH School of Information and Communication Technologies, Sweden, December 2008.

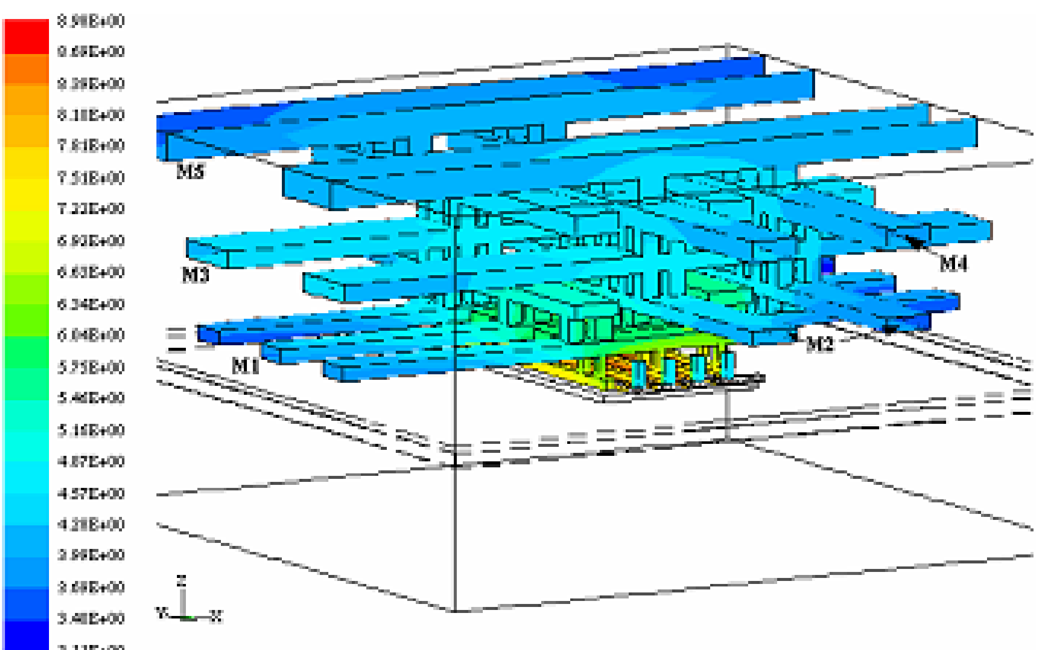
TSV Modeling

- Electrical modeling of 3-D via
- Electrical modeling of bundled 3-D vias
- ***Thermal modeling of 3-D via***
- Effect of 3-D via placement on transistor properties

Thermal Modeling Challenges of 3D Structures

Wiring stacks are incredibly complex

- 11 metal levels with total thickness of order 8 μm
- Highly variable amount of metal interconnection through the stack
- Mix of dielectric layers including low-k and ultra-low-k; future may include air-gap technologies
- Dielectrics with poorly known and anisotropic thermal conductivities



© 2008 IBM Corporation

Closed-Form Temperature Expressions

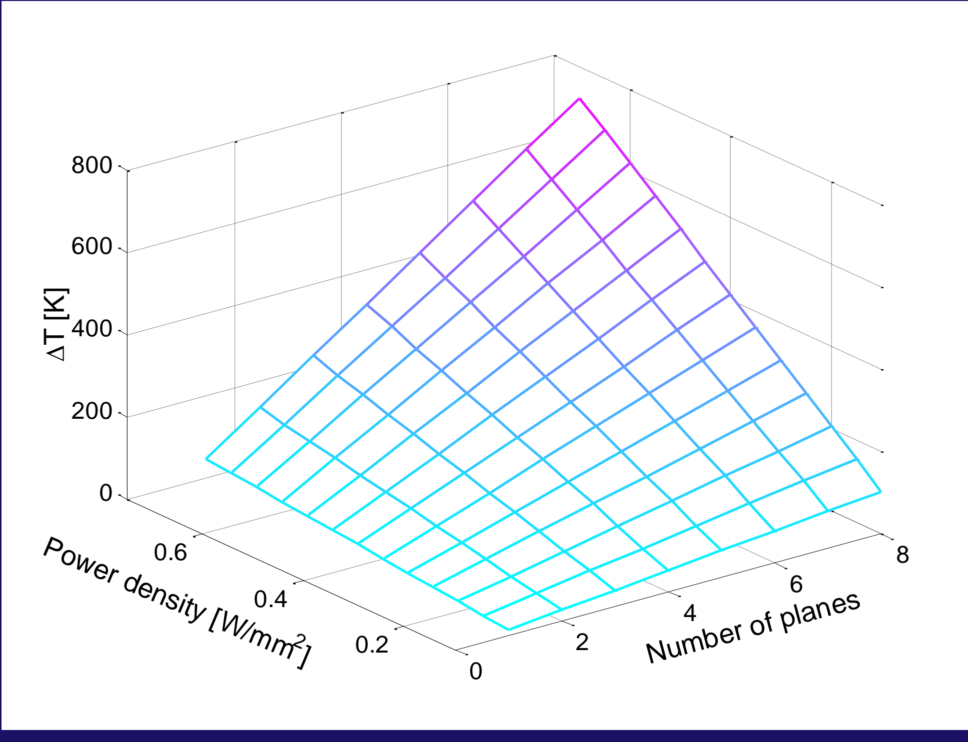
- Steady state thermal equation

$$\nabla(k\nabla T) = -Q$$

- 2-D ΔT equation based on one-dimensional heat flow

$$\Delta T = R_{th}\frac{P}{A}$$

  - P/A is power density
  - R_{th} is thermal resistance



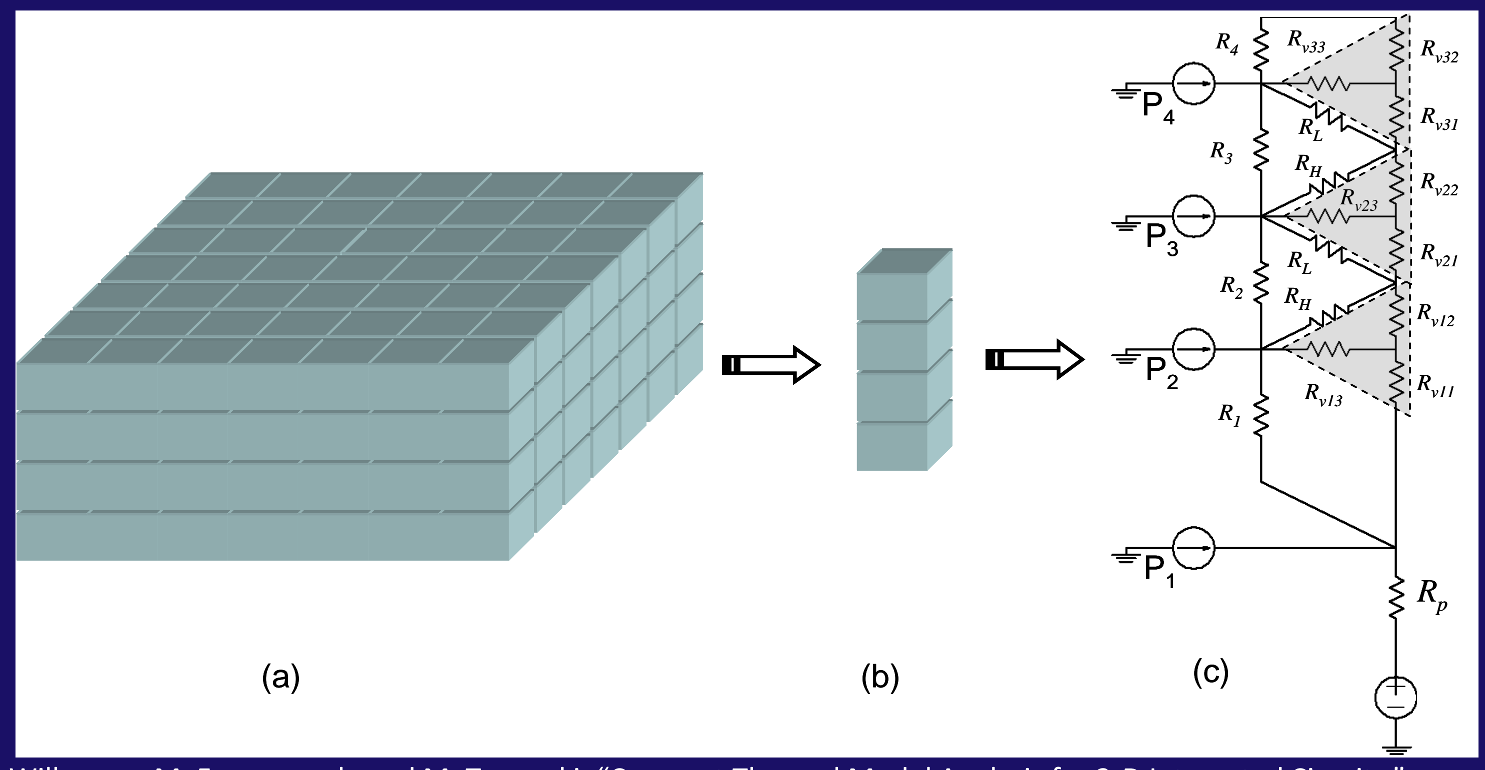
- 3-D ΔT equation: P_k = power consumption plane k, R_k = thermal resistance of plane k

$$\Delta T_j = \sum_{i=1}^{j}\left[R_i\left(\sum_{k=i}^{n}\frac{P_k}{A}\right)\right] \qquad \Delta T_n = \left(\frac{P}{A}\right)\left[\frac{R}{2}n^2 + \left(R_{ps} - \frac{R}{2}\right)n\right]$$

M. B. Kleiner, S. A. Kuhn, P. Ramn, and W. Weber, "Thermal Analysis of Vertically Integrated Circuits," *Proceedings of the IEEE International Electron Devices Meeting,* pp. 487 – 490, December 1995.

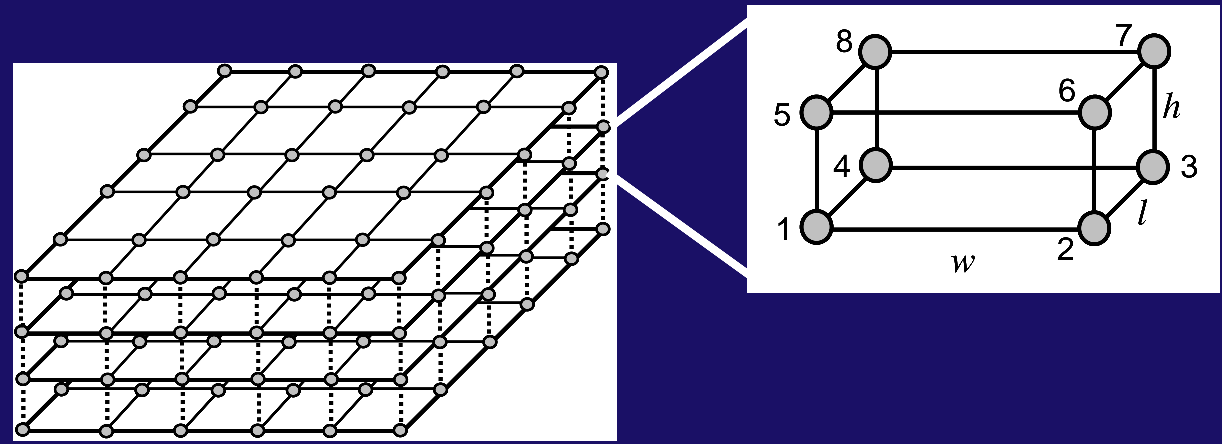
Compact Thermal Models

- Temperature and heat variation across and between planes
- Temperature and power density vectors depend on all three directions
- 3-D system modeled as thermal resistive stack
- Each pillar successively modeled by 1-D thermal network
  - Thermal resistors
  - Heat sources: all heat generated by all devices contained in each tile



P. Wilkerson, M. Furmanczyk, and M. Turowski, "Compact Thermal Model Analysis for 3-D Integrated Circuits," *Proceedings of the International Conference on Mixed Design of Integrated Circuits and Systems*, pp. 277 – 282, June 2004.

Mesh-Based Thermal Models



- Applied to complex geometries without boundary conditions
- Solve differential equation by finite element method (FEM), finite difference method, boundary element method

$$k\nabla^2 T = -Q$$

- Temperature of parallelepiped (node)

$$T(x,y,z) = Nt = \sum_{i=1}^{8} N_i t_i$$

N_i -> shape function

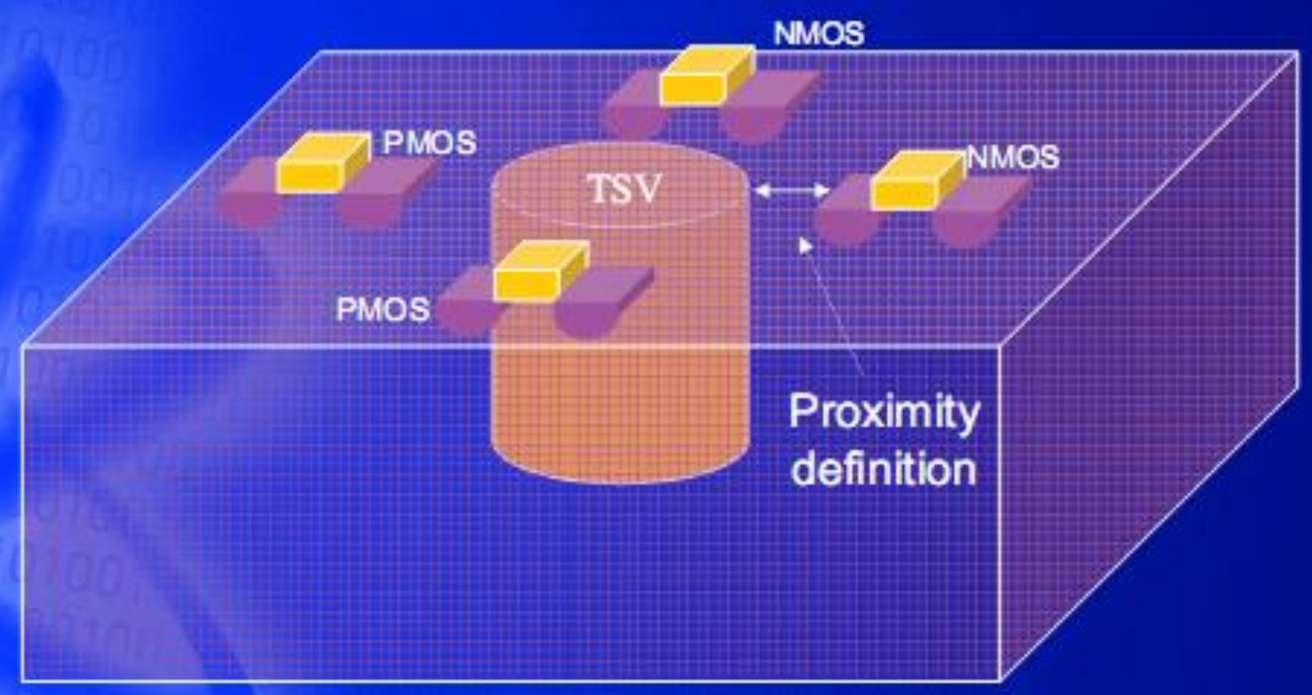
t_i -> temperature

- No fixed resistances = greater accuracy than compact thermal models

TSV Modeling

- Electrical modeling of 3-D via
- Electrical modeling of bundled 3-D vias
- Thermal modeling of 3-D via
- ***Effect of 3-D via placement on transistor properties***

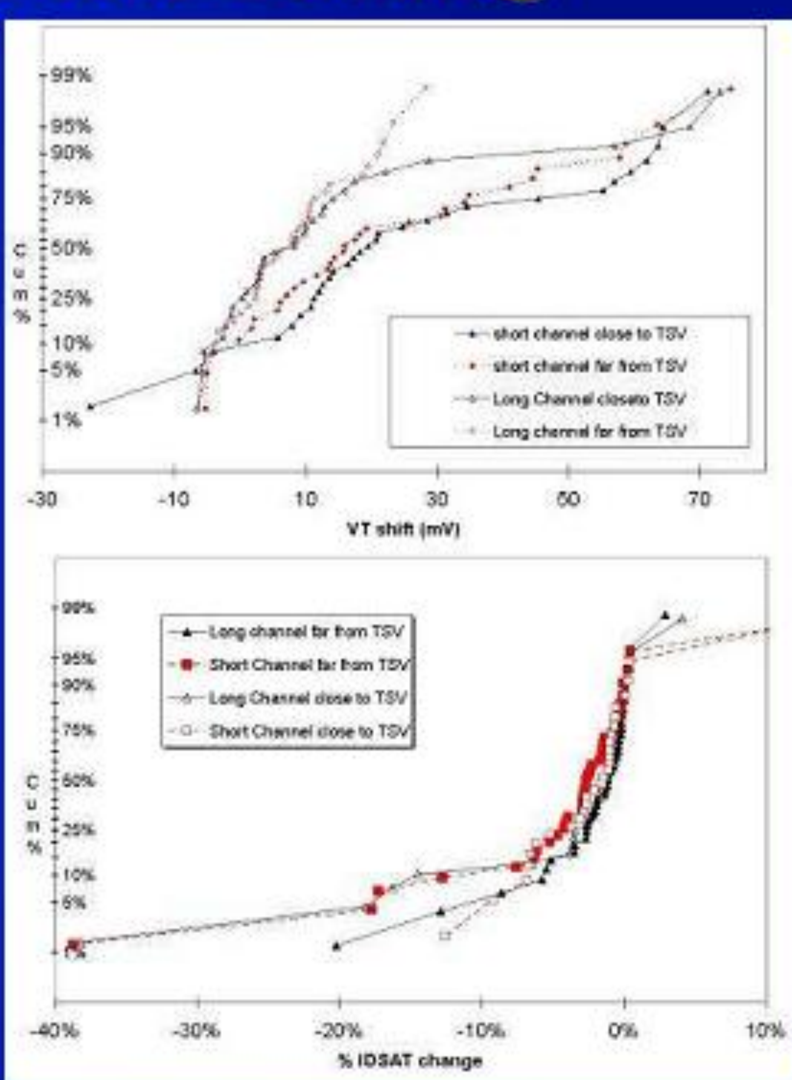
Impact on transistor performance



Determine proximity effect by placing large TSVs within arrays of individual transistors

Die stacking TSV device testing

- Measured V_T and I_{DSAT} on devices before and after processing in near and far proximity to TSV.
- Negligible impact seen in V_T and I_{DSAT} for both PMOS and NMOS devices for all proximities studied.
- Tails due to non-optimized thinning process.
- Determined that keep-out zone will not grow die area.



Michael Newman, et. al, "Fabrication and Electrical Characterization of 3D Vertical Interconnects", 2006 Proc. 56th Electronic Components & Technology Conf., May 2006

Presentation Outline

- Three-dimensional (3-D) integration
- Physical design techniques
- TSV modeling
- ***Design methodologies and flow***
- 3-D architectures
- Rochester test chips – past, present, and future
- Conclusions

Objective for 3-D CAD Tools

"New design tools will be required to optimize interlayer connections for maximized circuit performance…"

TSVs

- Density / consume silicon area
- Impedance characteristics

Heterogeneity

- Interdie process variations
- Disparate technologies

Interconnect length

- Longest nets in a 3-D system

*M. Ieong *et al.*, "Three Dimensional CMOS Devices and Integrated Circuits," *Proceedings of the IEEE International Custom Integrated Circuits Conference*, pp. 207-213, September 2003

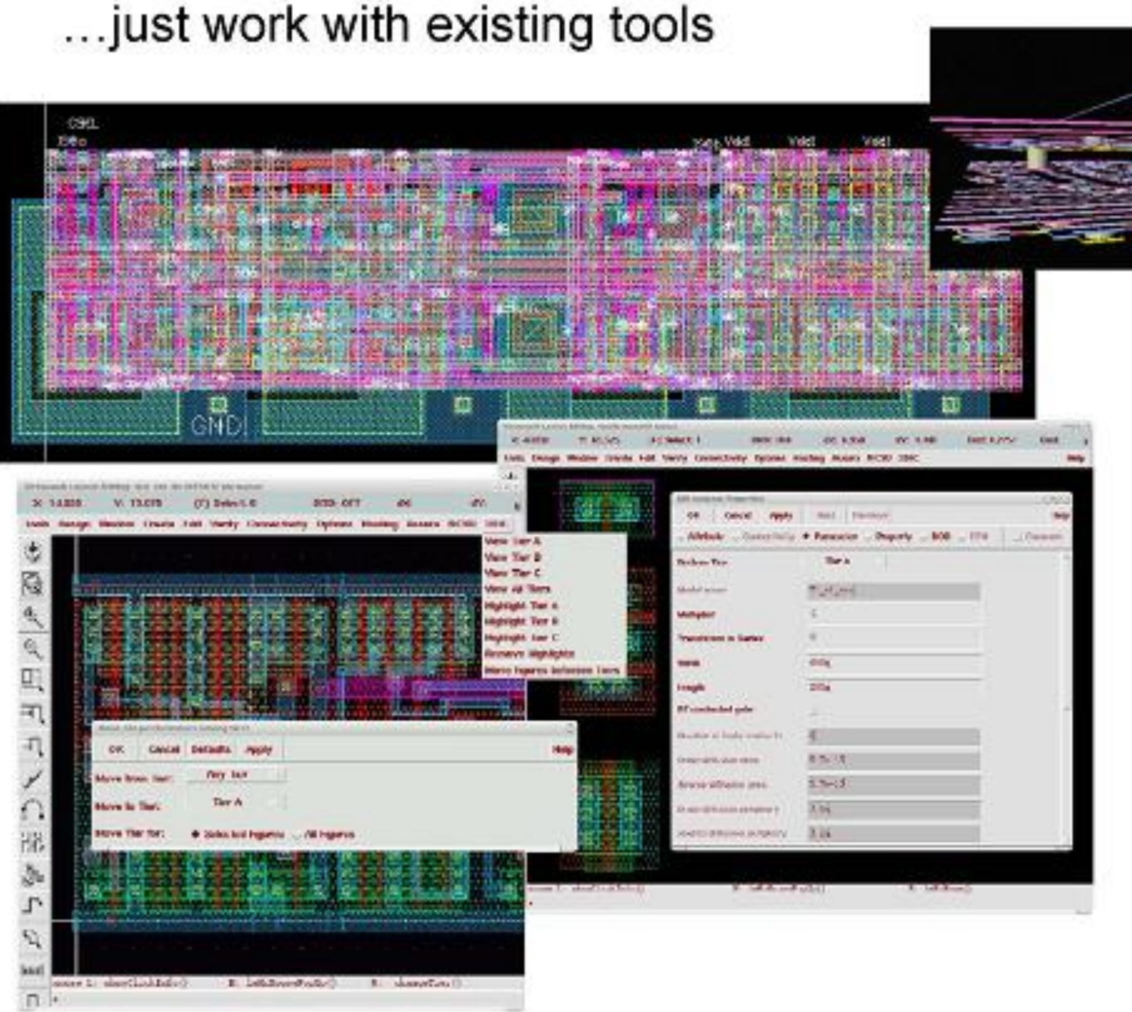
3-D Tools: A Work in Progress

- True 3-D commercial tools (3-D LVS, DRC capable)
  - R3Logic, Max-3D, PTC-PRO/E
- Need to accelerate digital IC design tools
  - Place and route tools
  - General floorplanning
  - Thermally-aware floorplanning
  - Power delivery
  - Power management
  - Clock delivery

- Integrate existing 2-D flows with 3-D analysis engines
- Package and IC design tools for mechancial, electrical, and thermal analysis

In the Beginning… (everything was easy)

…just work with existing tools



Painful, but doable IF:

- Circuits are small
- Via placement is known
- Process only has 20 layers

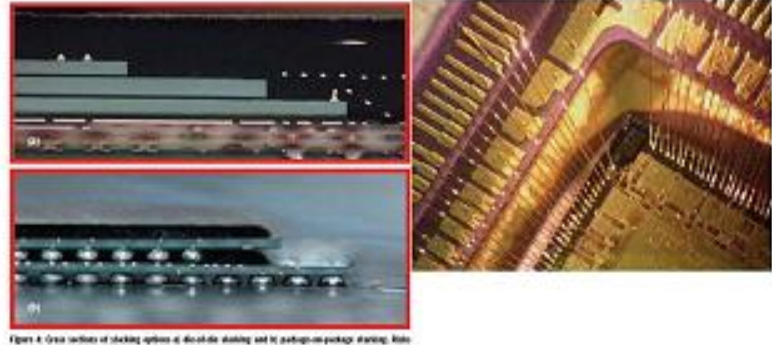
© 2008 R3Logic

DRC, LVS, Transistor synthesis, Crossprobing. Multiple tapeouts, 0.35um-45nm >20GB, ~10B devices

3D EDA Tool Needs By Application

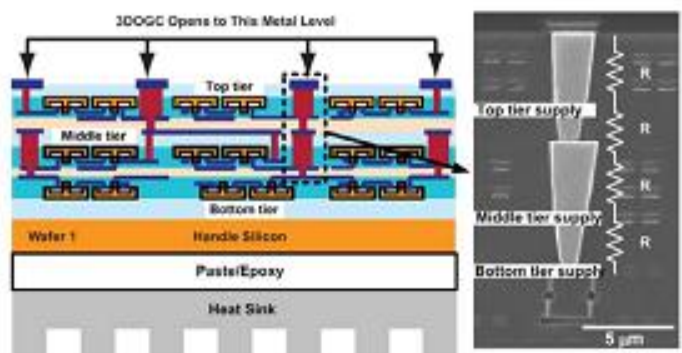
3D Package Design

- Signal Integrity
- Crosstalk
- Mechanical / thermal issues
- KGD (Known Good Die)
- Power Delivery

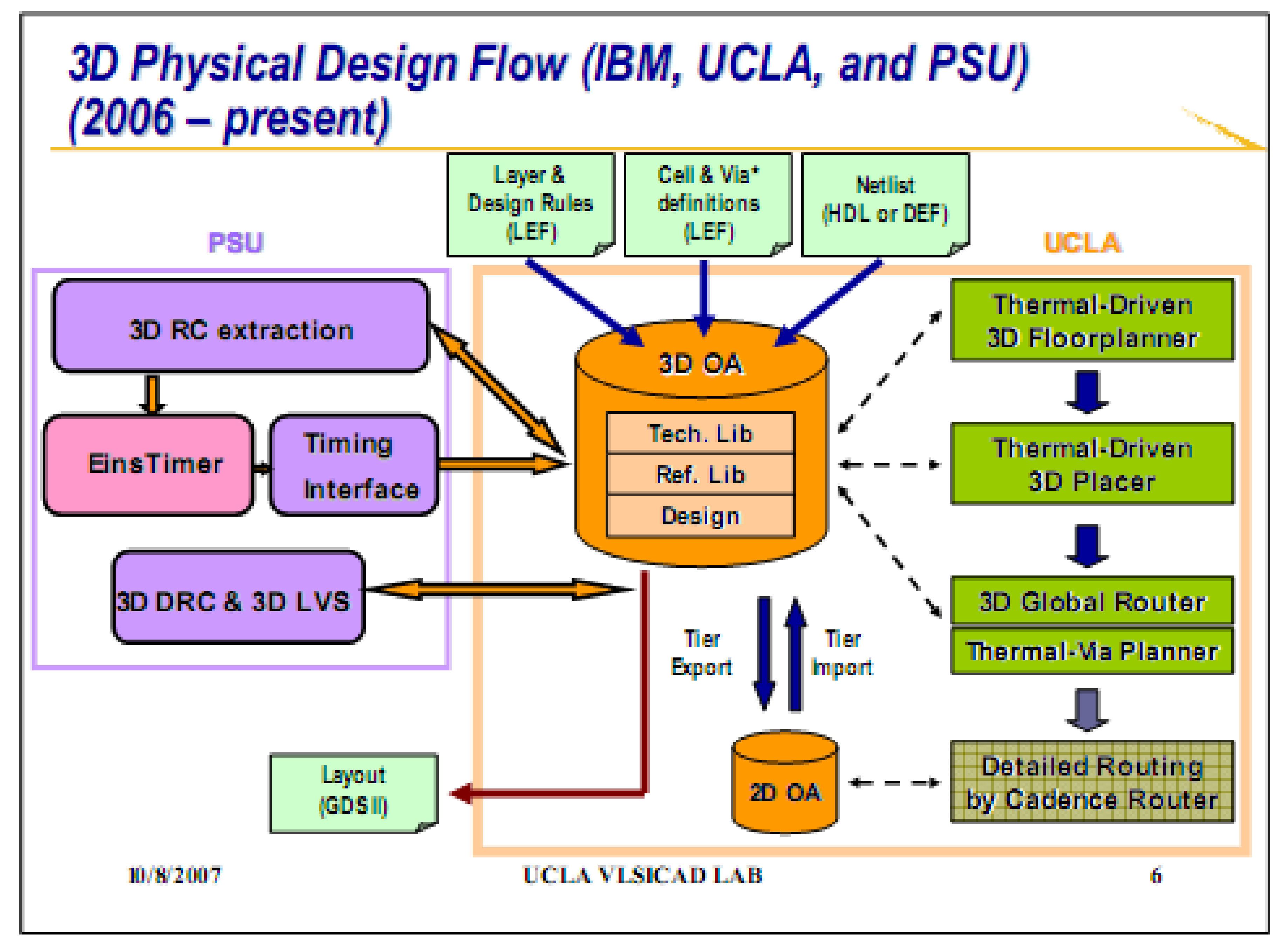


3D IC Design

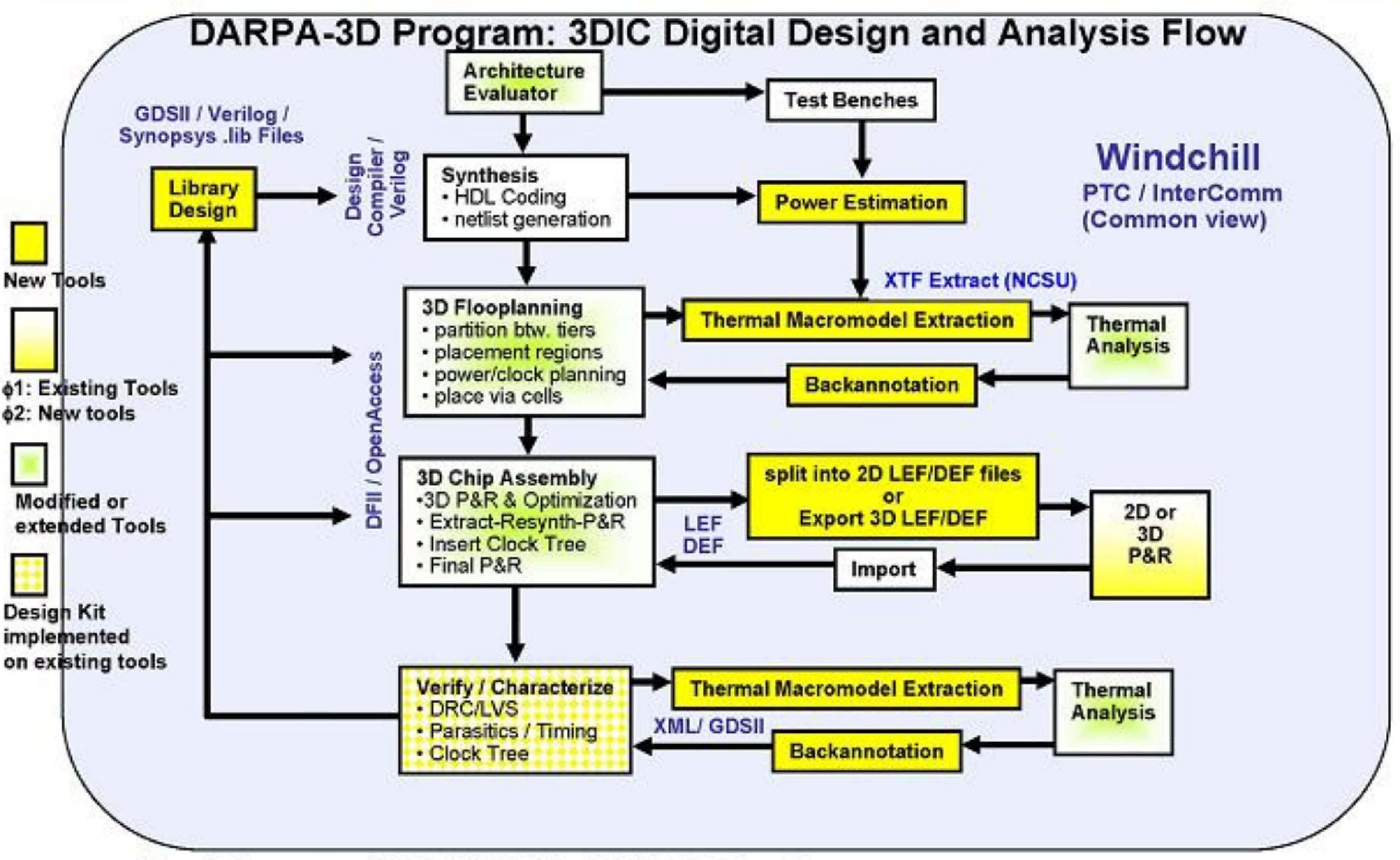
- IP Reuse
- Floorplanning / Partitioning
- Synthesis P&R
- MGD (Maybe Good Die)
- DFT / DFR (Design-for-Repair)
- Thermal management
- Power Delivery
- Mask layout / DRC / ERC



© 2008 R3Logic


3D Physical Design Flow (IBM, UCLA, and PSU) (2006 – present)
Layer & Design Rules (LEF)
Cell & Via* definitions (LEF)
Netlist (HDL or DEF)
PSU
UCLA
3D RC extraction
EinsTimer
Timing Interface
3D DRC & 3D LVS
3D OA
Tech. Lib
Ref. Lib
Design
Thermal-Driven 3D Floorplanner
Thermal-Driven 3D Placer
3D Global Router
Thermal-Via Planner
Detailed Routing by Cadence Router
Tier Export
Tier Import
2D OA
Layout (GDS II)

Getting There: On-going Research



Participants: PTC-NCSU-UMN-R3Logic

© 2008 R3Logic

Elements of the 3D Design Eco-System

Key handoff criteria

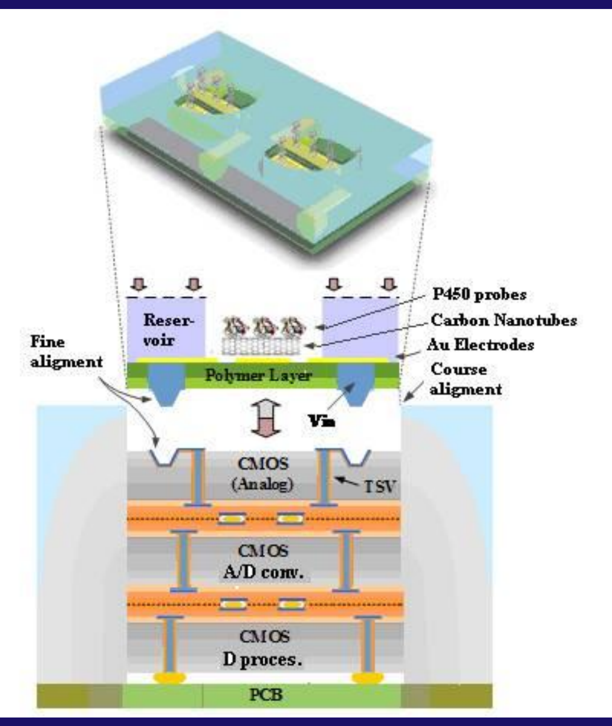
- to verify 2D SoCs are:
  - Functionality
  - Timing/SI
  - Power dissipation
  - Testability / Coverage
  - Manufacturability,...
- for 3D stacks <u>also</u> verify:
  - Alignment of TSVs
  - TSVs & return channels
  - Inter-die noise coupling
  - Magnetic interference
  - Thermal interaction
  - Mechanical stress
  - Testability of stack,...

Presentation Outline

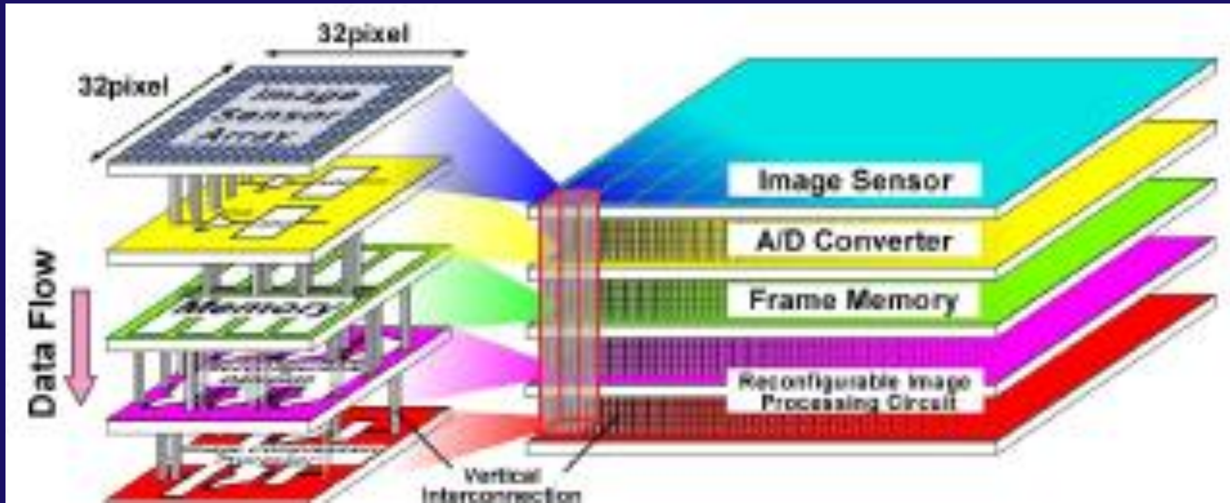
- Three-dimensional (3-D) integration
- Physical design techniques
- TSV modeling
- Design methodologies and flow
- ***3-D architectures***
- Rochester test chips – past, present, and future
- Conclusions

Applications of 3-D Integrated Systems

- Lab on a chip

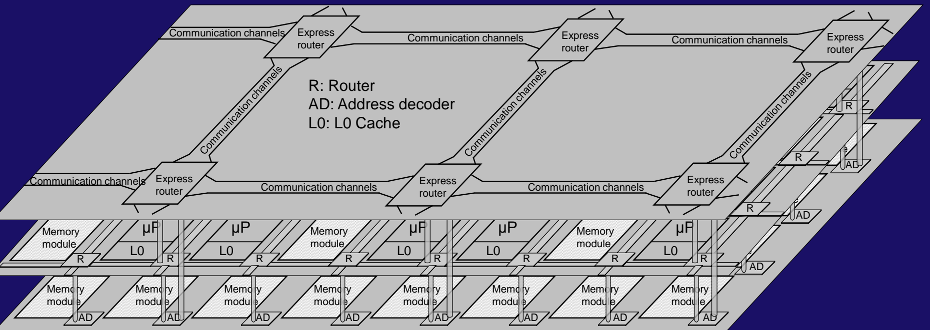


- Real–time image processing systems



*M. Koyanagi, T. Fikushima, and T. Tanaka, "Three-Dimensional Technology and Integrated Systems," *Proceedings of the IEEE Asia and South Pacific Design Automation Conference,* pp. 409-415, January 2009.

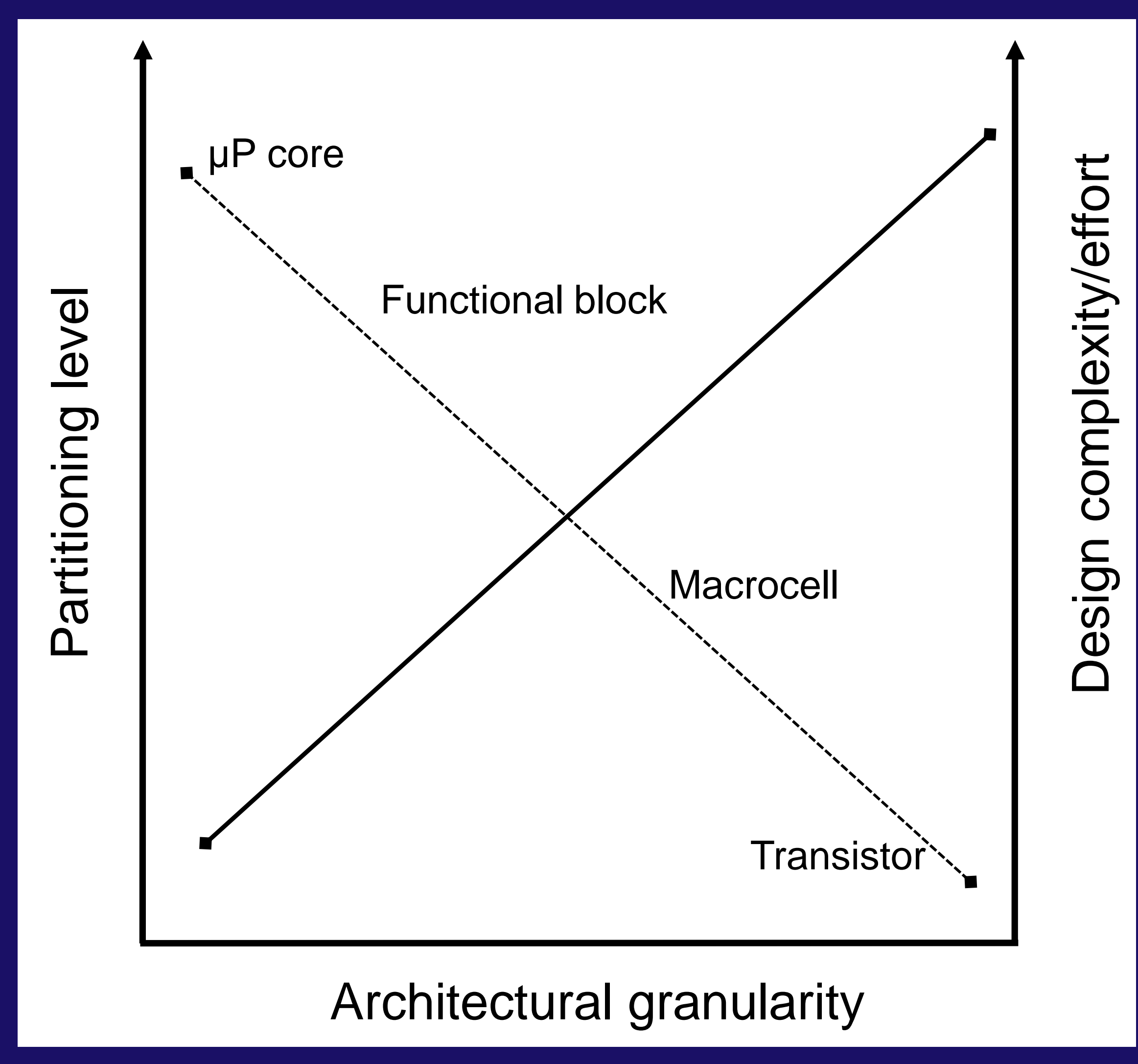
- Multi-core 3-D architectures

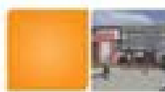
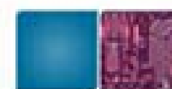
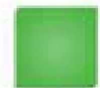


3-D Architectures

- ***Memory on logic***
- Communication networks: NoC
- Heterogeneous 3-D Systems
- Heterogeneous 3-D systems: free-space optics
- Heterogeneous 3-D systems: optical waveguides

3-D Microprocessors and Memories

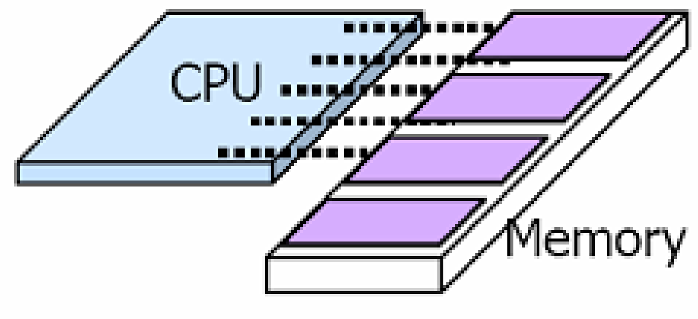


The Art of Stacking

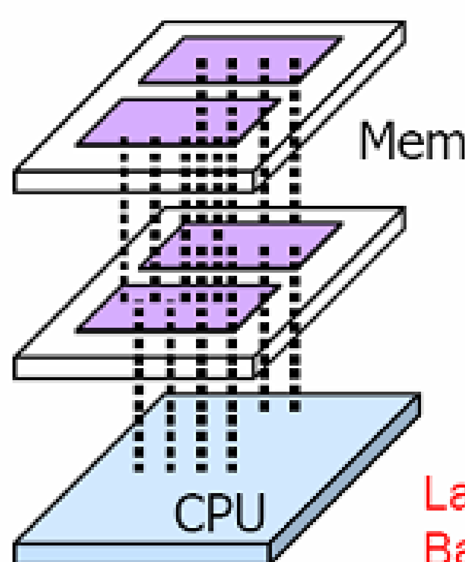
- Stacking array-based components
  - Tezzaron's FaStack including stacked SRAM, SRAM+controller, DRAM
  - ZyCube image sensors
  - Samsung's WSP (4x) stacked 2Gb DRAM
- Stacking distinct components (for embedded systems)
  - Processor
  - SRAM
  - DRAM
  - Peripherals
- Processor with Stacked 2D Modules
  - Many cores and cache banks
  - 2D modules placement in 3D space
- Processor with Stacked 3D Modules
  - Module folding
  - Bit slicing
  - Stratified CMOS: PMOS + NMOS

3D - Memory Access



2-D: Connections on the periphery

- Long global connections
- CPU to off-chip main memory with latency and misses



3-D: Connections across the area

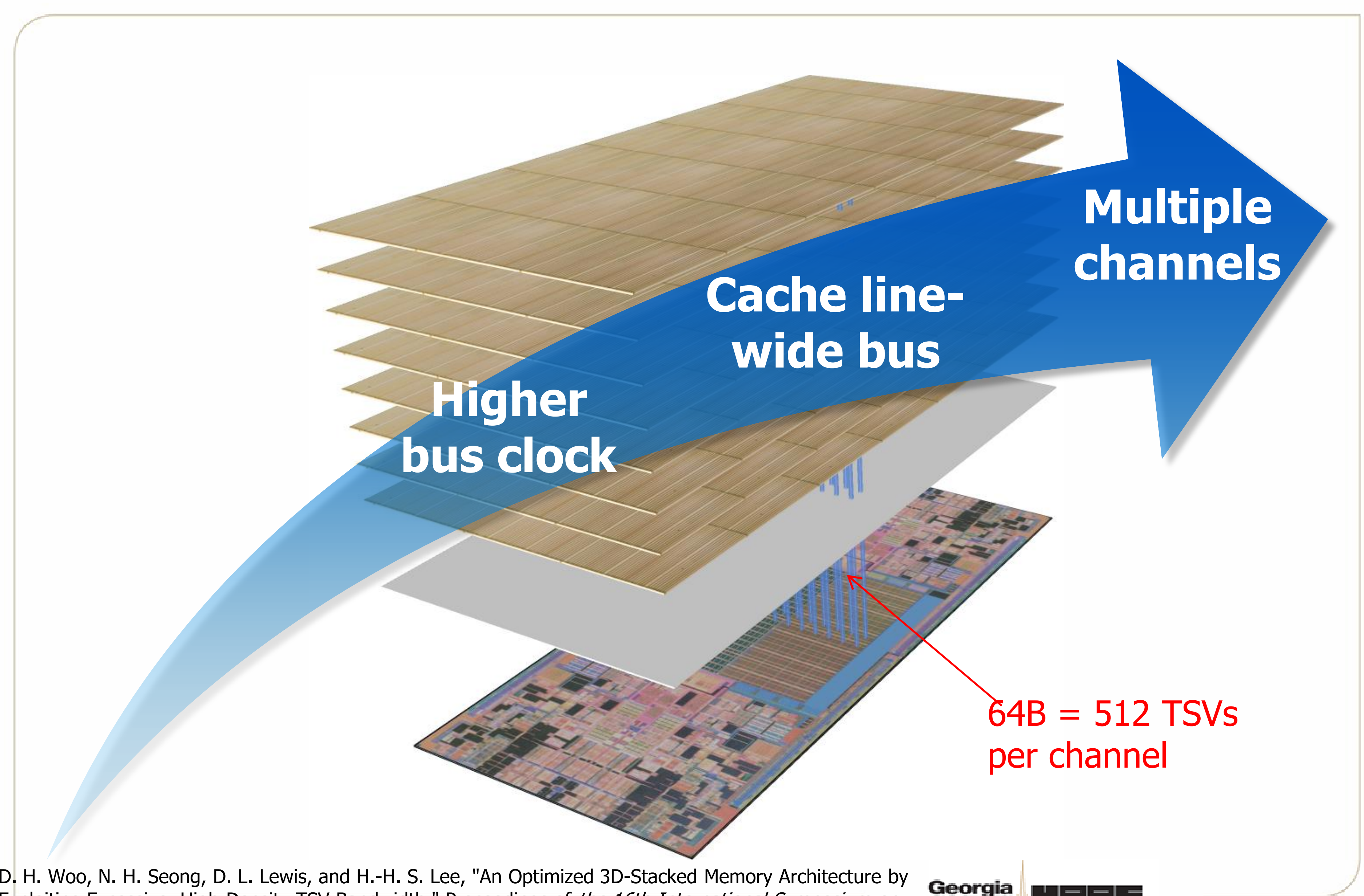
- Connections short + vertical
- Suitable for high-bandwidth and vector operations
- No pin cost, large block access of data

Latency: Important for random access (servers, e.g.), single core
Bandwidth: Multiple cores, multi-threads, graphics

S. Tiwari; "Potential, Characteristics, and Issues of 3D SOI; 3D SOI Opportunities" Short Course, 2005 International SOI Conference

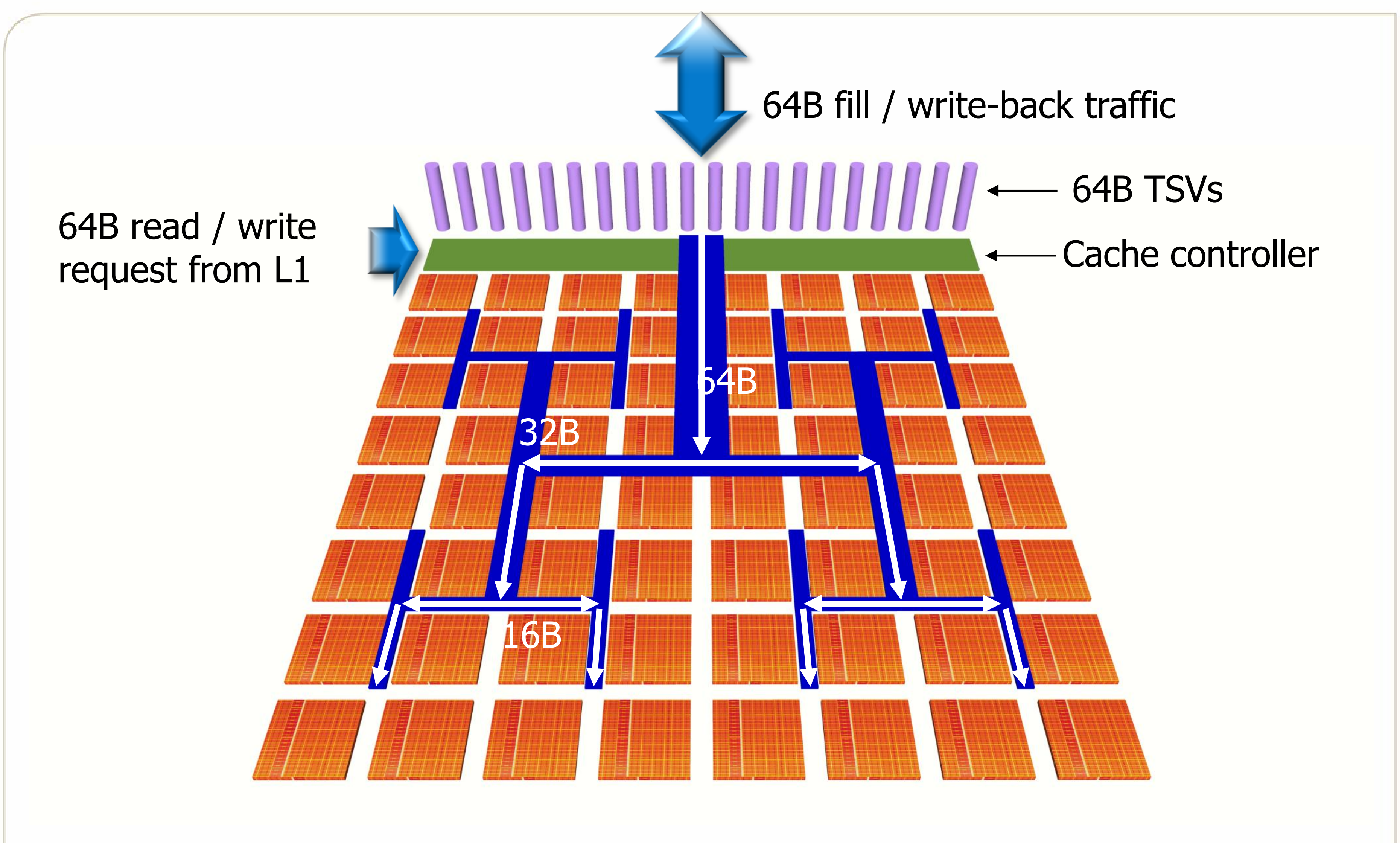
© 2008 IBM Corporation

3D-Stacked DRAM



D. H. Woo, N. H. Seong, D. L. Lewis, and H.-H. S. Lee, "An Optimized 3D-Stacked Memory Architecture by Exploiting Excessive, High-Density TSV Bandwidth." Proceedings of *the 16th International Symposium on High-Performance Computer Architecture*, pp.429-440, Bangalore, India, January, 2010.

Conventional Subarray Technique



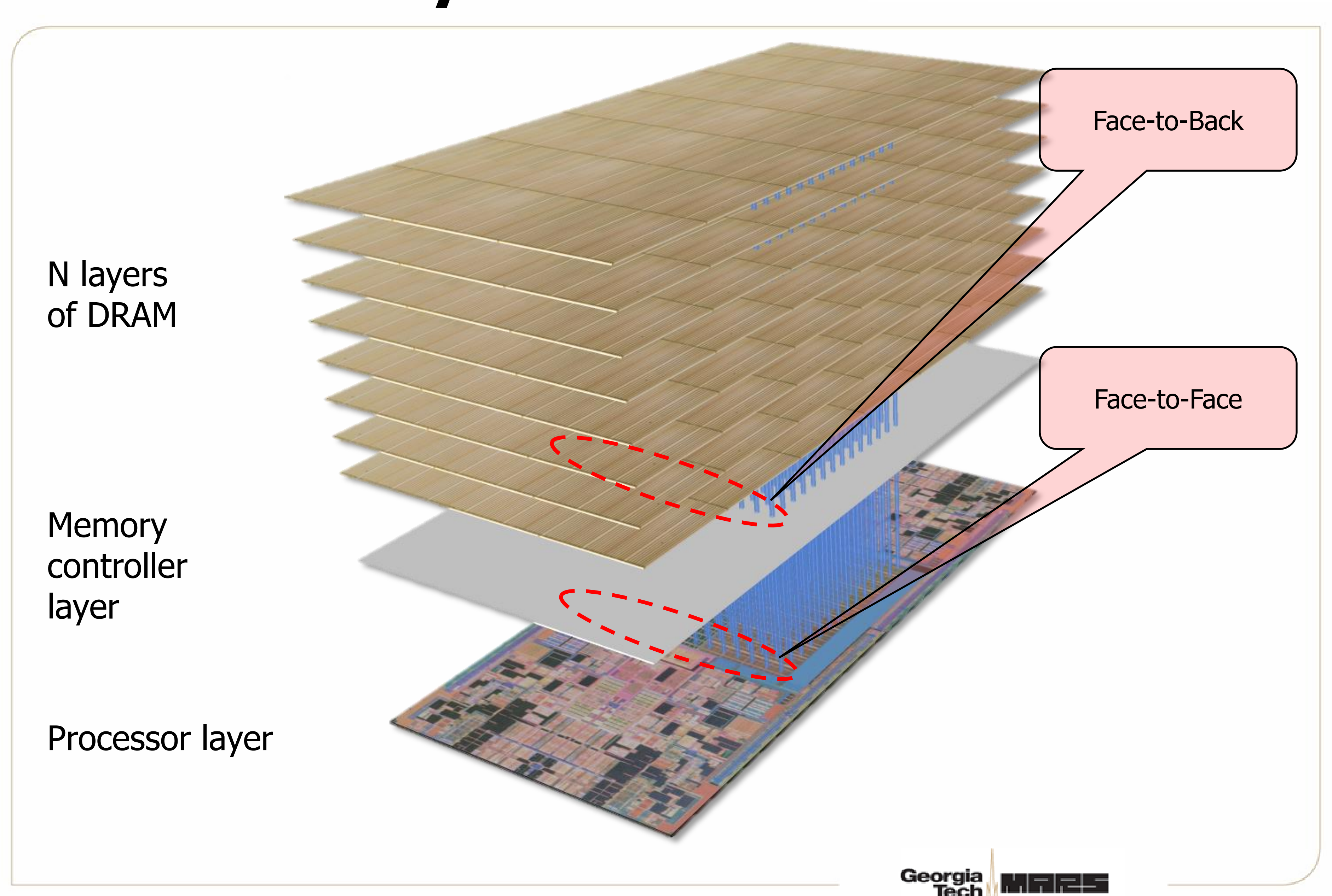
SMART-3D Cache Design

4KB fill / write-back traffic
(64B per subbank)

One or two cycles higher latency

D. H. Woo, N. H. Seong, D. L. Lewis, and H.-H. S. Lee, "An Optimized 3D-Stacked Memory Architecture by Exploiting Excessive, High-Density TSV Bandwidth." Proceedings of *the 16th International Symposium on High-Performance Computer Architecture*, pp.429-440, Bangalore, India, January, 2010.

SMART-3D System Architecture



DRAM Design Issues in SMART-3D

256Mb DRAM array per tile

256 TSVs per tile

32k Shared TSVs

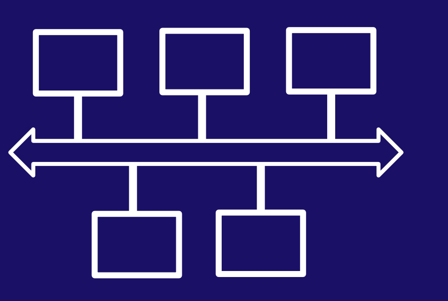
Folded DRAM layers

D. H. Woo, N. H. Seong, D. L. Lewis, and H.-H. S. Lee, "An Optimized 3D-Stacked Memory Architecture by Exploiting Excessive, High-Density TSV Bandwidth." Proceedings of *the 16th International Symposium on High-Performance Computer Architecture*, pp. 429-440, Bangalore, India, January, 2010.

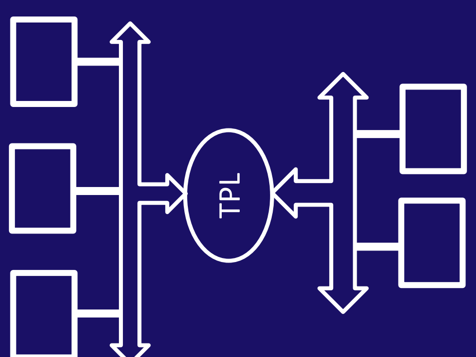
3-D Architectures

- Memory on logic
- ***<u>Communication networks: NoC</u>***
- Heterogeneous 3-D Systems
- Heterogeneous 3-D systems: free-space optics
- Heterogeneous 3-D systems: optical waveguides

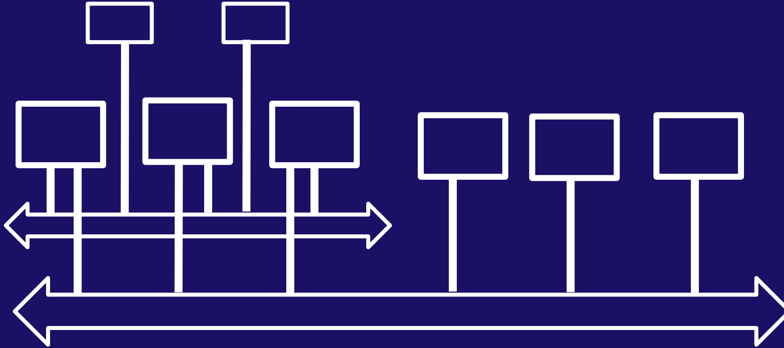
Evolution of Interconnect Architectures



- Shared buss

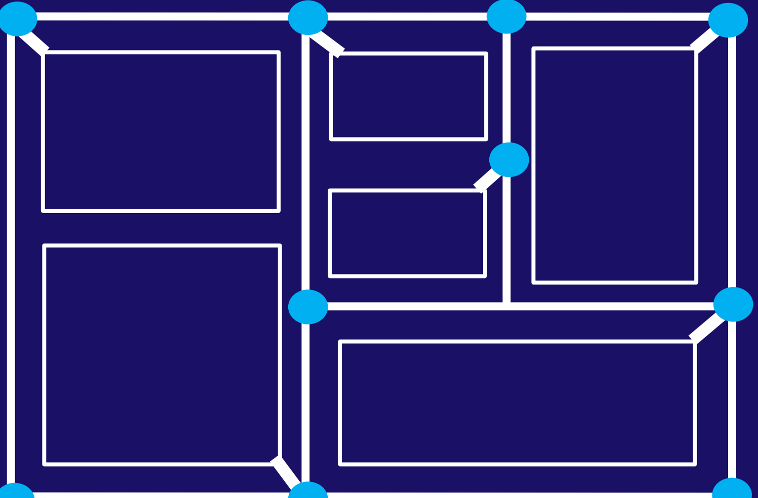


- Segmented buss



- Multi-level segmented buss

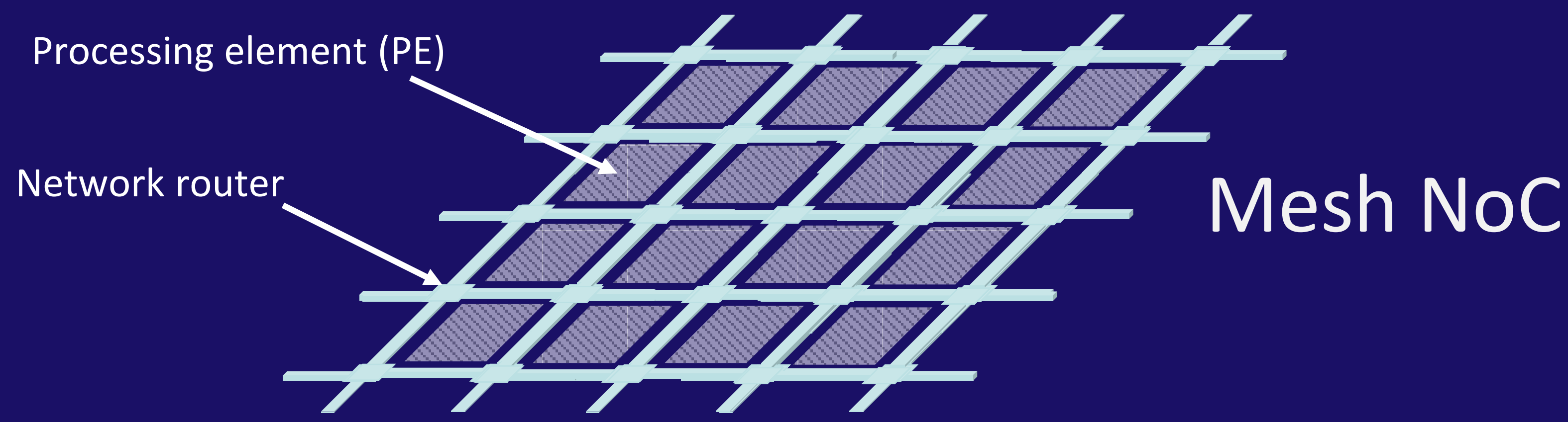
- Buss architecture limitations
  - Large buss delays
  - Data contention for resources
  - Signal integrity



- Network-on-chip

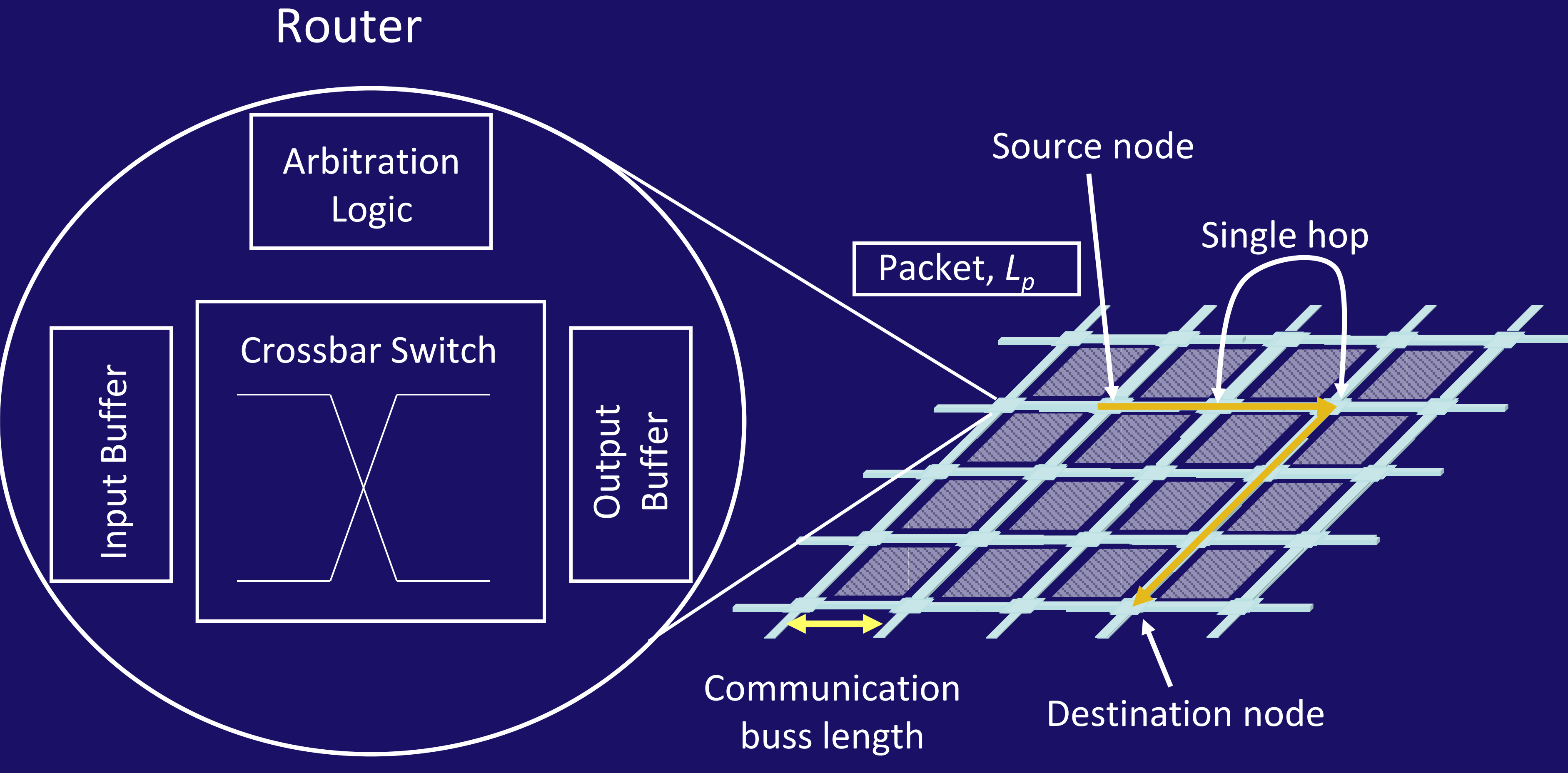
Network-on-Chip (NoC)

- Network-on-chip is another approach to mitigate the interconnect bottleneck in modern IC design
  - Canonical interconnect structure
  - Shared interconnect bandwidth
  - Increased flexibility
- PEs exchange data packets through the network in an internet-like manner
- Network routers transfer data within the network similar to computer networks

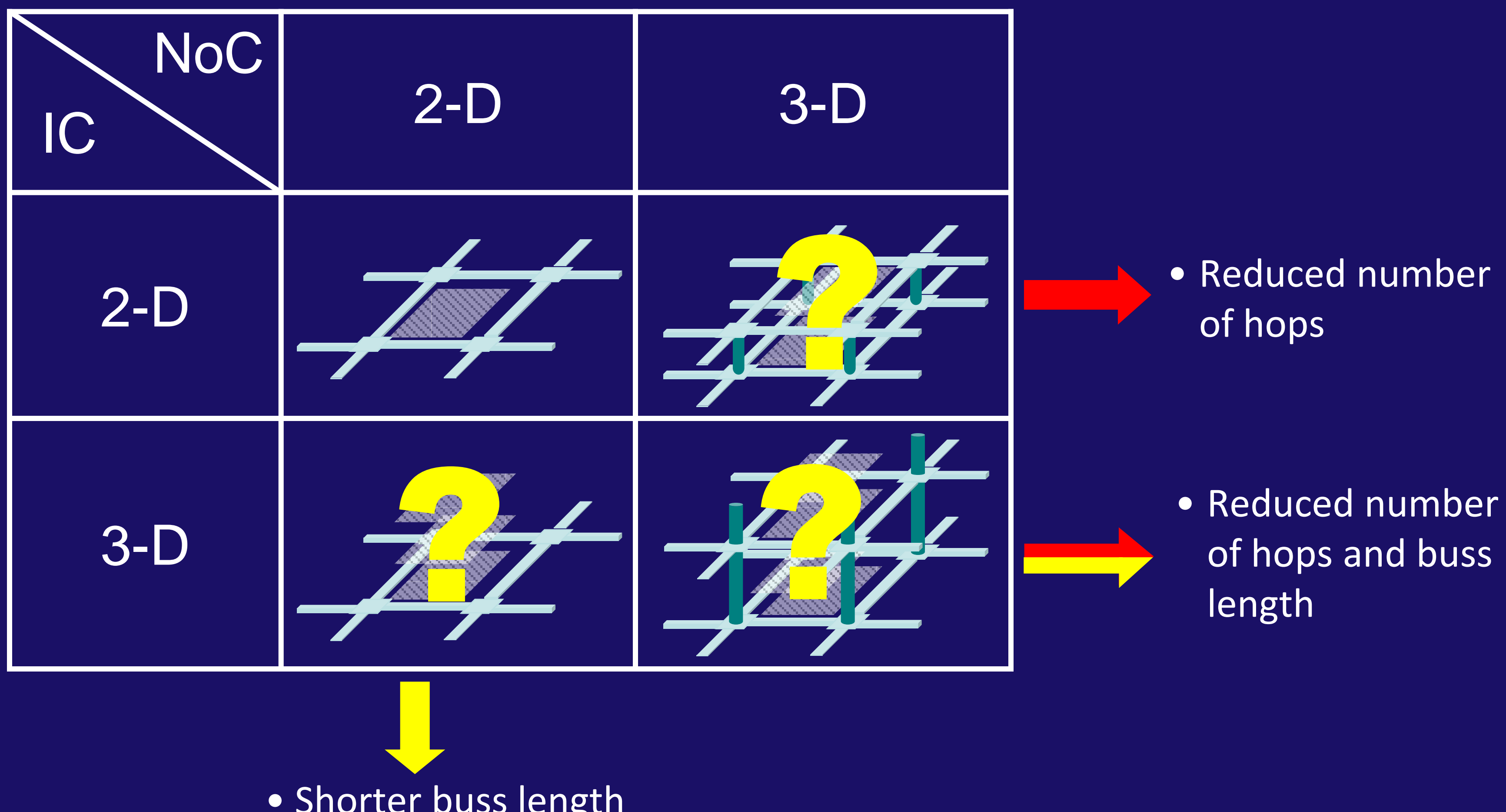


Mesh NoC

NoC Mesh Structure



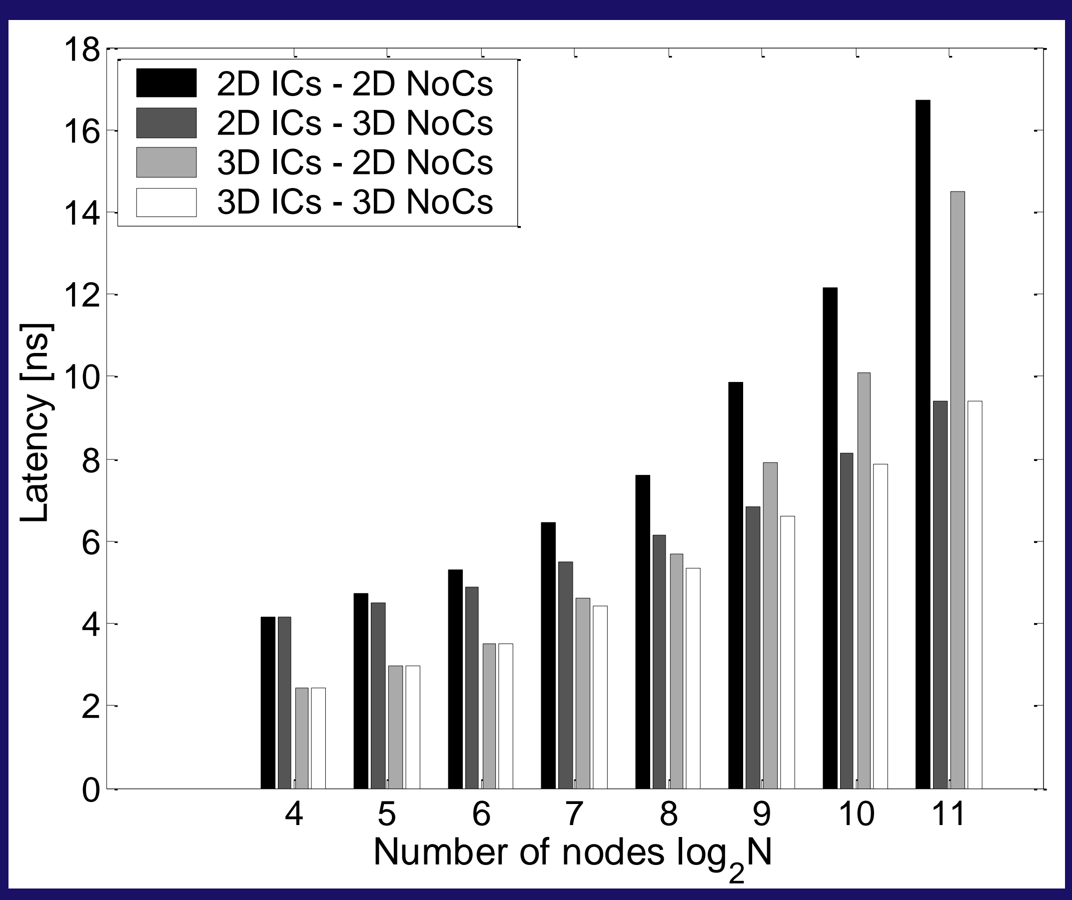
Various Topologies for 3-D Mesh IC-NoC



[*] V. F. Pavlidis and E. G. Friedman, "3-D Topologies for Networks-on-Chip," *IEEE Transactions on Very Large Integration (VLSI) Systems,* Vol. 15, No. 10, pp. 1081-1090, October 2007

Performance Comparison for 3-D NoC Topologies

- Dense networks with small PE areas favor 3-D NoCs and 2-D ICs
  - Due to large number of hops and short busses
- Small networks with large PE areas favor 3-D IC and 2-D networks
  - Due to small number of hops and long busses



- A_{PE} = 4 mm^2
- Impr. = 36.2%, N = 256

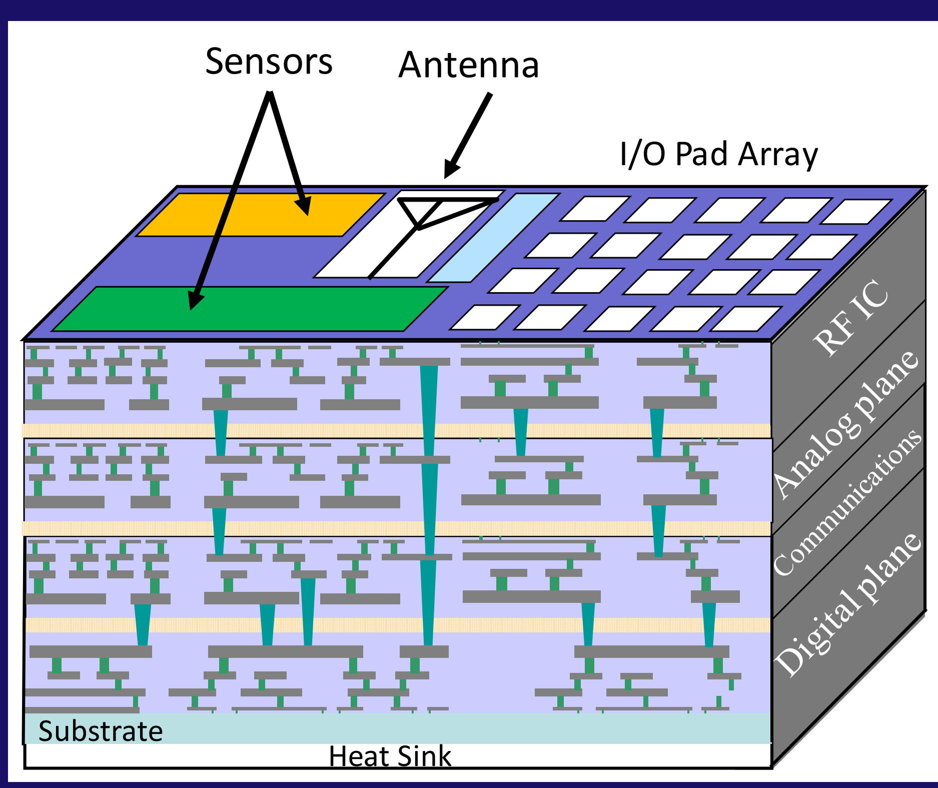
* V. F. Pavlidis and E. G. Friedman, "3-D Topologies for Networks-on-Chip," *Proceedings of the IEEE International SOC Conference*, pp. 285-288, September 2006

3-D Architectures

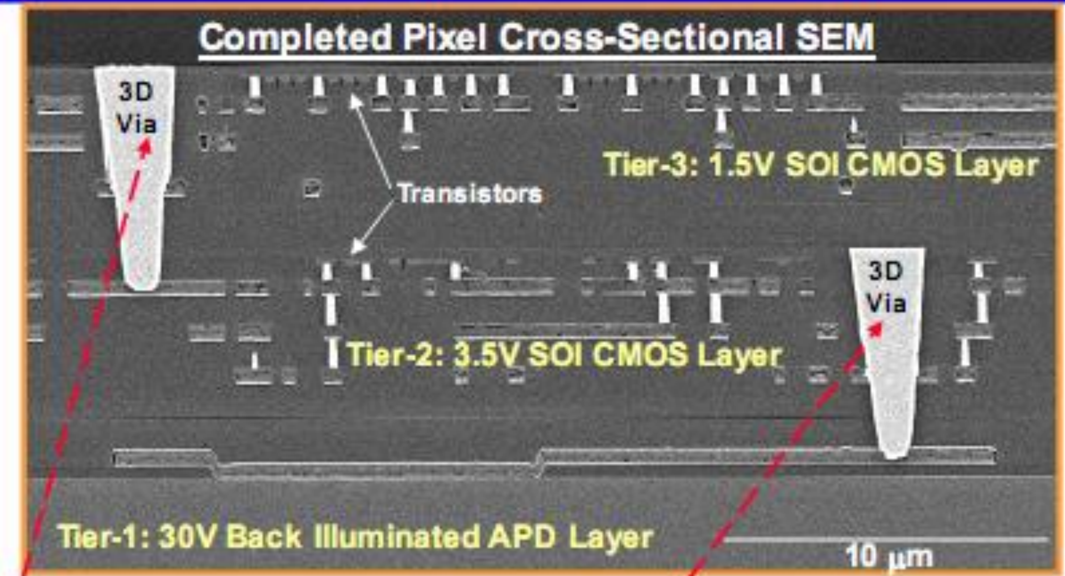
- Memory on logic
- Communication networks: NoC
- ***Heterogeneous 3-D Systems***
- Heterogeneous 3-D systems: free-space optics
- Heterogeneous 3-D systems: optical waveguides

Heterogeneous 3-D Integrated Systems

- Integrate processing and sensing within a multi-plane system
- Develop design methodologies to manage plane-to-plane interactions
  - Prevent processing planes from disturbing sensor planes
- Develop general purpose processing planes
  - Compatible with
    - Different types of sensors
    - Disparate communication schemes
- Manage heterogeneous data fusion



3D-Integrated, 3-Tier Avalanche Photodiode Focal Plane



- *VISA* laser radar focal plane based on single-photon-sensitive Geiger-mode avalanche photodiodes
  - 64 x 64 format
  - 50-µm pixel size

To-Scale Pixel Layout of Completed 3-tier Laser Radar Focal Plane

Tier-3 High-Speed Counter

Tier-2 APD Drive/Sense Circuitry

Tier-1 Avalanche Photodiode (APD)

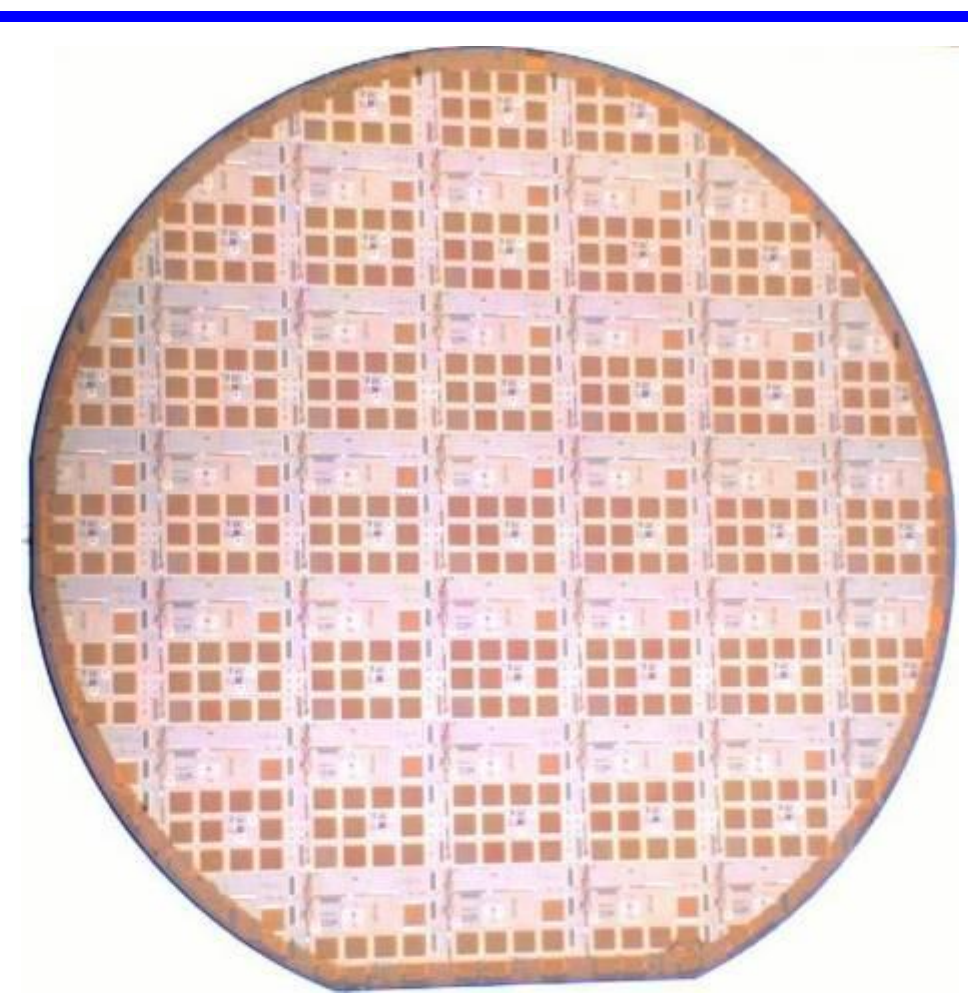
~250 transistors/pixel (50 µm x 50 µm)

Presented at 2006 ISSCC

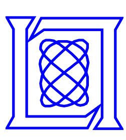
3D-Integration with III-V Detectors

Presented at 2006 IPRM

- **Enables extension of 3D-integration technology to higher density, longer wavelength focal plane detectors**
  - **Tight pixel-pitch IR focal planes and APD arrays**
  - **InGaAsP (1.06-μm), InGaAs (1.55-μm)**



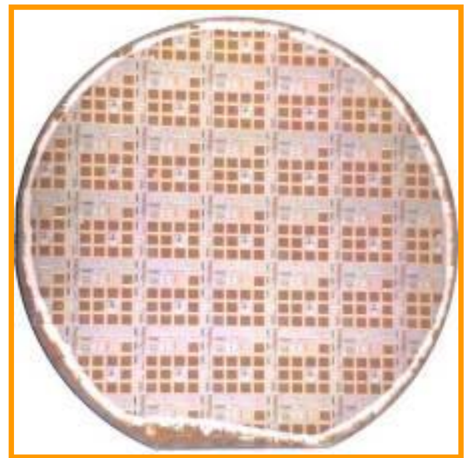
150-mm-diameter InP wafer with oxide-bonded circuit layer transferred from silicon wafer



Transferred CMOS-to-InP Integration
(Via-Chain Test Results)

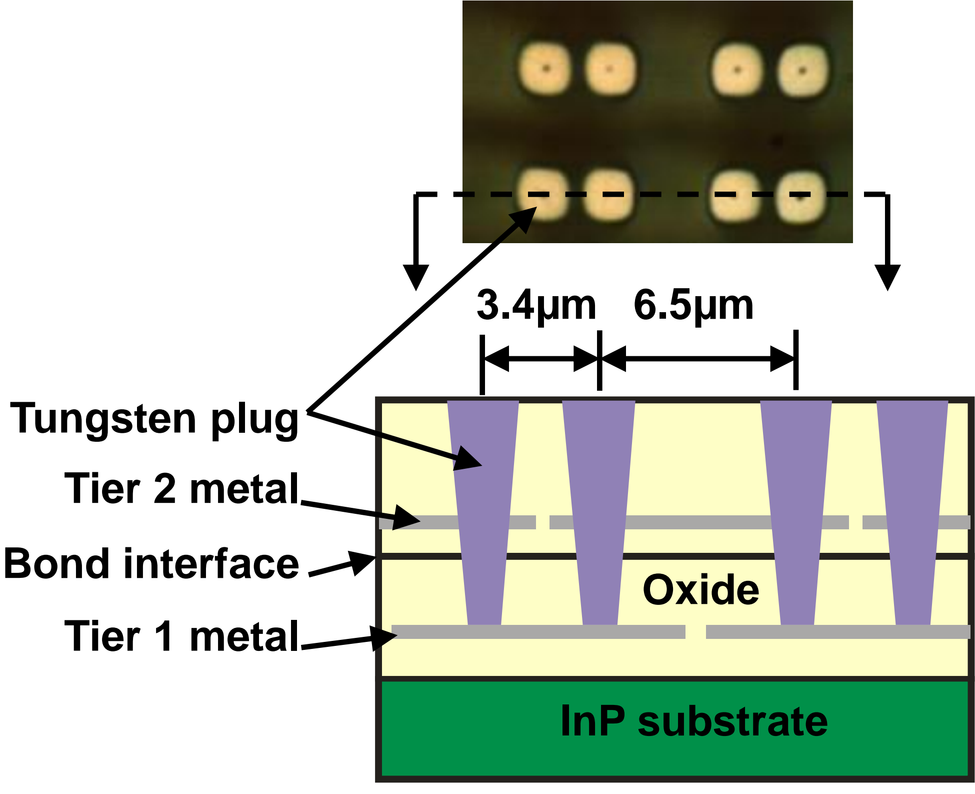
Wafer Die Map of Average 3D-Via Resistance (Ω) for 10,000-via Chains

	0.7	1.0	0.7	
0.8	0.8	0.6	0.8	0.8
0.8	0.8	1.0	0.8	0.7
0.8	0.8	0.8	0.8	0.8
	1.3	0.8	0.9	



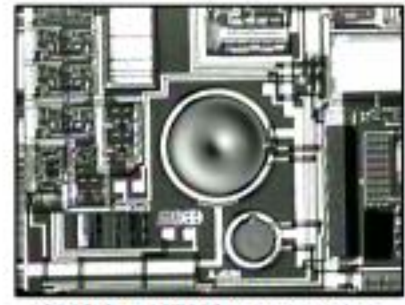
Photograph of 150-mm InP Wafer with Aligned and Bonded Tier

- **MIT-LL 3D integration and via processes successfully demonstrated on 150-mm InP wafers**

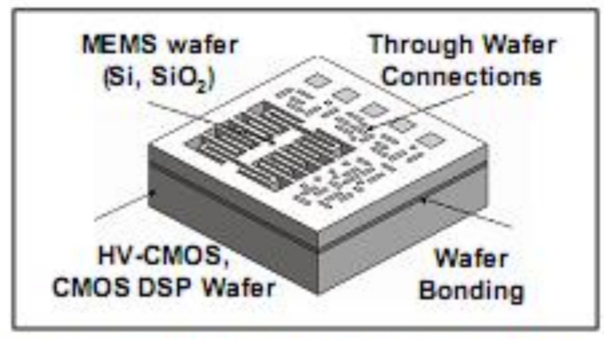


CMOS Technology for DALSA Integrated MEMS

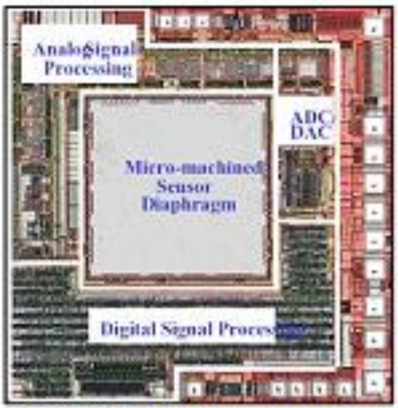
- DALSA integrates both in-house fabricated CMOS as well as sub-0.25μm DSP, telecom, RF-ID wafers made in Asia;
- Wafers made in Asia are currently cored from 200mm to 150mm before MEMS, WLP & BGAs integration



CMOS + MEMS automotive (Kavlico)



3D Integration of MEMS + HV-CMOS + CMOS DSP



CMOS + MEMS automotive (Freescale)

R. Brooks "Imaging and MEMS Enabling Technologies at DALSA," *Annual Executive Symposium on Photonics Commercialization, Canadian Photonics Fabrication Centre*, June 2006.

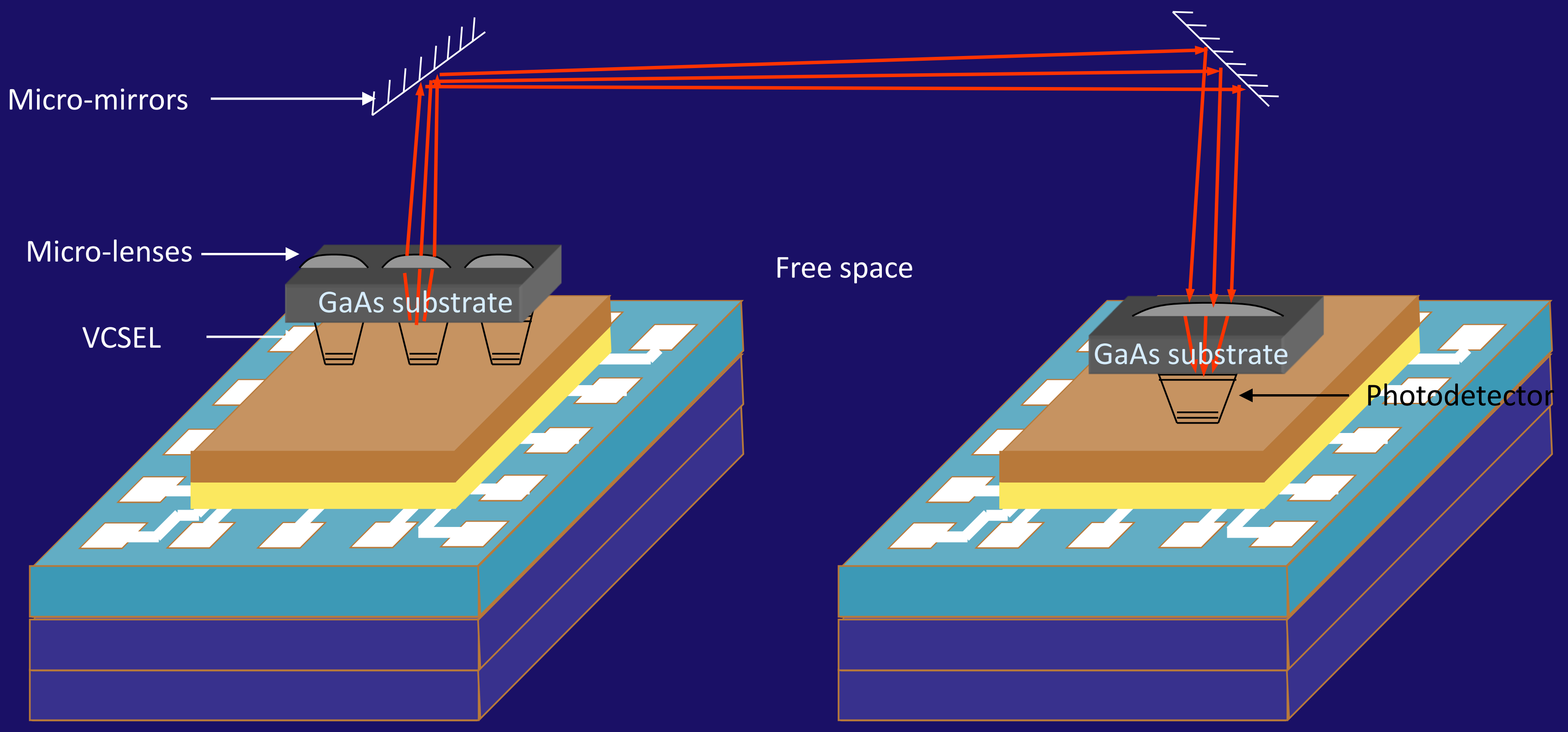
Example Wafer-Level Optical/Electrical/Mechanical Integration

3D interconnects of multiple function wafers. Vertical through wafer vias with ultra fine BGAs (40µm pitch) allow flip chip packaging on PCBs using lead free solders.

3-D Architectures

- Memory on logic
- Communication networks: NoC
- Heterogeneous 3-D Systems
- ***Heterogeneous 3-D systems: free-space optics***
- Heterogeneous 3-D systems: optical waveguides

3-D Free Space Optics



Dedicated transmitters

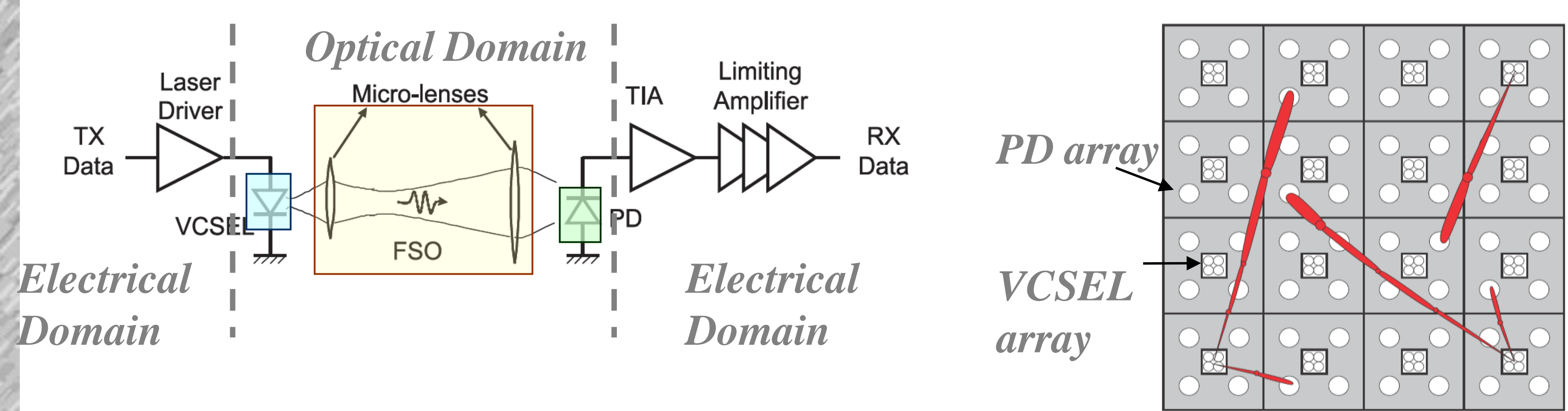
- ~ N^2 lasers
- Simple, fast (no WDM)
- Area = 5 mm^2 for 16 node system
- Consumes energy only when "ON"

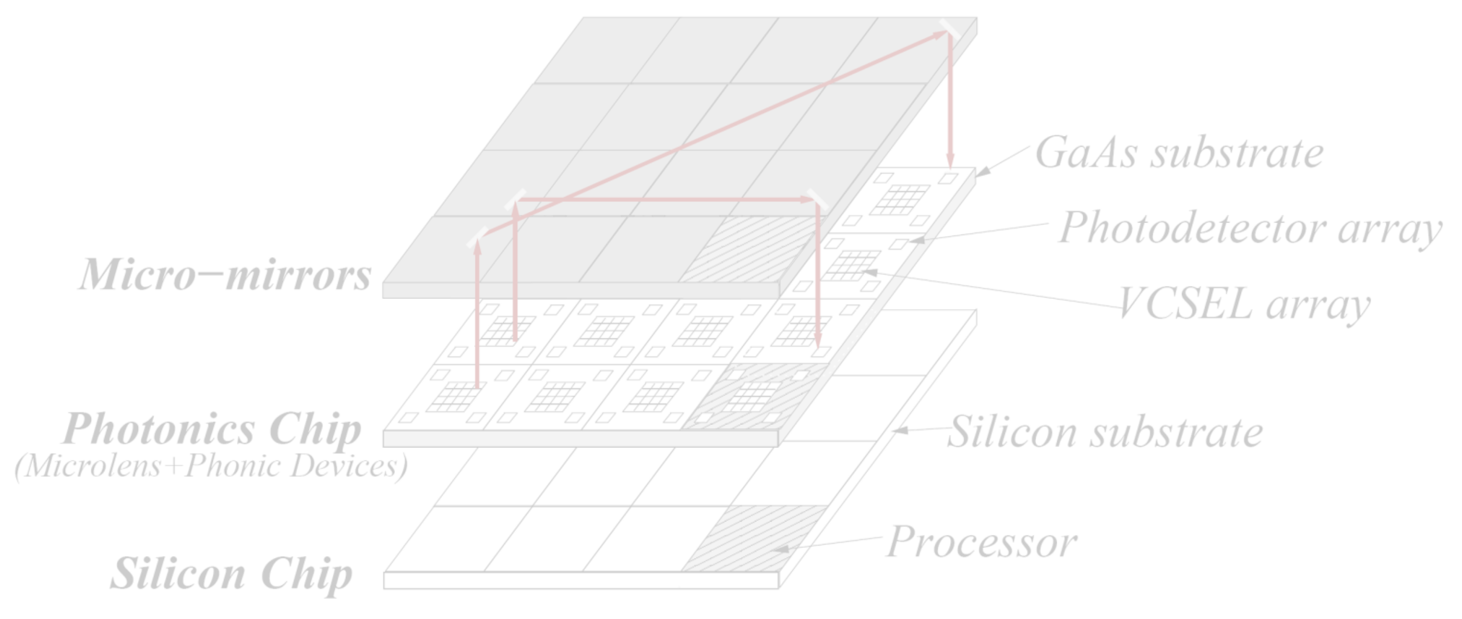
Shared receivers

- No dedicated receivers needed

J. Xue, A. Garg, B. Ciftcioglu, S. Wang, I. Savidis, J. Hu, M. Jain, M. Huang, H. Wu, E. G. Friedman, G. W. Wicks, and D. Moore, "An Intra-Chip Free-Space Optical Interconnect," *Proceedings of the 3rd Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI)* in conjunction with the International Symposium on Computer Architecture, June 2009.

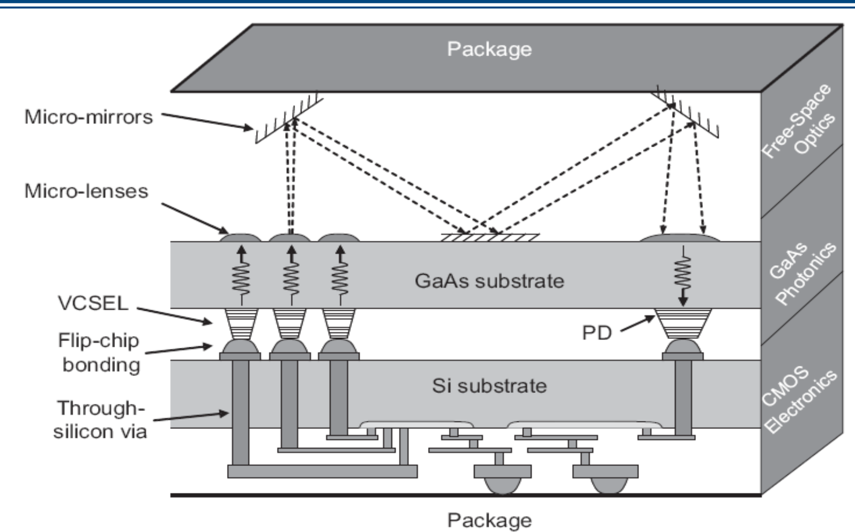
Optical Link and System Structure



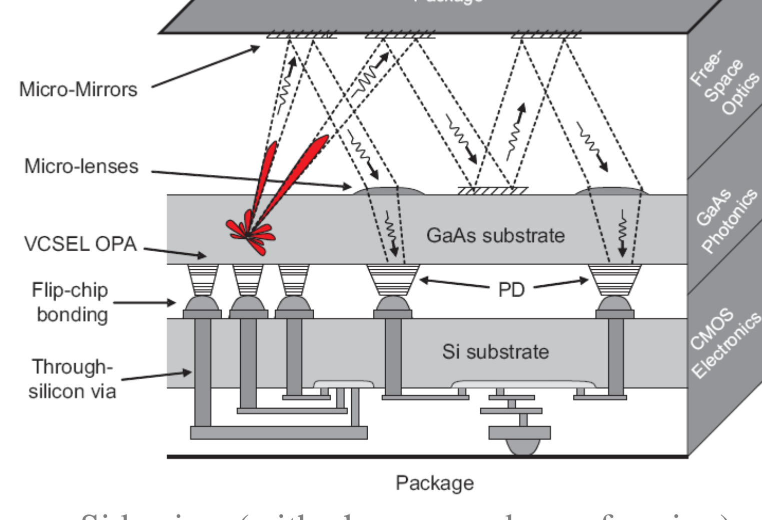


University of Rochester
MELIORA
1850

Chip Side View



Side view (mirror-guided only)



Side view (with phase array beam-forming)

- Mostly current (commercially available) technology
  - Large VCSEL arrays, high-density (movable) micro mirrors, high-speed modulators and PDs
- Efficiency: integrated light source, free-space propagation, direct optical paths

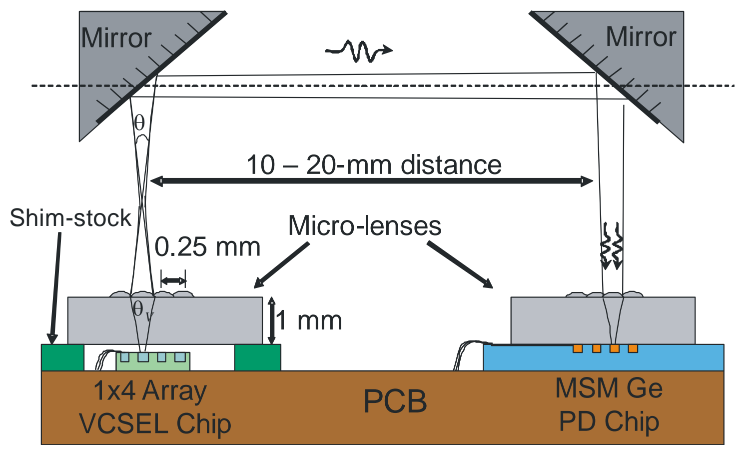
J. Xue, A. Garg, B. Ciftcioglu, J. Hu, S. Wang, I. Savidis, M. Jain, R. Berman, P. Liu, M. Huang, H. Wu, E. G. Friedman, G. Wicks, and D. Moore, "An Intra-Chip Free-Space Optical Interconnect," *Proceedings of the 37th International Symposium on Computer Architecture (ISCA)*, June 2010.

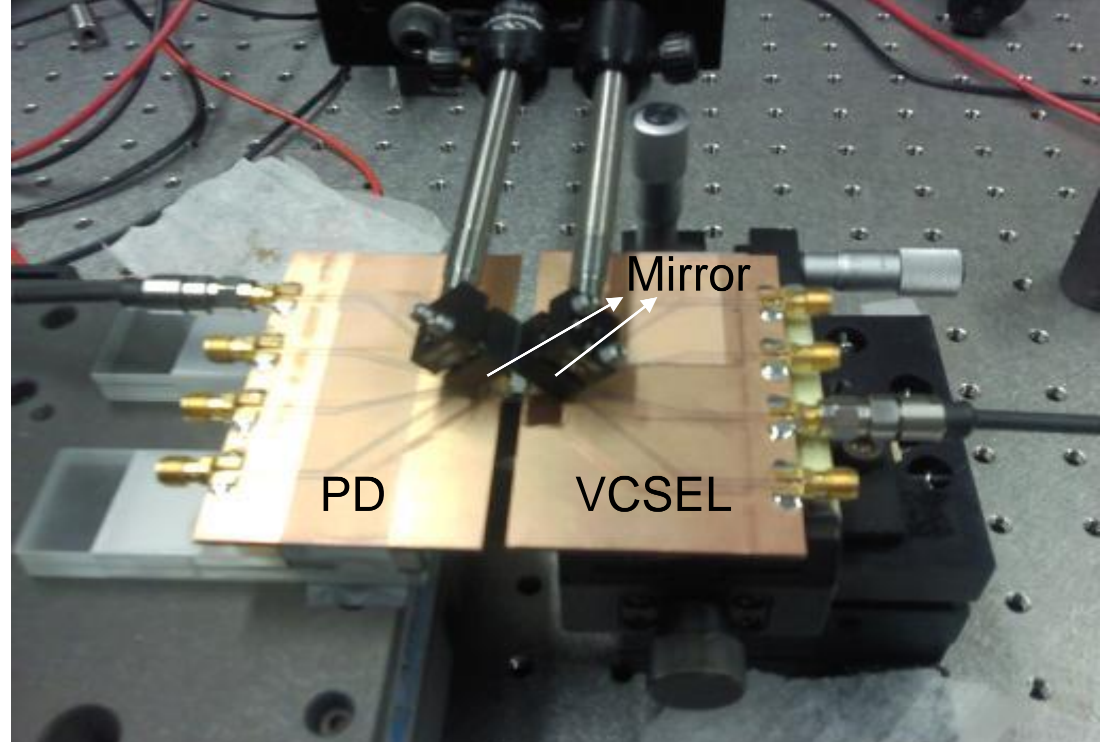
Readily Available Technology

Commercial VCSELs

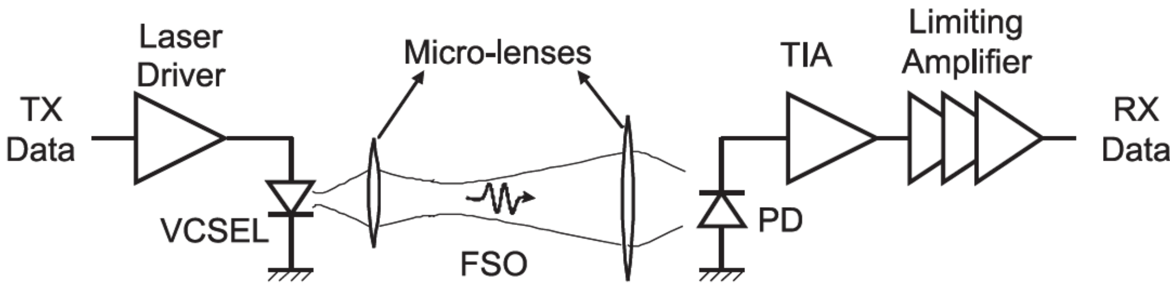
Commercial microlenses

Link Demo on Board Level





Efficient Optical Links

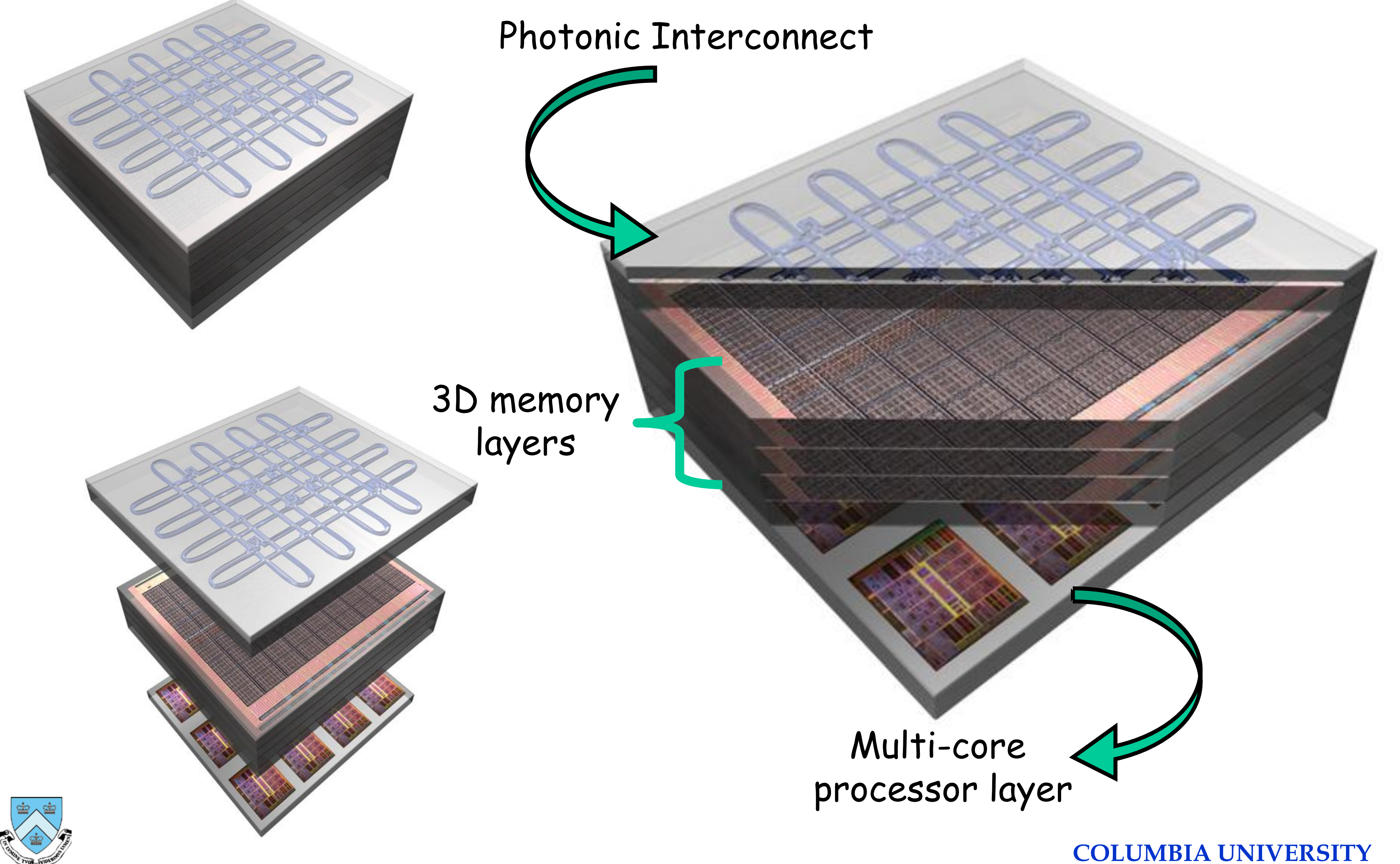


Free-Space Optics	
Transmission distance	2 cm
Optical wavelength	980 nm
Microlens aperture	90 μm @ transmitter, 190 μm @ receiver
Optical path loss	2.6 dB
Transmitter & Receiver	
VCSEL	aperture=5 μm, parasitic=235 Ω // 90 fF threshold=0.14 mA, extinction ratio=11:1
Laser driver	bandwidth=43 GHz
PD	responsivity=0.5 A/W, capacitance=100 fF
TIA & Limiting amp	bandwidth=36 GHz, gain=15000 V/A
Link	
Data rate	40 Gbps
Signal-to-noise ratio	7.5 dB
Bit-error-rate (BER)	10^{-10}
Cycle-to-cycle jitter	1.7 ps
Power Consumption	
Transmitter (active)	0.96 mW for VCSEL (0.48 mA@2V) 6.3 mW for laser driver
Transmitter (standby)	0.43 mW
Receiver	4.2 mW

3-D Architectures

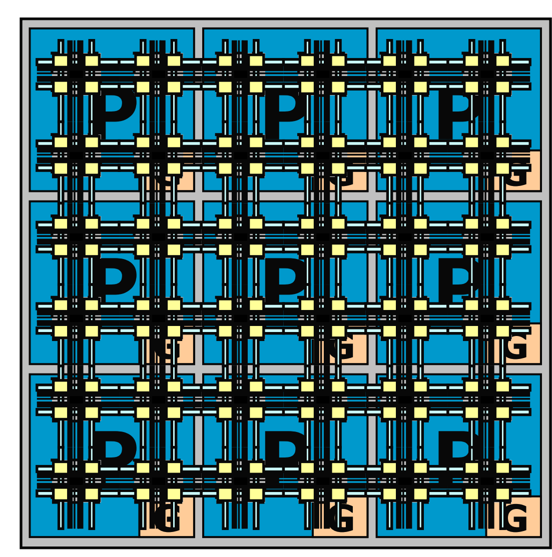
- Memory on logic
- Communication networks: NoC
- Heterogeneous 3-D Systems
- Heterogeneous 3-D systems: free-space optics
- ***Heterogeneous 3-D systems: optical waveguides***

Nanophotonic Interconnected Design Driver



Photonic On-Chip Network

- **Goal: Design a NoC for a chip multiprocessor (CMP)**
- Electronics
  - ✓ Integration density → abundant buffering and processing
  - ✗ Power dissipation grows with data rate
- Photonics
  - ✓ Low loss, large bandwidth, bit-rate transparency
  - ✗ Limited processing, no buffers
- Our solution – a hybrid approach
  - Data transmission in a photonic network
  - Control in an electronic network
  - Paths reserved before transmission → No optical buffering

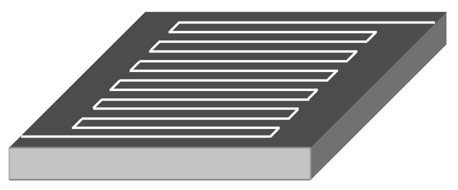


K. Bergman, "Nano-Photonic Interconnection Networks for Chip-Multiprocessor Computing Systems."

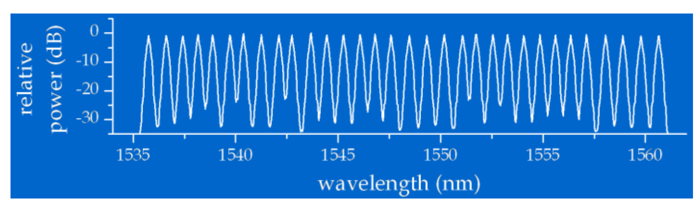
Key Building Blocks

LOW LOSS BROADBAND NANO-WIRES

5cm SOI nanowire



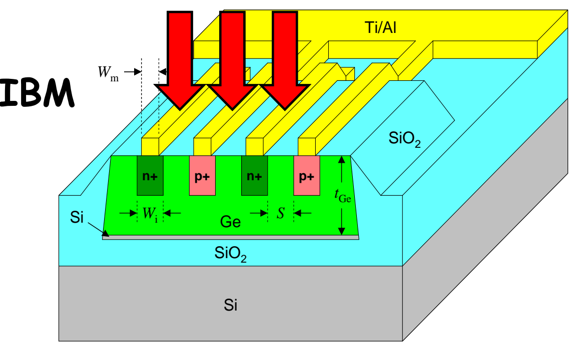
1.28Tb/s (32 λ x 40Gb/s)



IBM/Columbia

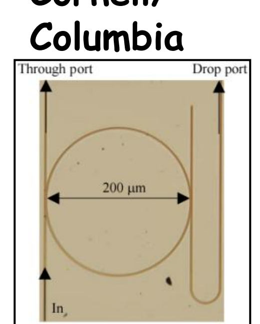
HIGH-SPEED RECEIVER

IBM

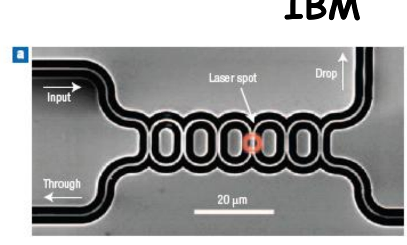


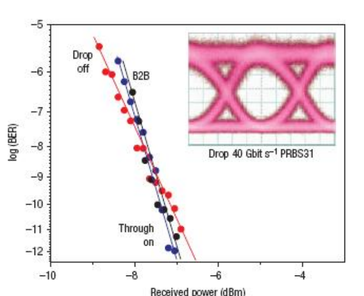
BROADBAND MULTI-λ ROUTER SWITCH

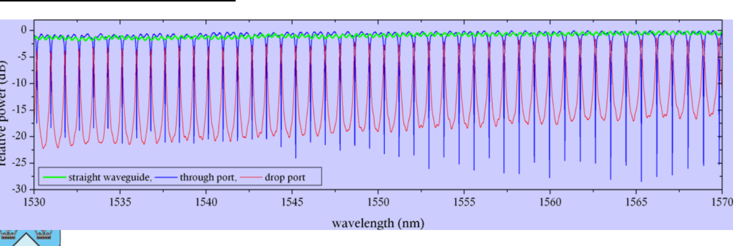
Cornell/ Columbia



IBM

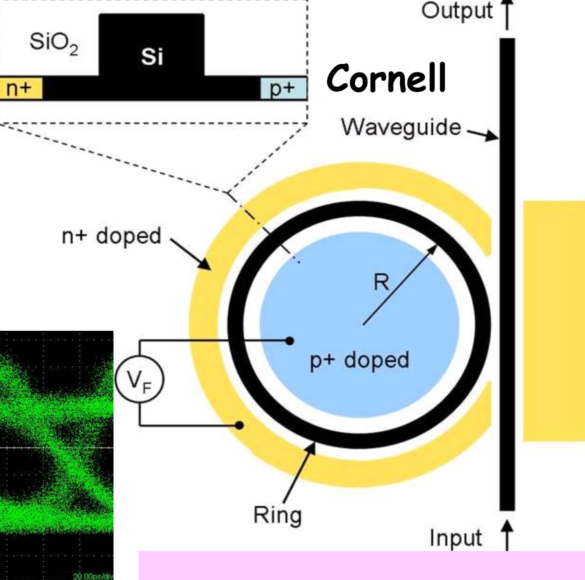






HIGH-SPEED MODULATOR

Cornell

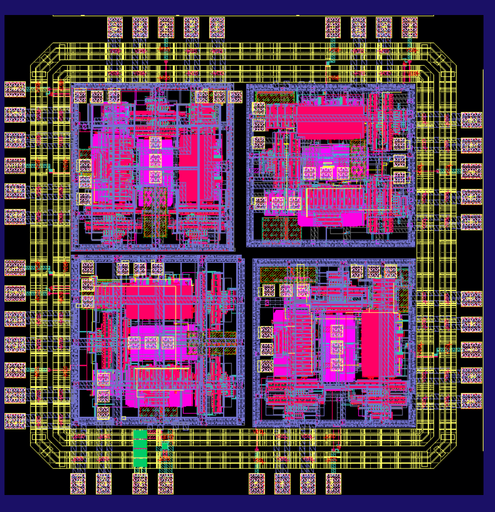


Presentation Outline

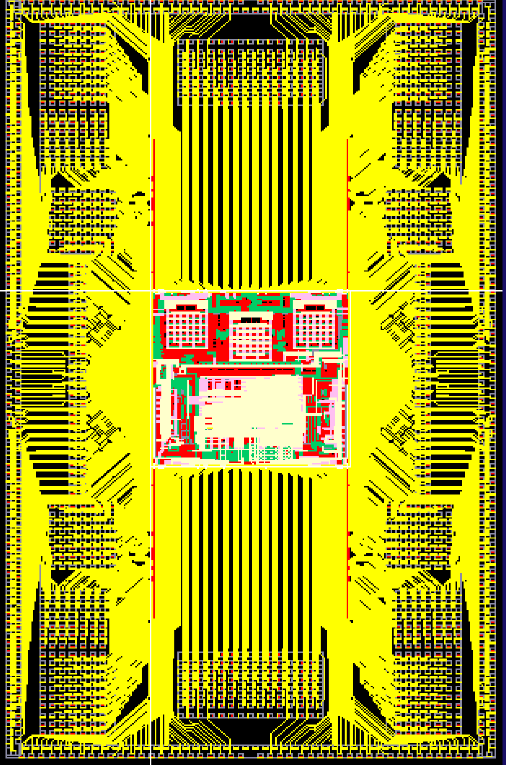
- Three-dimensional (3-D) integration
- Physical design techniques
- TSV modeling
- Design methodologies and flow
- 3-D architectures
- ***Rochester test chips – past, present, and future***
- Conclusions

Rochester 3-D Test Chips

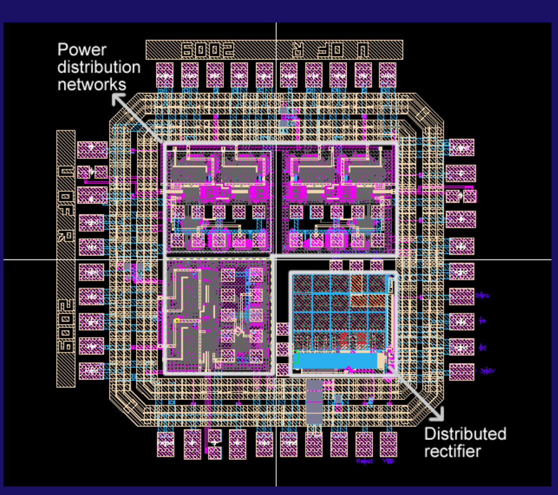
Past



Future

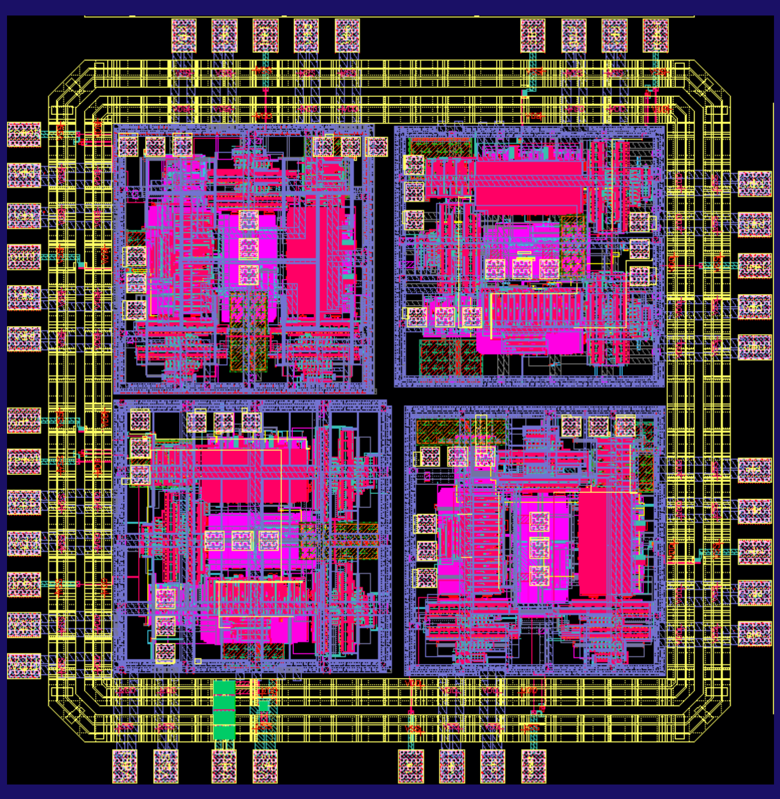


Present



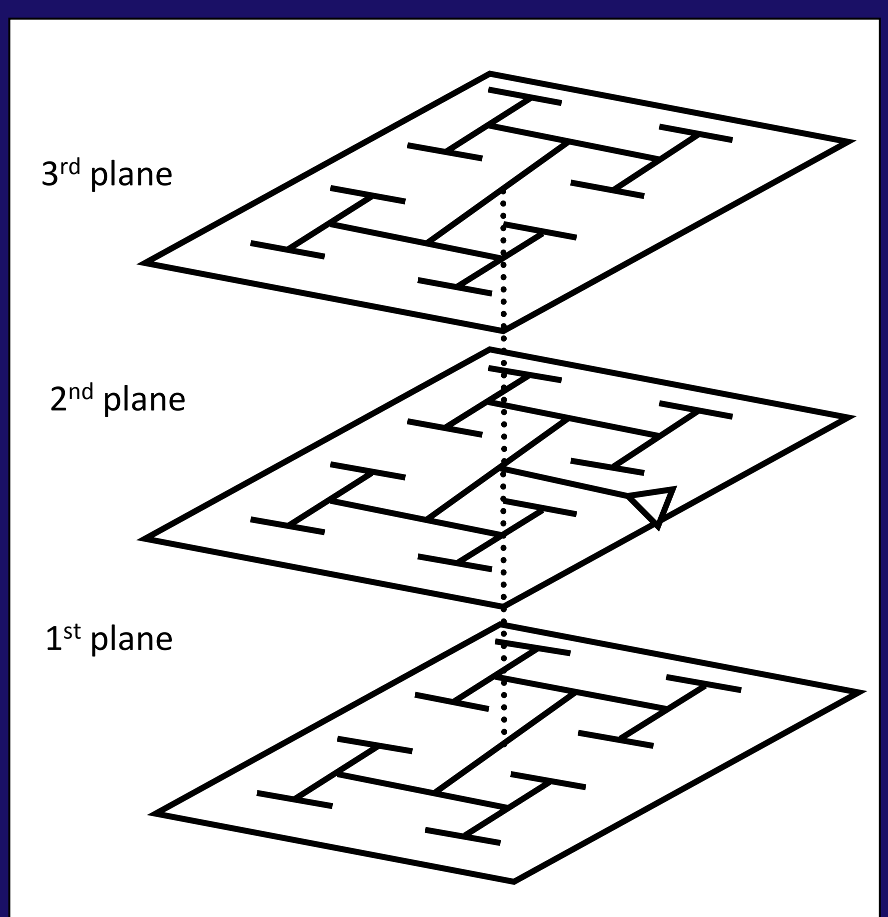
Rochester 3-D Test Chips

Past



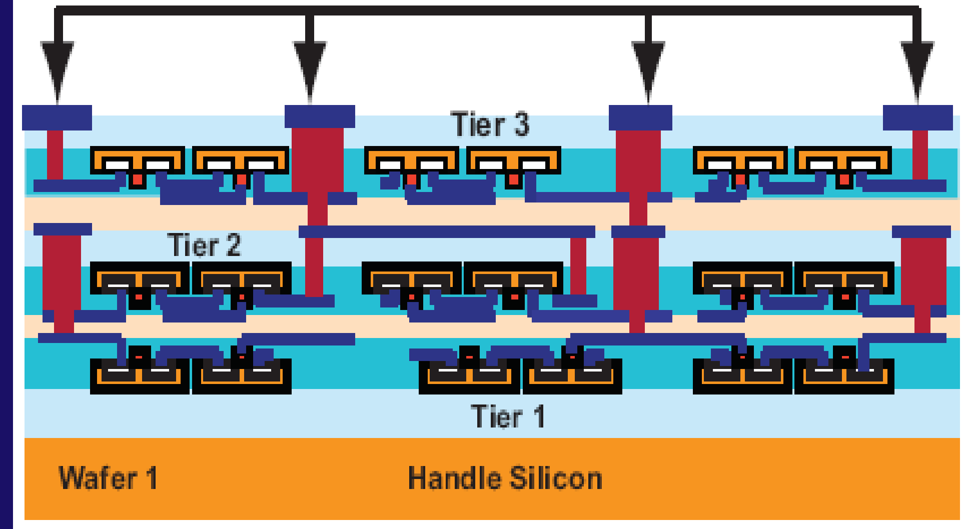
Clock Signal Distribution for 3-D ICs

- Multiplane system
  - Process variations
- Different forms of 3-D integration
  - System-in-Package (SiP)
  - 3-D ICs (high density vias)
- Clock signal distribution under pronounced thermal effects



MIT Lincoln Laboratories 3-D IC Fabrication Process

- FDSOI 180 nm CMOS process
  - Three plane process
  - Three metal layers for each plane
  - Back side metal layer for planes 2 and 3
  - One polysilicon layer
- 1.75 µm × 1.75 µm cross section of TSVs
  - For the 2nd 3-D multiproject

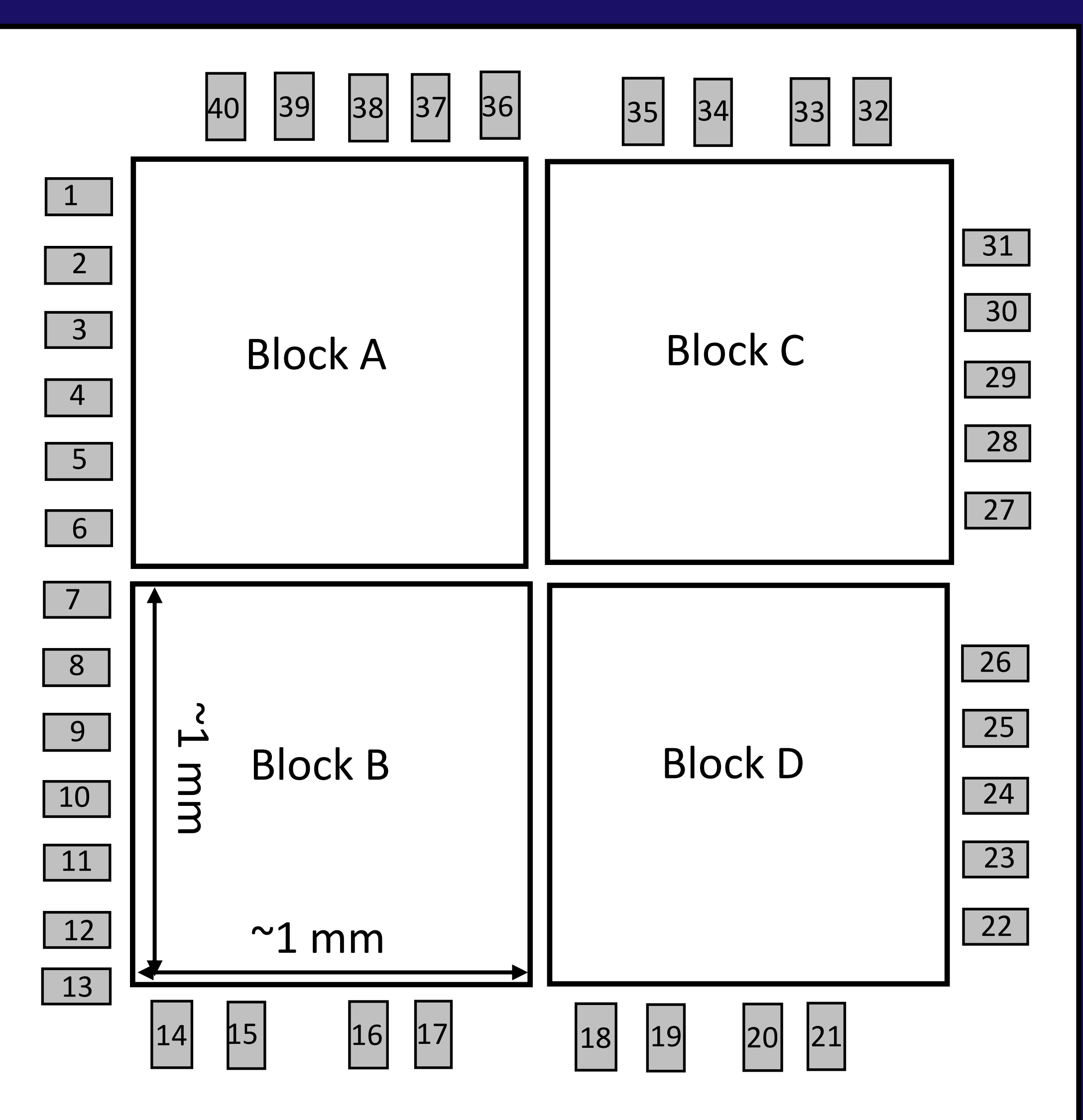


- Planes one and two
  - Face to face bonding
- Planes two and three
  - Back to face bonding

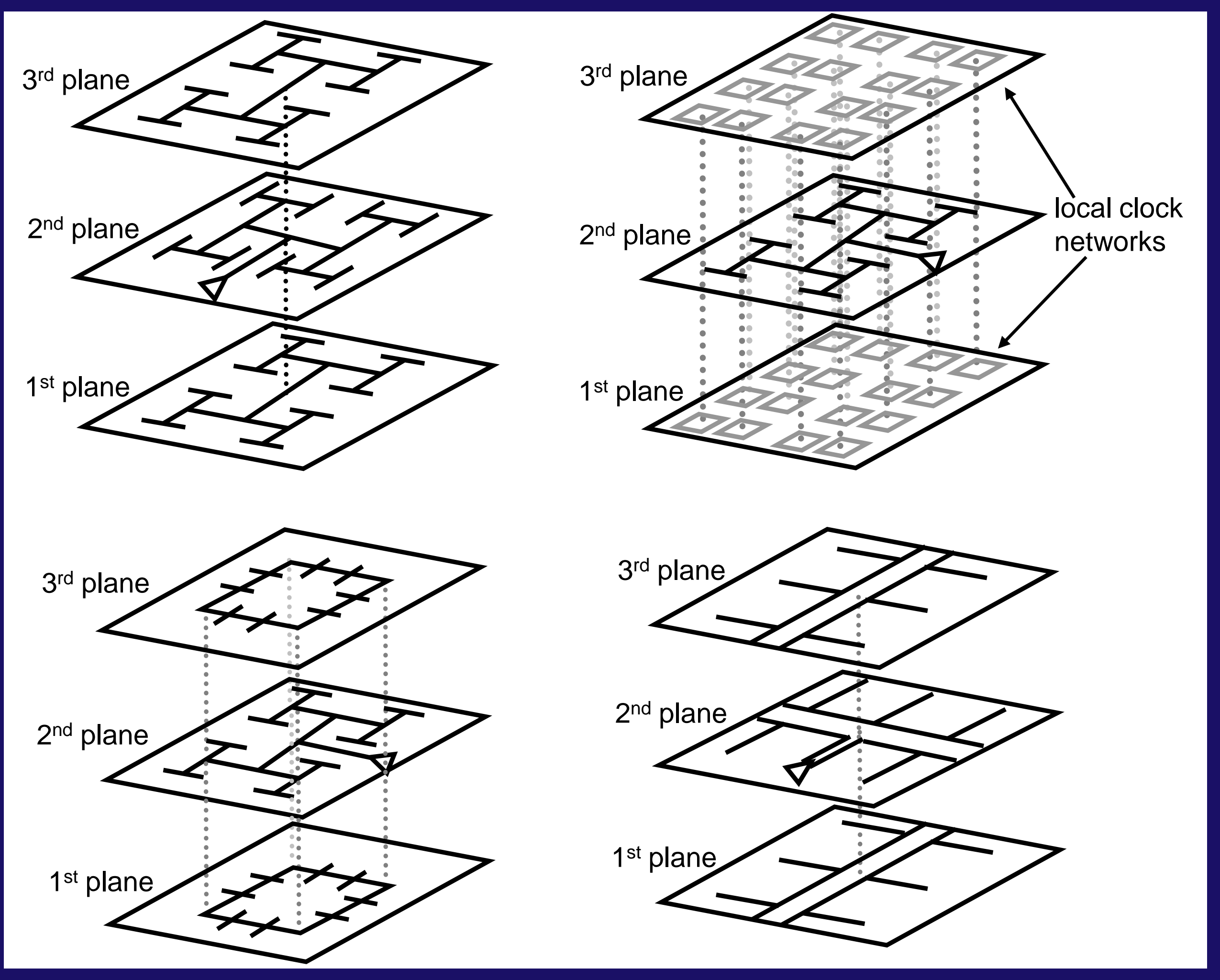
*Massachusetts Institute of Technology Lincoln Laboratory, *FDSOI Design Guide*

Block Diagram of the 3-D Test Circuit

- Each block includes
  - Identical logic
  - Different clock distribution network
- Objectives
  - Evaluate clock skew
  - Measure power consumption
- Area - 3 mm × 3 mm

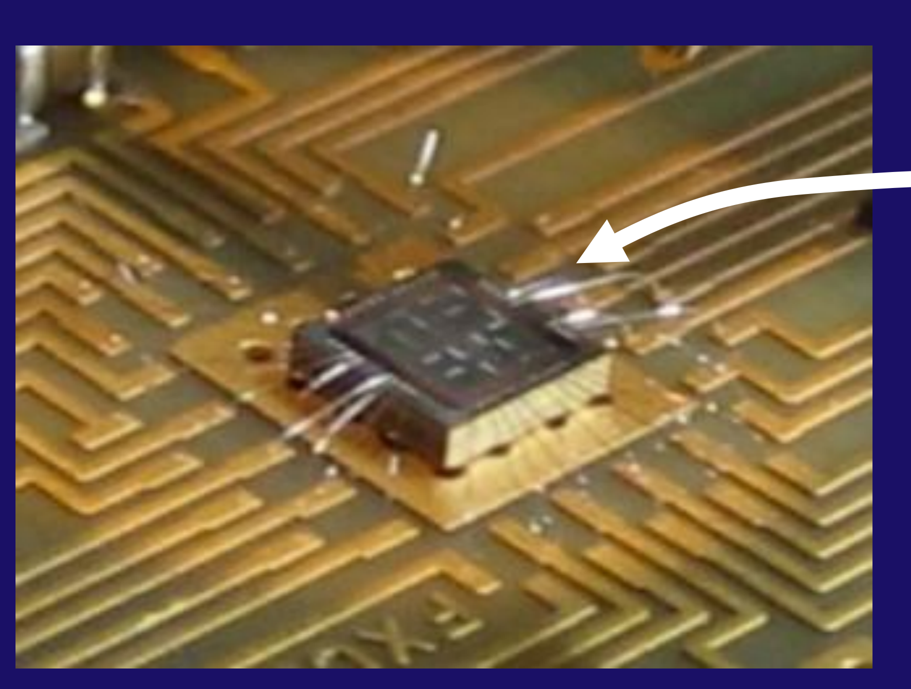


3-D Clock Distribution Networks



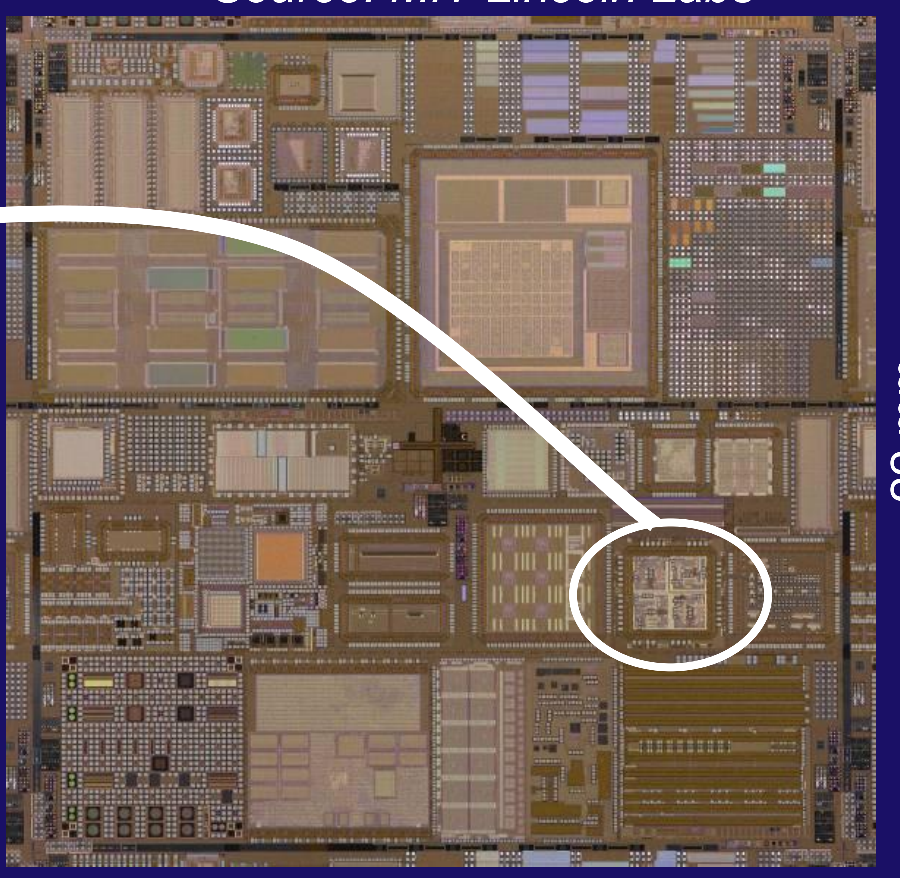
- The clock network on the 2nd plane is rotated by 90° to eliminate inductive coupling

“The Rochester Cube”



3DM2 Die Photo

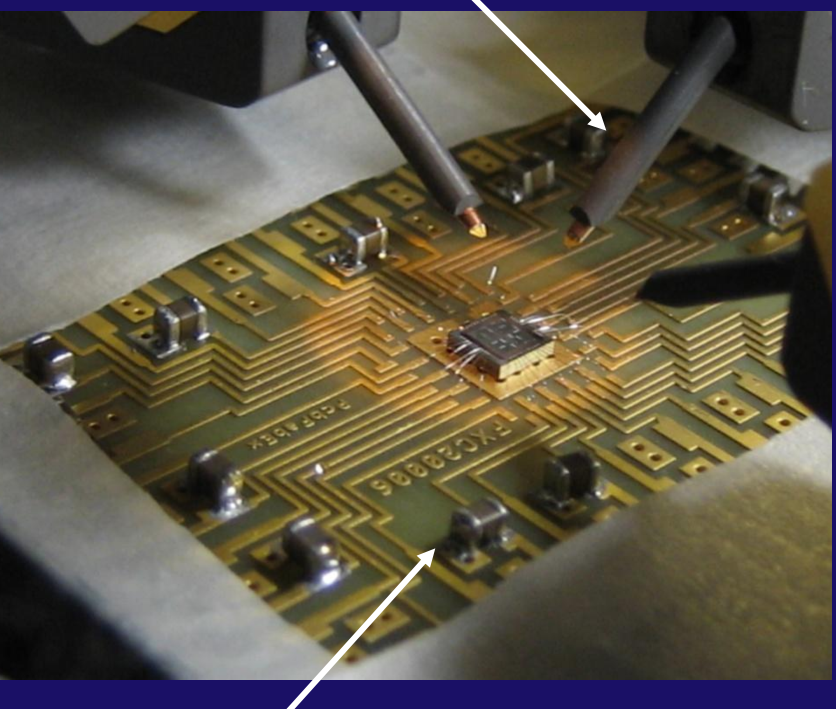
Source: MIT Lincoln Labs



- 20 participants
  - Industry, universities, laboratories
- 30 prototype circuits

Fabricated 3-D Test Circuit

RF probe



Decoupling capacitor

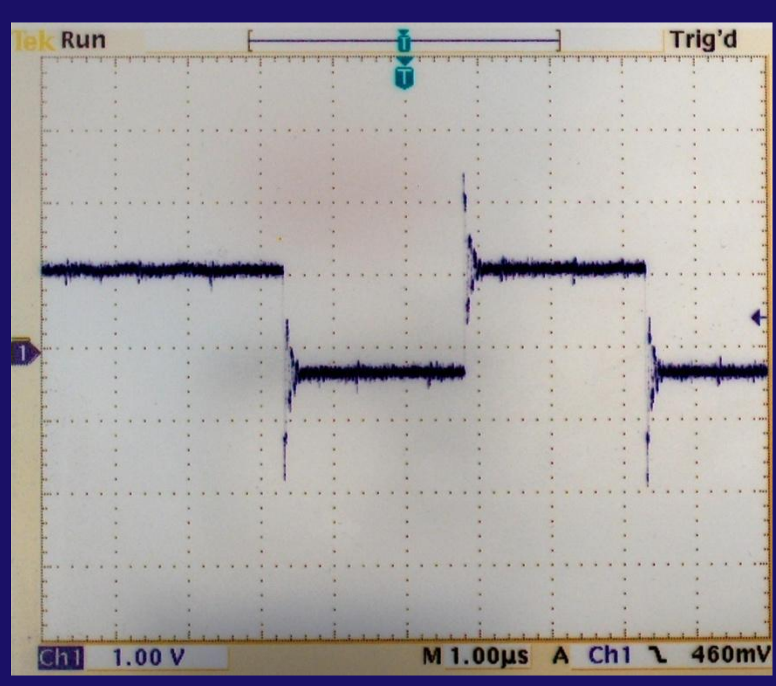
RF pads

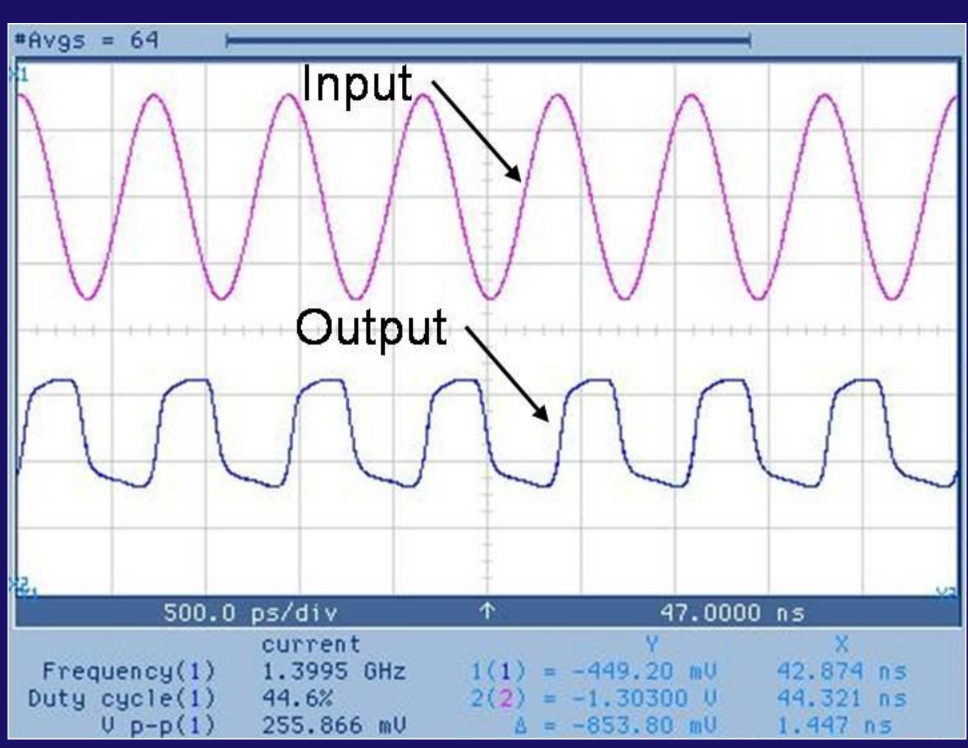
Clock input

Clock output on the 3rd plane

- Full custom design
- ~ 120K transistors

Clock and Data Waveforms



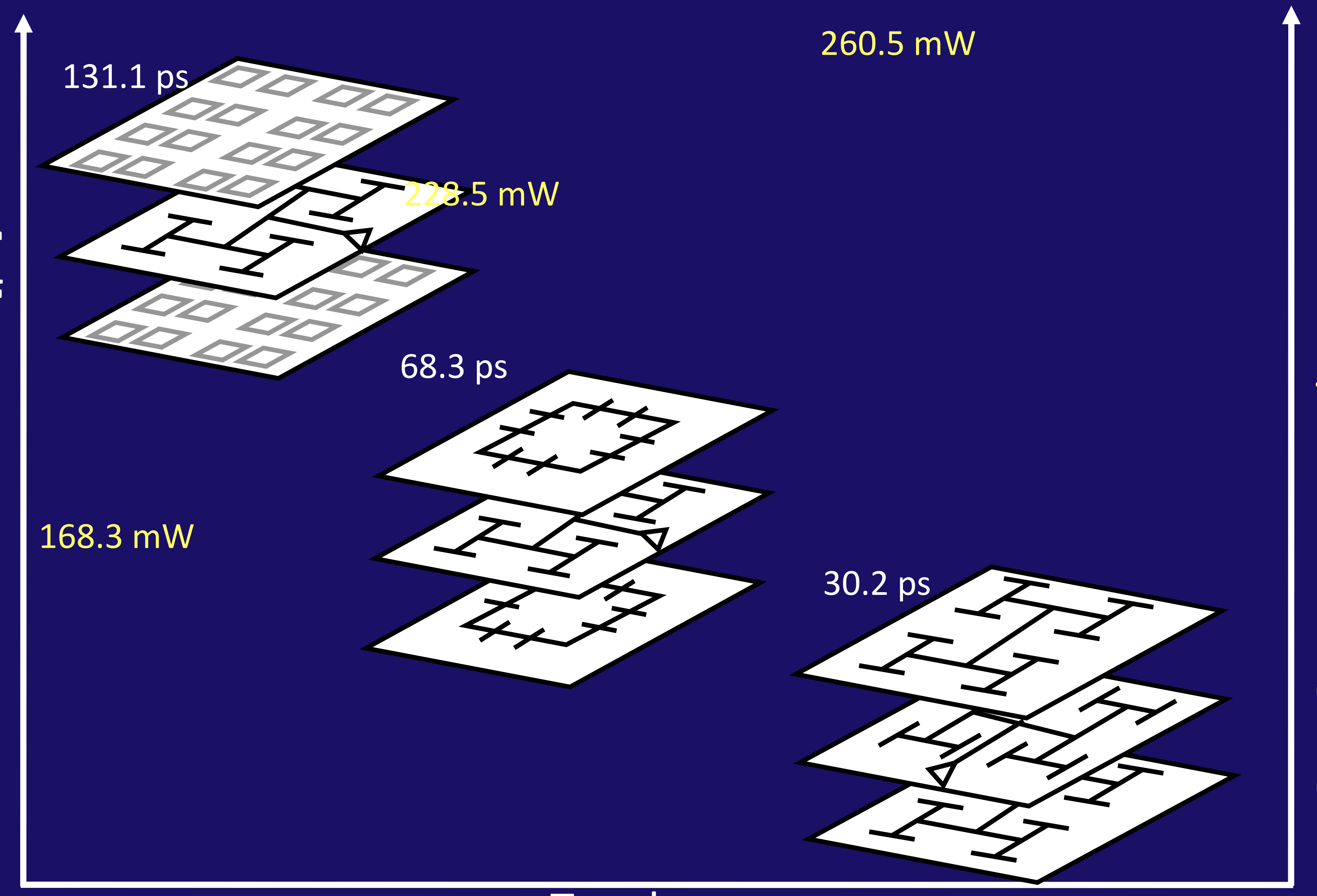


- Output bit at 1 MHz

- Clock output at 1.4 GHz from the 3rd plane

V. F. Pavlidis and E. G. Friedman, "Interconnect-Based Design Methodologies for Three-Dimensional Integrated Circuits," *Proceedings of the IEEE,* Vol. 97, No. 1, pp. 124 – 140, January 2009.

Clock Skew and Power Measurements



V. F. Pavlidis, I. Savidis, and E. G. Friedman, “Clock Distribution Networks for 3-D ICs,” *Proceedings of the IEEE International Custom Integrated Circuits Conference,* September 2008

Clock Slew: Rise and Fall Times

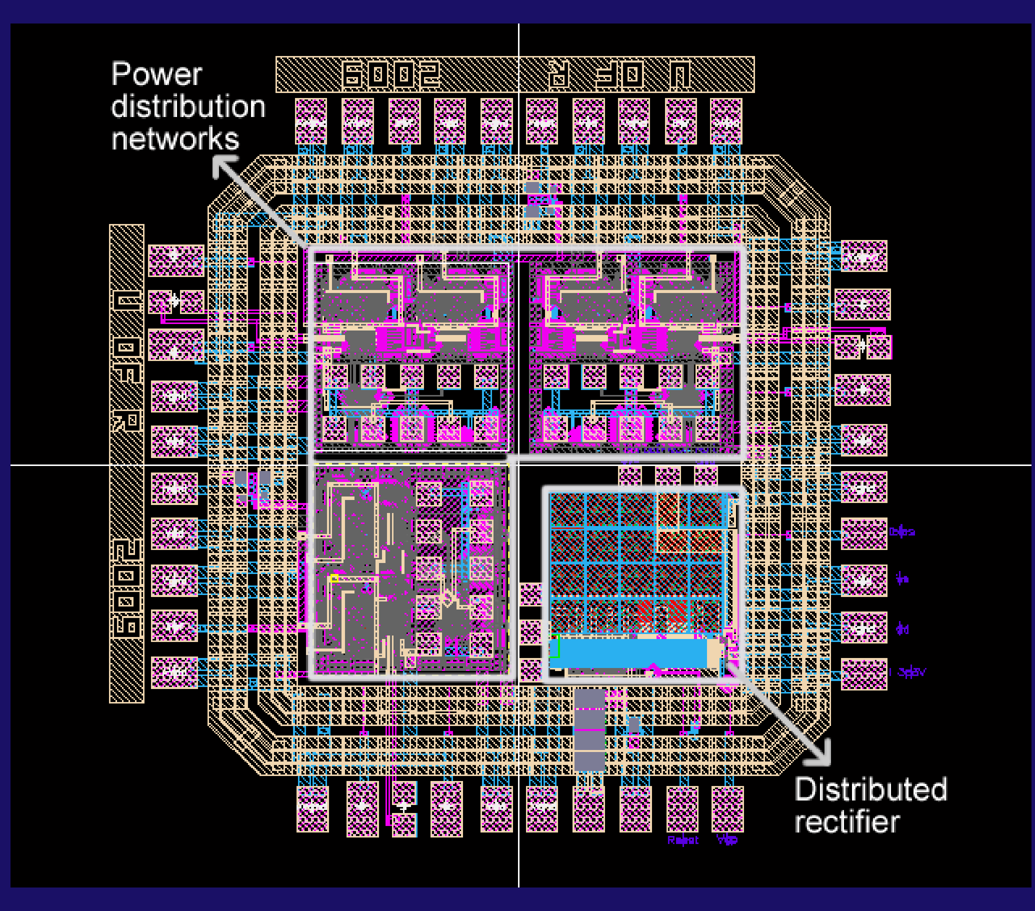
Topology	*Rise time (20% to 80%)* [ps]				*Fall time (80% to 20%)* [ps]			
	Plane A	*Plane B*	*Plane C*	*Avg.*	*Plane A*	*Plane B*	*Plane C*	*Avg.*
H-trees	92.5	98.3	164.2	118.3	116.9	194.7	210.0	173.9
Local rings	91.0	79.1	127.3	99.1	85.7	90.6	284.5	153.6
Global rings	108.7	101.3	108.4	106.1	104.0	59.3	83.8	82.4

- Undershoots during falling edge increase significantly as compared to rise time
- Mismatch between size of devices in clock buffers also contributes to unbalanced clock edges

*Unpublished data

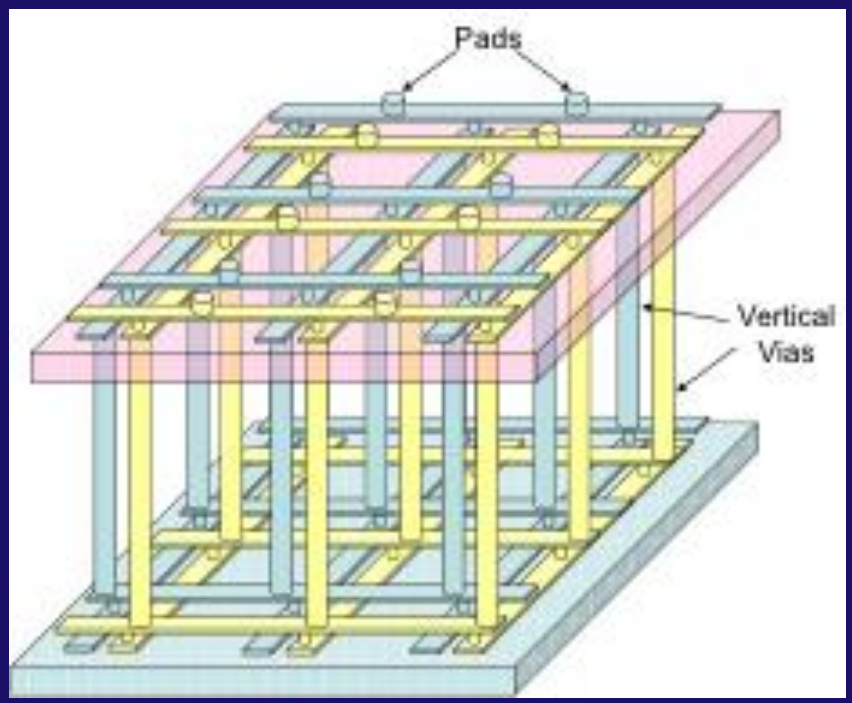
Rochester 3-D Test Chips

Present



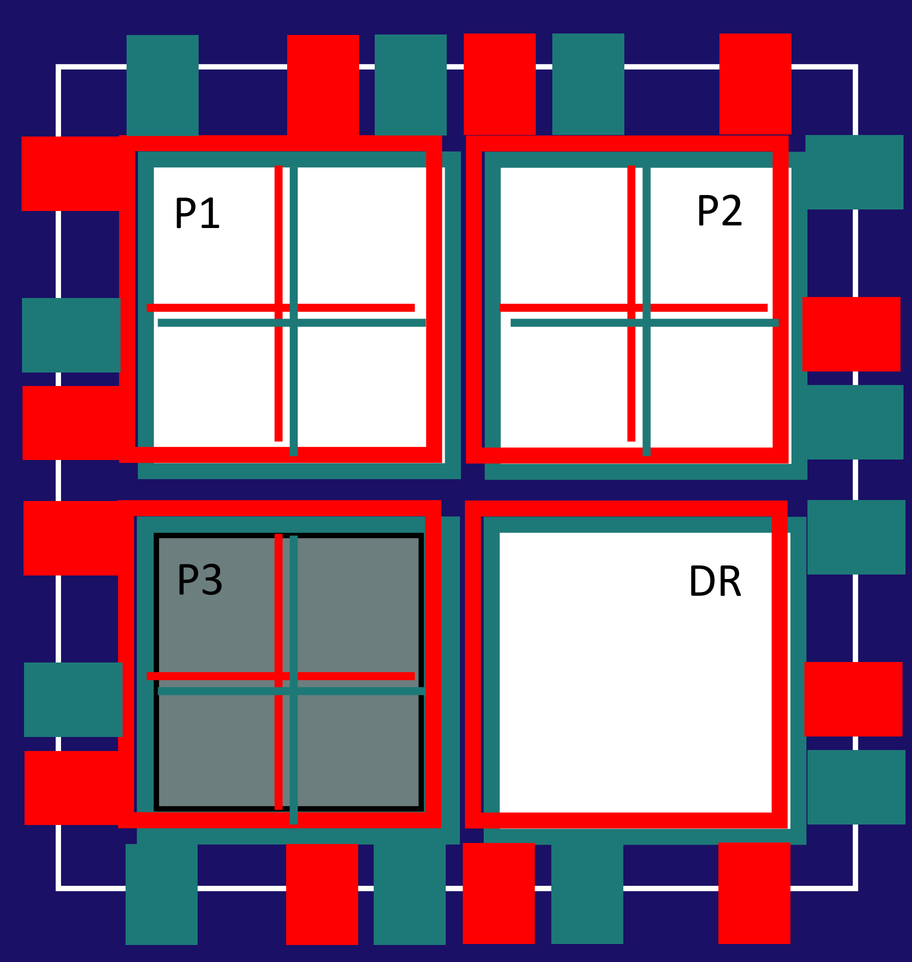
Test Circuits for 3-D Power Delivery

- Different power distribution topologies
- Several TSV placement schemes examining effect of via density on power delivery
- Power generation
  - On-chip distributed power converters
  - Distributed rectifier circuit

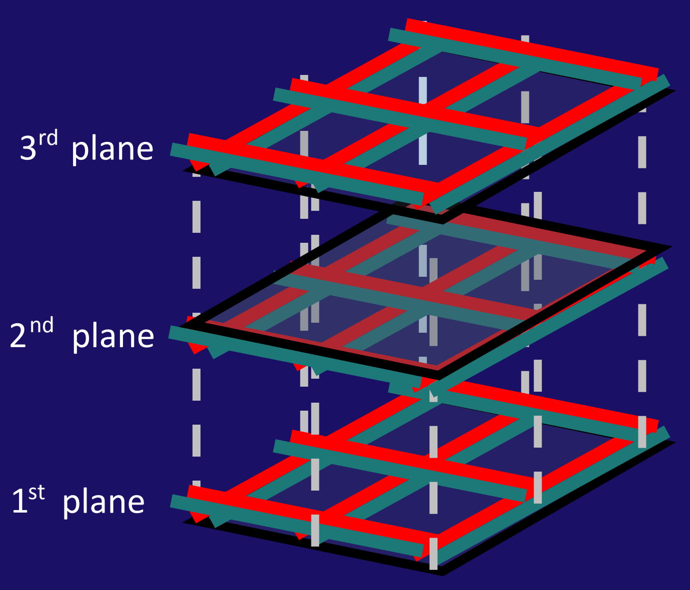


Power Delivery Test Chip
Design Objectives

- Blocks P1 - P3
  - Three different power distribution networks
  - Investigate variations in noise for each power network
- Block DR
  - Distributed rectifier circuit for application to DC-to-DC buck converters

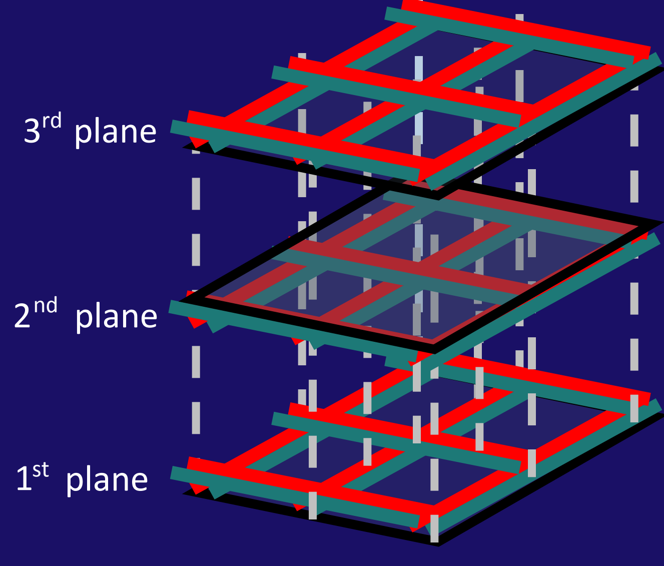


Power Distribution Network Topologies for 3-D ICs



P1: interdigitated

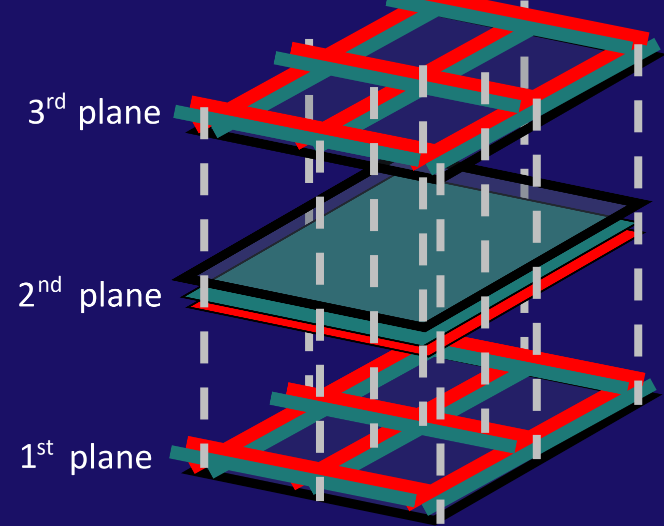
- 3-D vias on periphery



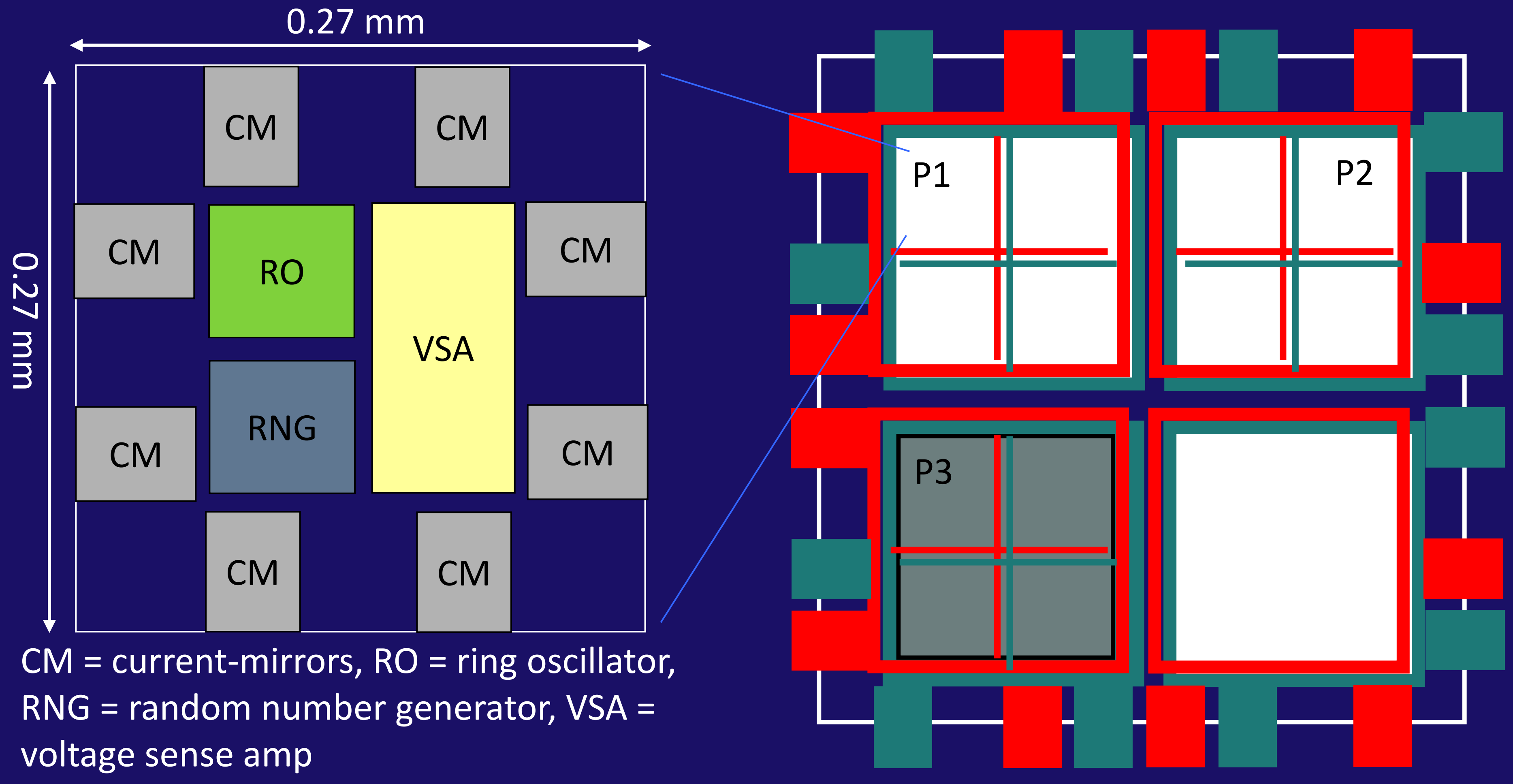
P2: interdigitated

- 3-D vias on periphery and through middle

P3: gnd planes on plane 2, interdigitated on planes 1 and 3



Noise Detection Circuitry

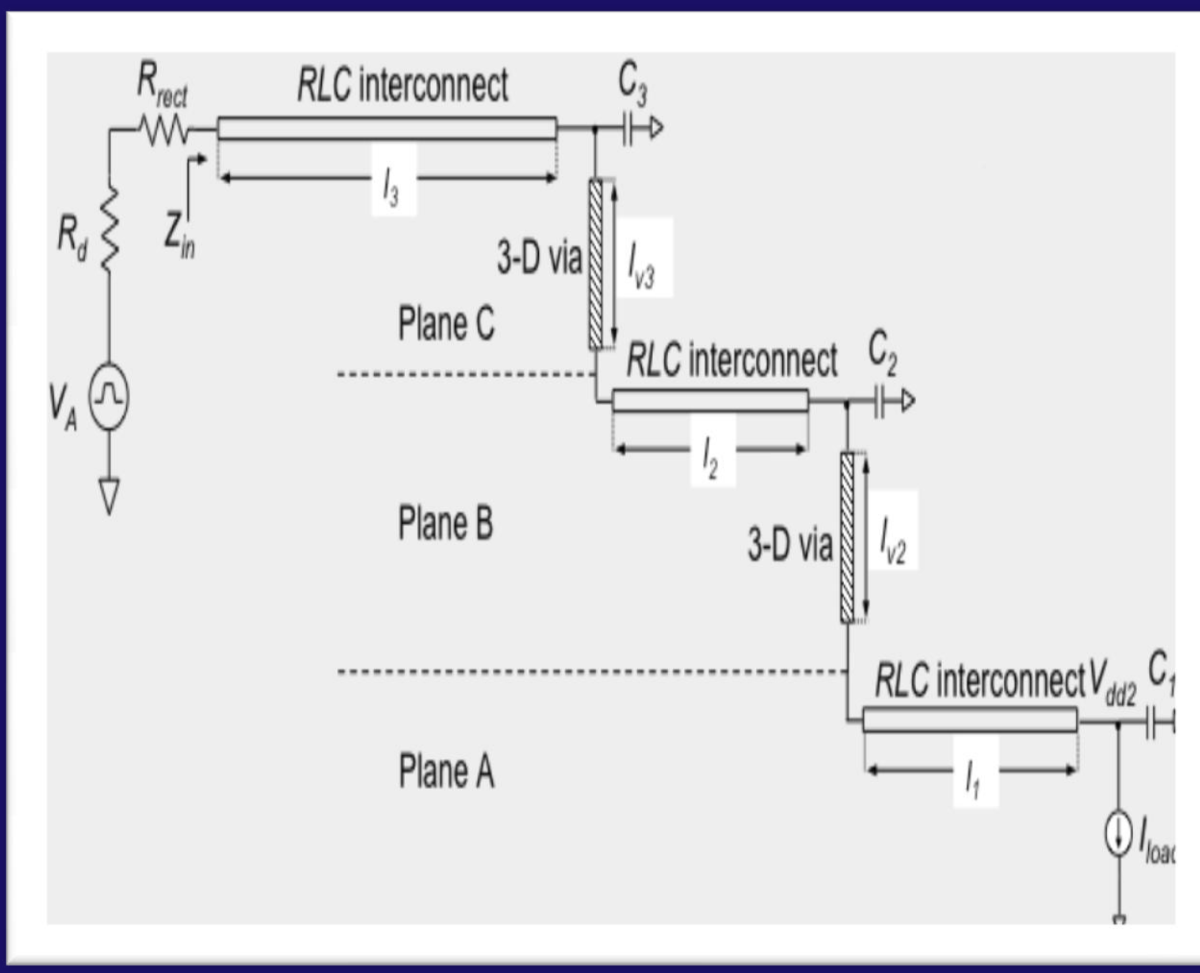


CM = current-mirrors, RO = ring oscillator, RNG = random number generator, VSA = voltage sense amp

- Voltage sense amps are used to detect and measure noise on each plane for each power distribution topology
  - Noise analyzed on both V_{DD} and ground lines

Distributed On-Chip Rectifier

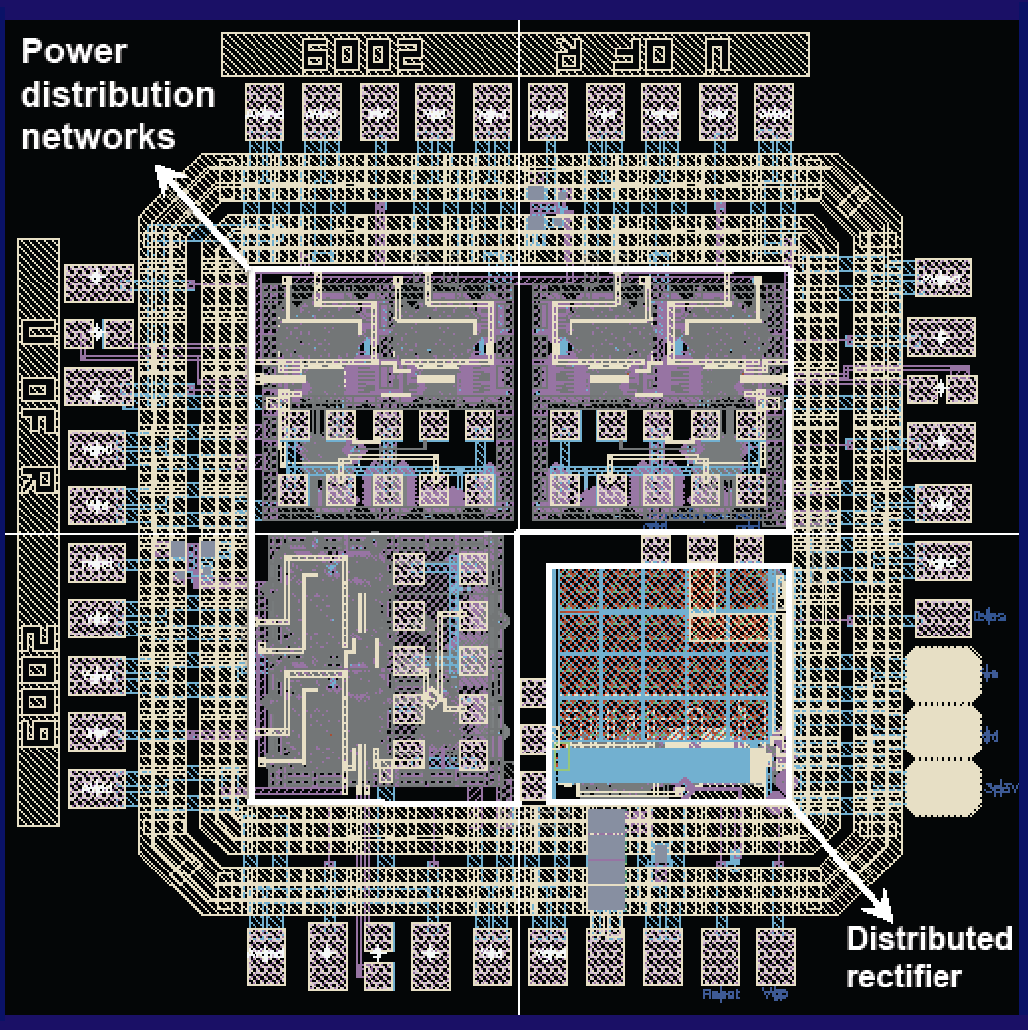
- Exploits rectifier portion of buck converter
  - Generates and distributes power supplies in 3-D integrated circuits
  - Eliminates need for on-chip inductors
- Rectifier is composed of transmission lines
  - Terminated with lumped capacitances
- Inter-plane structure is connected by 3-D TSVs
- Low pass behavior
  - *RC*-like characteristics
  - Sharp roll-off
    - Due to distributed nature



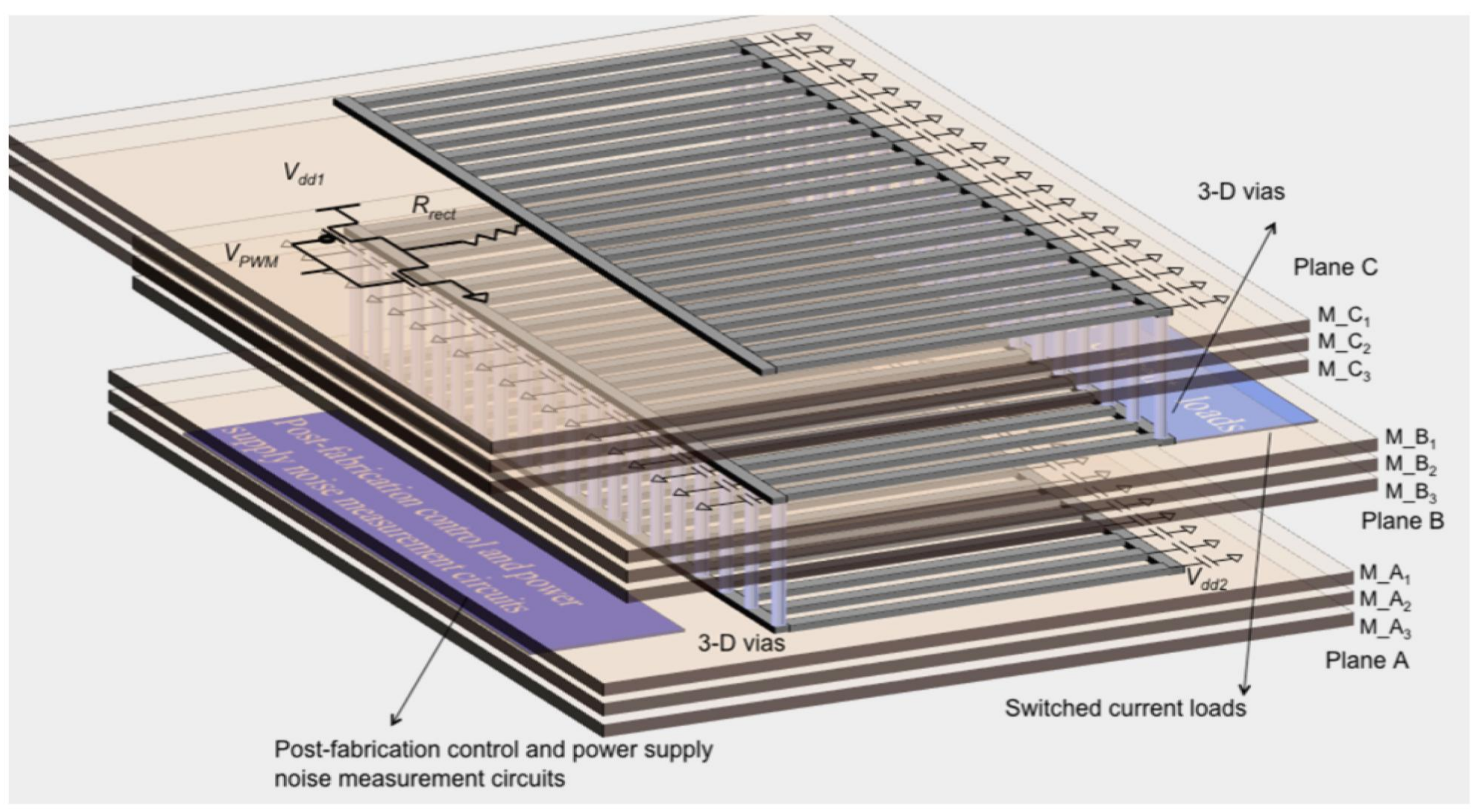
J. Rosenfeld and E. G. Friedman, "'On-Chip DC-DC Converters for Three-Dimensional ICs," *Proceedings of the IEEE International Symposium on Quality Electronic Design,* March 2009.

Power Delivery Test Circuit

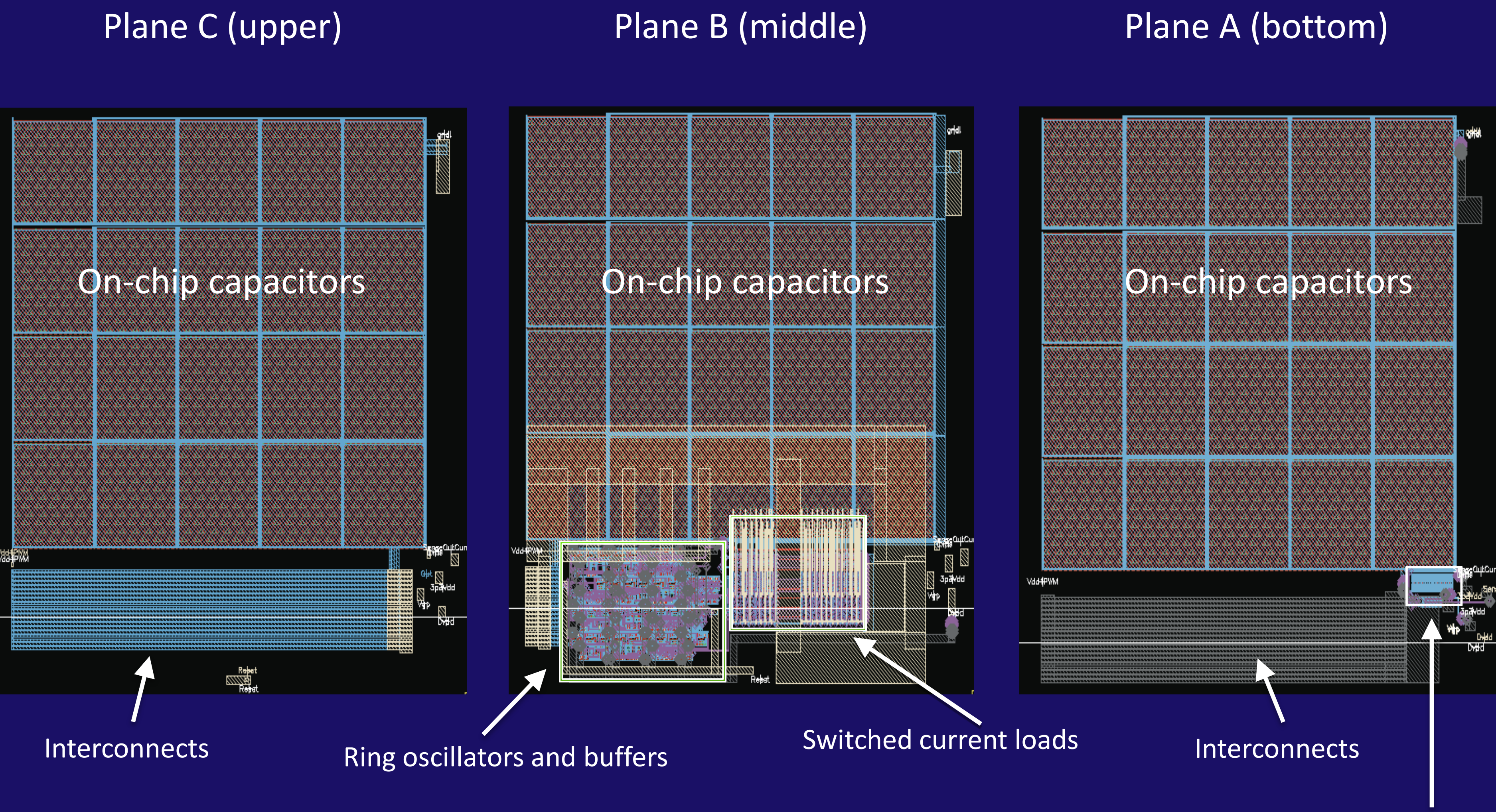
- Lincoln Lab 3-D CMOS process
  - 150 nm FDSOI
  - Three physical planes
  - Three metal layers per plane
  - Back side metal on top two planes
  - Each wafer is separately processed
- 1.25 μm × 1.25 μm cross section of TSVs
- Planes one and two
  - Face to face bonding
- Planes two and three
  - Back to face bonding



Schematic Structure of 3-D Rectifier

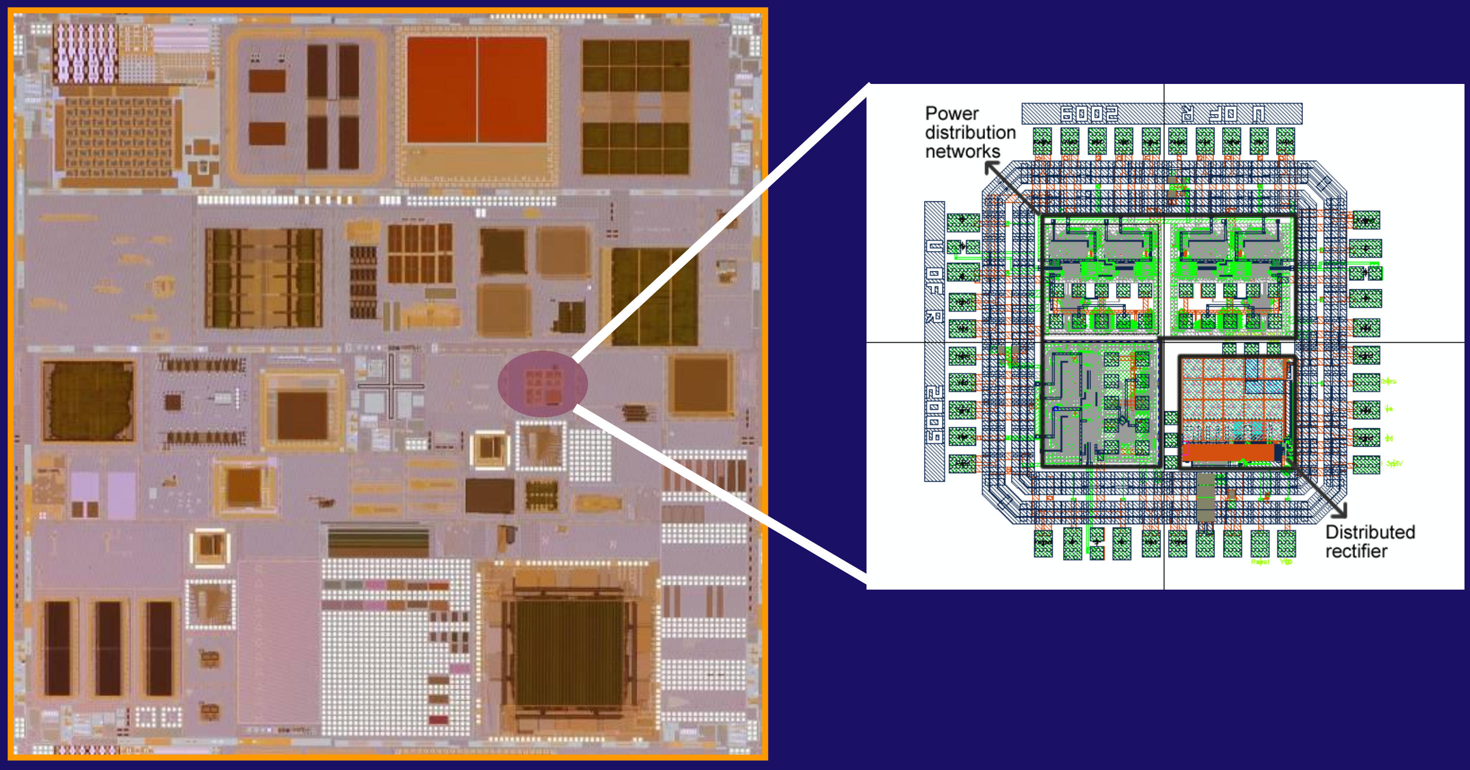


Physical Layout of Distributed Rectifier



MITLL 3-D IC Multiproject Run

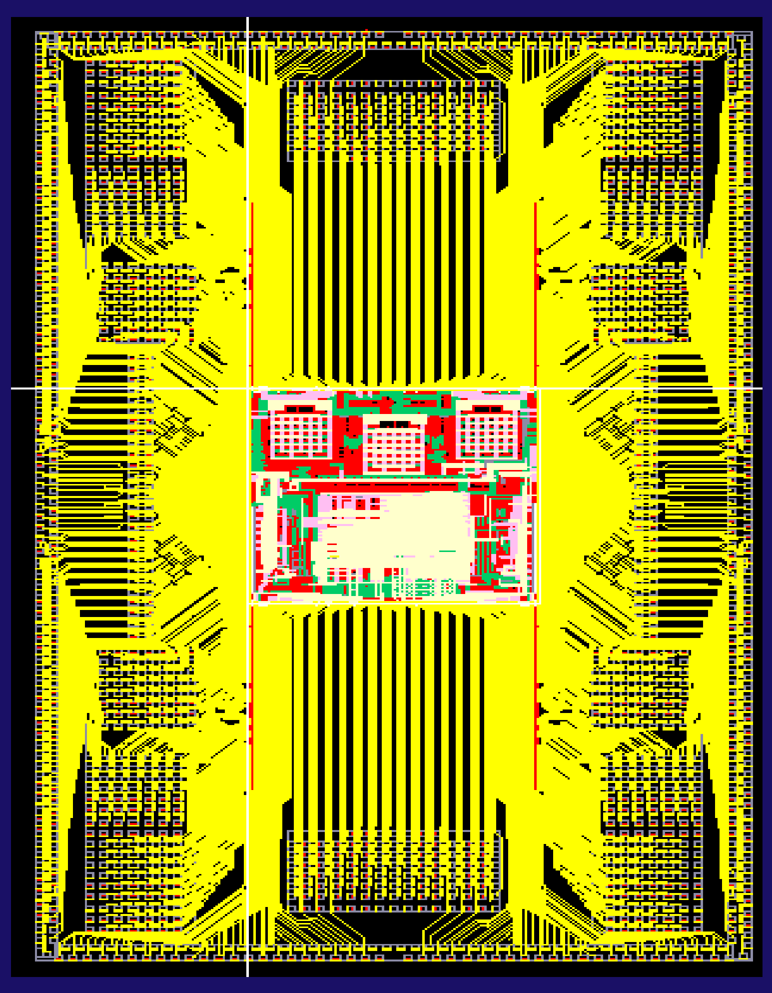
3DM3 T1 Die Photo
Source: MIT Lincoln Labs



- 25 participants
    - Industry, universities, laboratories
- 39 prototype circuits

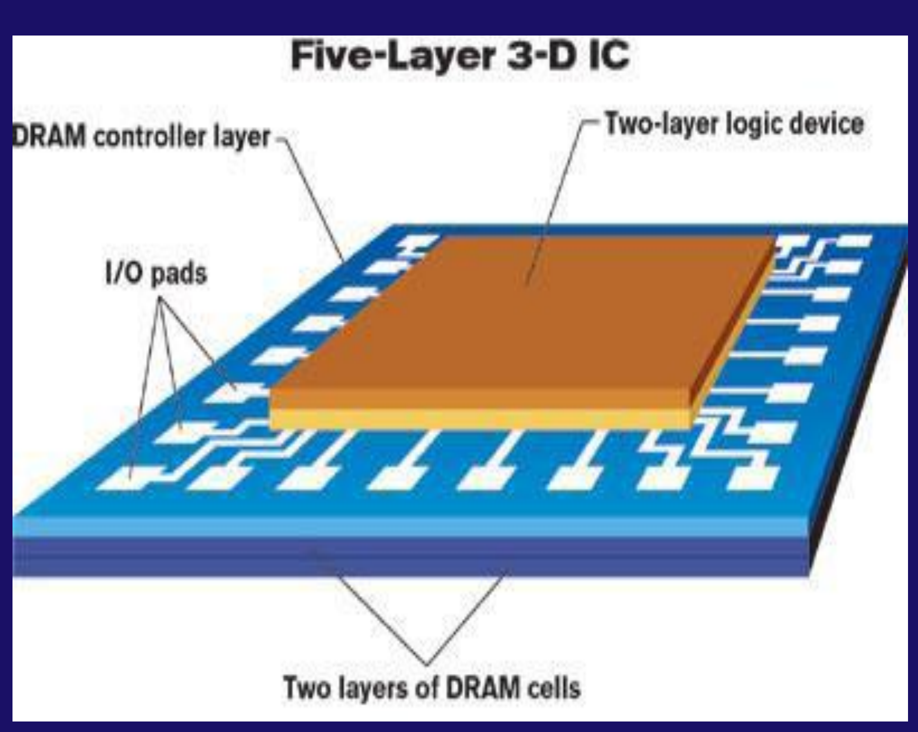
Rochester 3-D Test Chips

Future



Tezzaron: 3-D Logic on Memory Multi-Project Wafer (MPW)

- Two logic layers
  - 130 nm process
  - 6 metal levels per plane
    - 5 metals for interconnect
    - Metal 6 for face-to-face bonding
  - 5 x 5 mm^2
  - Wafer-to-wafer bonded
- One DRAM controller layer
  - ~ 800 I/O pads for communication with outside world
- Two layers DRAM cells
  - Proprietary technology
  - 1 Gbit data per plane
- Logic bonded to memory by die-to-wafer process



MPW

Full Frame

Test chips:
TX, TY
2.0 x 6.3 mm

Subreticules:
A, B, C, D, E, F, G, H, 1, 2
5.5 x 6.3 mm

Notice Symmetry about vertical center line

Top tiers

DARPA MPW

DARPA Seedling Program

30.4mm

Collaboration with R3Logic and NCSU

25.4mm

Twelve 5x5mm sites
Six 2.5x5mm sites
~25 participants

17 will incorporate the 1/2/4Gb 8 port DRAM

One is extending to 4 logic layers

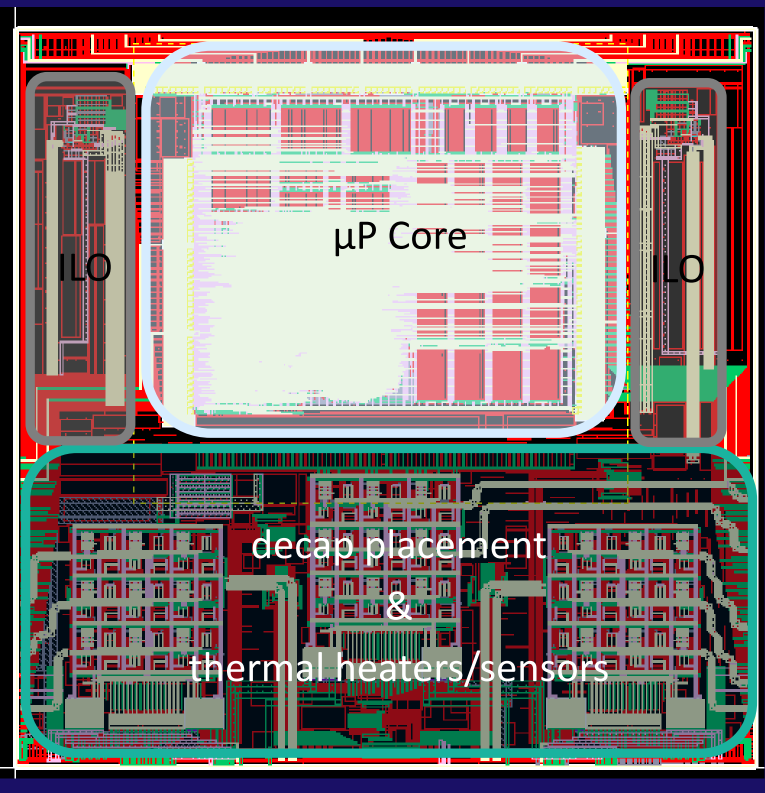
Tezzaron Semiconductor

Next 3-D Test Circuit Projects Tezzaron Logic Planes

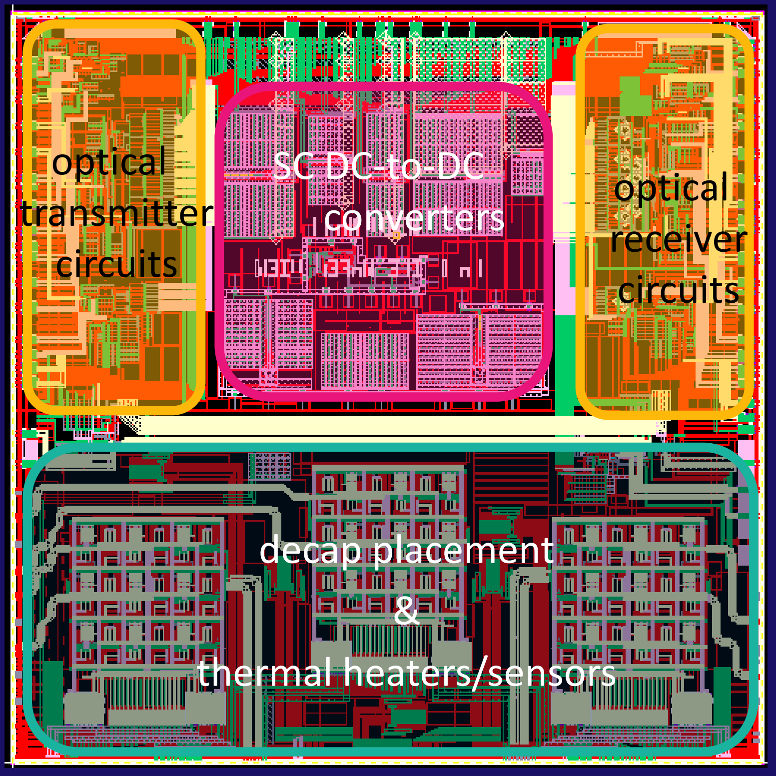
- 3-D free optical system
  - VCSEL driver circuitry (transmitter)
  - Transimpedance amplifier (receiver)
  - Limiting amplifier (receiver)
    - Volt to volt converter
  - Distributed pulse generation circuitry
  - Injection locked clock multiplier
  - Switch capacitor DC-to-DC converter
- 3-D microprocessor
  - Bit-error-rate at different stages of pipeline
  - Cross-plane thermal stressing
- Decap placement in 3-D stack
  - Noise generating circuits
  - V_{dd} and G_{nd} noise detect circuits
- Thermal aware floorplanning
  - Cross-plane thermal coupling
  - Heat generators
  - On-chip thermal sensors

Tezzaron Circuit Breakdown

Top Logic Plane



Bottom Logic Plane

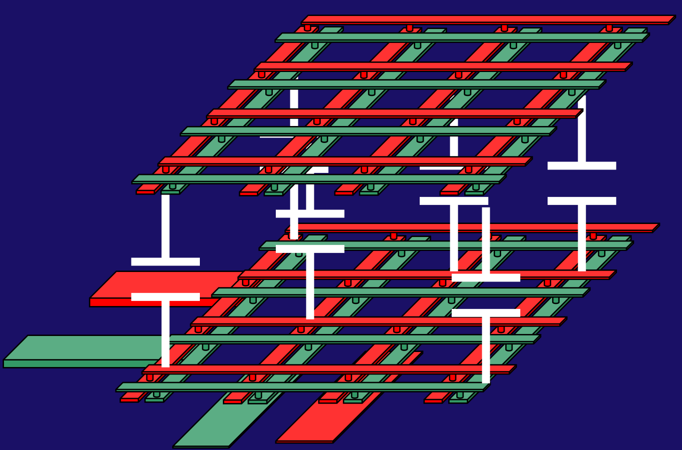


Decap Placement in 3D Stack

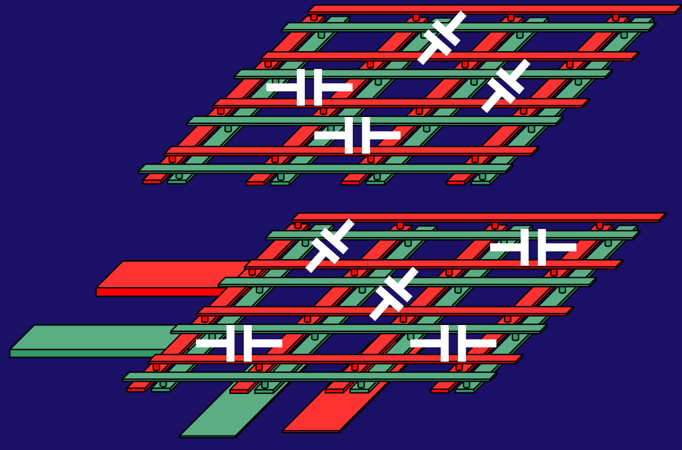
No Decap

Large Decap at Input of PDN

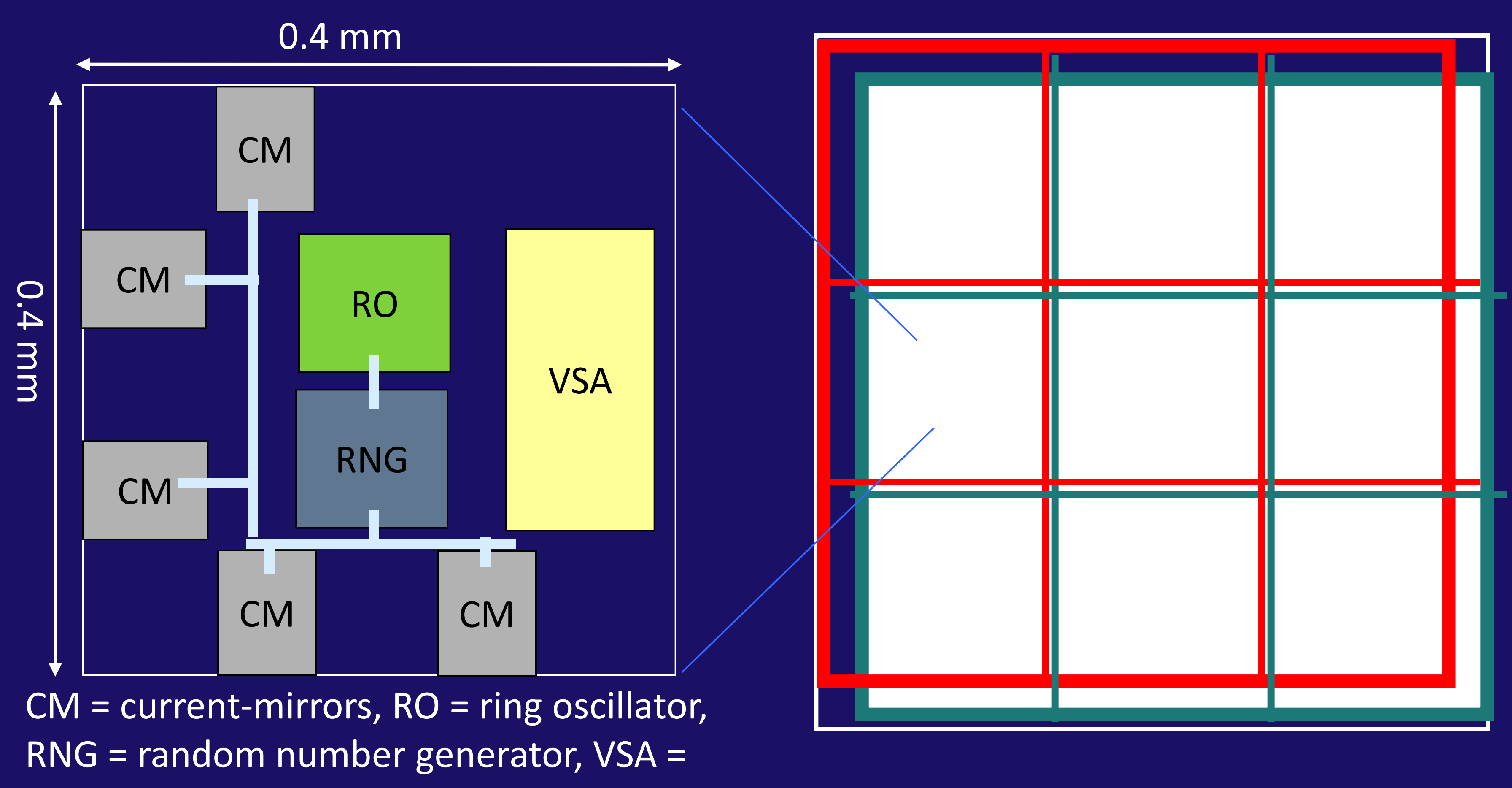
Shared Decap: TSVs or active



Local Decap on each Plane

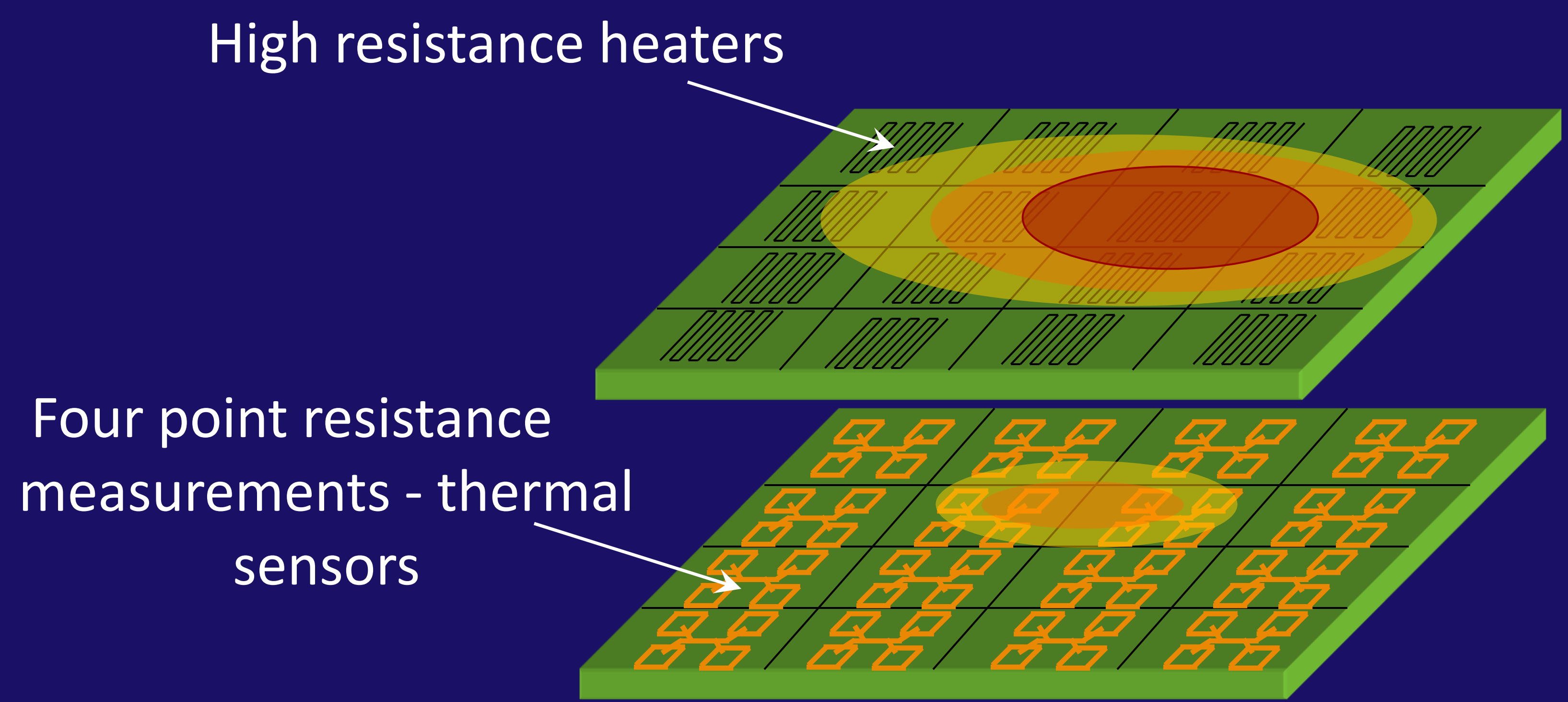


Noise Detection Circuitry



CM = current-mirrors, RO = ring oscillator, RNG = random number generator, VSA = voltage sense amp

Thermal Aware Floorplanning



Note:

1) Thermal sensors may be replaced by diodes or transistor in subthreshold
2) Four point resistance of metal line: metal line should be 5 to 10 ohms to reduce Joule heating
3) Each heater can be activated individually

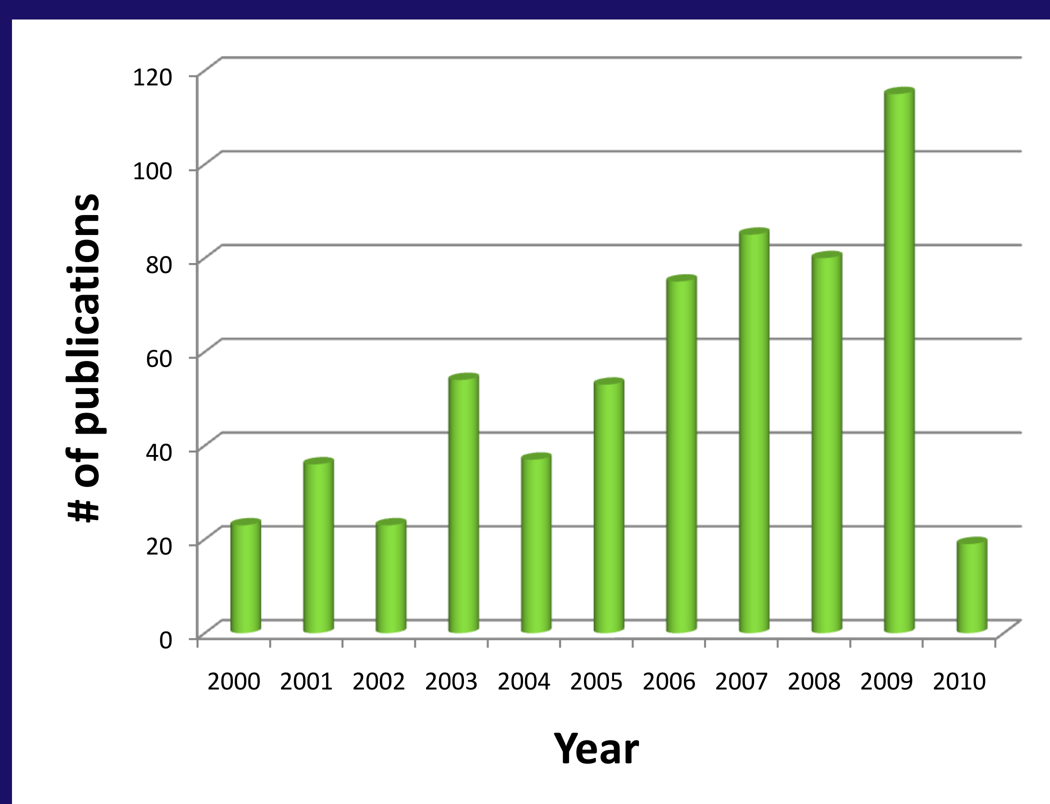
Presentation Outline

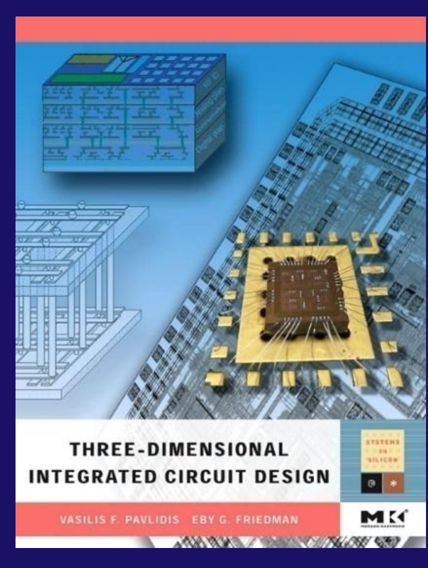
- Three-dimensional (3-D) integration
- Physical design techniques
- TSV modeling
- Design methodologies and flow
- 3-D architectures
- Rochester test chips – past, present, and future
- ***Conclusions***

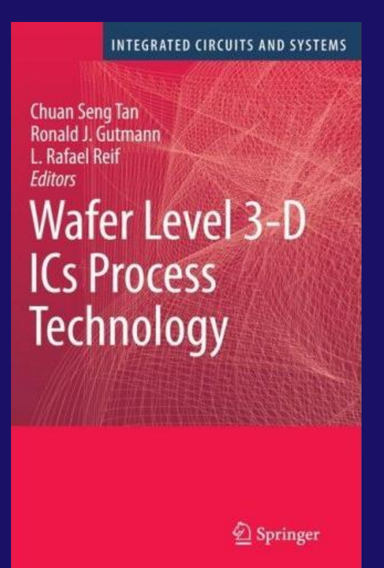
Conclusions

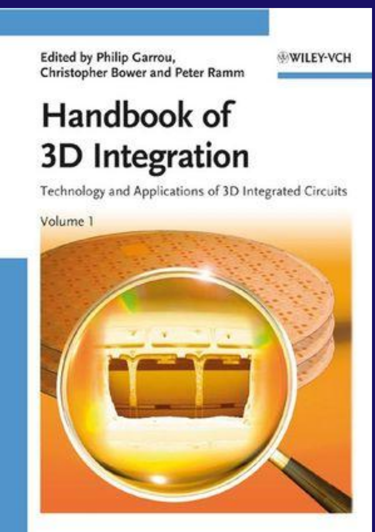
- Three-dimensional integration is a promising solution to expected limits of scaling
- Interplane through silicon vias (TSVs) are the key
- Advanced and novel 3-D architectures are now possible
- Fabricated test circuits are exercising 3-D process, modeling, and design methodologies
- Increasing number of 3-D circuits are under development
  - With products on the way
- 3-D integration is a likely next step in the evolution of semiconductor technology

An Increasing Interest in 3-D ICs









- *Source: IEEEXplore*
- *Search term: 3-D integration*

Geographic Mapping of 3D IC Players

Copyrights © Yole Développement SARL. All rights reserved.

Thank You