Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits

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***Abstract* - A closed form expression for the propagation delay of a CMOS gate driving a distributed *RLC* line is introduced that is within 5% of dynamic circuit simulations for a wide range of *RLC* loads. It is shown that the traditional quadratic dependence of the propagation delay on the length of an *RC* line approaches a linear dependence as inductance effects increase. The closed form delay model is applied to the problem of repeater insertion in *RLC* interconnect. Closed form solutions are presented for inserting repeaters into *RLC* lines that are highly accurate with respect to numerical solutions. An *RC* model as compared to an *RLC* model creates errors of up to 30% in the total propagation delay of a repeater system. Considering inductance in repeater insertion is also shown to significantly save repeater area and power consumption. The error between the *RC* and *RLC* models increases as the gate parasitic impedances decrease which is consistent with technology scaling trends. Thus, the importance of inductance in high performance VLSI design methodologies will increase as technologies scale.**

I. Introduction

It has become well accepted that interconnect delay dominates gate delay in current deep submicrometer VLSI circuits [1]-[5]. Currently, inductance is becoming more important with faster on-chip rise times and longer wire lengths. Wide wires are frequently encountered in clock distribution networks and in upper metal layers. These wires are low resistance wires that can exhibit significant inductive effects. Furthermore, increasing performance requirements are pushing the introduction of new materials for low resistance interconnect [6]. With these trends it is becoming more important to include inductance when modeling on-chip interconnect. Criteria to determine which nets should consider on-chip inductance have been described in [7] and [8].

The focus of this paper is to provide an accurate estimate of the propagation delay of a CMOS gate driving a *distributed RLC* line as well as to develop design expressions for optimum repeater insertion to minimize the delay of a signal propagating along a distributed *RLC* line. The paper is organized as follows. In section II, a simple yet accurate propagation delay formula describing a CMOS gate driving a distributed *RLC* load is presented. In section III, the propagation delay formula is used to develop design expressions for optimum repeater insertion to minimize the propagation delay of a distributed *RLC* line. Some conclusions are offered in section IV. A proof of the expressions for optimum repeater insertion in an *RLC* line is provided in the appendix.

II. Propagation Delay of a CMOS Gate Driving an *RLC* Load

An arbitrary CMOS gate driving an *RLC* transmission line representation of an interconnect line is shown in Fig. 1. R_t, L_t, and C_t are the total resistance, inductance, and capacitance of the line, respectively. The parasitic impedances R_t, L_t, and C_t are given by $R_t = Rl$, $L_t = Ll$, and $C_t = Cl$, respectively, where R, L, and C are the resistance, inductance, and capacitance per unit length of the interconnect and l is the length of the line. R_{tr} is the equivalent output resistance of the gate driving the interconnect. C_L is the input capacitance of the following gate at the end of the interconnect section. A minimum size buffer has an output resistance R_0 and an input capacitance C_0. The input voltage V_{in} is a fast rising signal that can be approximated by a step signal. V_{out} is the far output voltage at the end of the interconnect section.

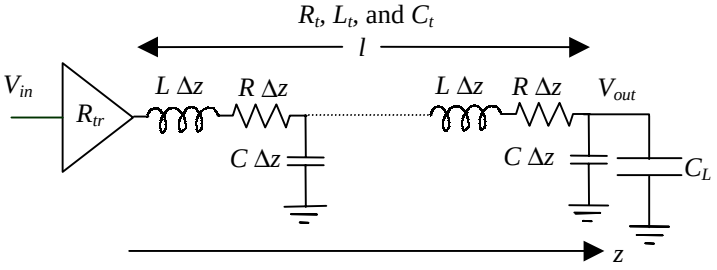

Fig. 1. A CMOS gate driving an *RLC* transmission line.

From the basic principles of a transmission line [12], the voltage transfer function $V_{out}(S)/V_{in}(S)$ at the end of a lossy transmission line with a source resistance z_s and a load impedance z_L is given by

$$\frac{V_{out}(S)}{V_{in}(S)} = \frac{2}{\left(\frac{z_s}{z_0}+1\right)\left(\frac{z_0}{z_L}+1\right)e^{\gamma l} + \left(\frac{z_s}{z_0}-1\right)\left(\frac{z_0}{z_L}-1\right)e^{-\gamma l}}, \qquad (1)$$

where γ is the propagation constant and z_0 is the characteristic impedance which are given by

$$z_0 = \sqrt{\frac{L_t}{C_t}}\sqrt{1+\frac{R_t}{SL_t}}, \quad \text{and} \quad \gamma l = S\sqrt{L_t C_t}\sqrt{1+\frac{R_t}{SL_t}}. \qquad (2)$$

For a CMOS gate driving another CMOS gate at the end of the line, $z_s = R_{tr}$ and $z_L = 1/SC_L$. A time scaling is applied by substituting t' / ω_n for each t where

$$\omega_n = \frac{1}{\sqrt{L_t(C_t + C_L)}}. \qquad (3)$$

From the characteristics of the Laplace transform, the complex frequency S is substituted by $\omega_n S'$. With this time scaling, the variables γ, z_0, and z_L are transformed to γ', z'_0, and z'_L, respectively, which can be evaluated by substituting $\omega_n S'$ for each S. If the exponential functions in the transfer function in (2) are replaced by a series expansion, the transfer function becomes

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$$\frac{V_{out}(S')}{V_{in}(S')} = \frac{1}{\left(1+\frac{z_s}{z'_L}\right)\left(1+\frac{(\gamma' l)^2}{2!}+.....\right)+\left(\frac{z_s}{z'_0}+\frac{z'_0}{z'_L}\right)\left((\gamma' l)+\frac{(\gamma' l)^3}{3!}+.....\right)}. \quad (4)$$

Substituting for $\gamma' l$, z'_0, and z'_L, the transfer function $V_{out}(S')/V_{in}(S')$ is a function of only three variables: ζ, R_T, and C_T which are

$$R_T = \frac{R_{tr}}{R_t}, \qquad C_T = \frac{C_L}{C_t}, \qquad \text{and} \quad (5)$$

$$\zeta = \frac{R_t}{2}\sqrt{\frac{C_t}{L_t}}\cdot\frac{R_T + C_T + R_T C_T + 0.5}{\sqrt{(1+C_T)}}. \quad (6)$$

The first few terms of the series expansion in S' are

$$\frac{V_{out}(S')}{V_{in}(S')} = \frac{1}{1+2\zeta S'+\left(\frac{0.5+C_T}{1+C_T}+16\zeta^2\left(1-\frac{R_T^2+C_T^2+(R_T C_T)^2}{(R_T+C_T+R_T C_T+0.5)^2}\right)\right)S'^2+\cdots}. \quad (7)$$

Thus, for a unit step input function, the output voltage waveform $V_{out}(t') = \mathcal{L}^{-1}\{(1/S)* V_{out}(S')/V_{in}(S')\}$ is also a function of the three variables ζ, R_T, and C_T. The scaled 50% propagation delay t'_{pd} can be calculated by solving $V_{out}(t'_{pd},\zeta,R_T,C_T) = 0.5$ which means that t'_{pd} is only a function of ζ, R_T, and C_T. Thus, the propagation delay of an *RLC* line with a source resistance R_{tr} and a load capacitance C_L has the form,

$$t_{pd} = \frac{t'_{pd}(\zeta, R_T, C_T)}{\omega_n}. \quad (8)$$

Note that this solution is characteristic of an *RLC* line and that no approximations have been made in deriving the result.

The scaled propagation delay t'_{pd} is dimensionless since ω_n has the units of 1/time. t'_{pd} is a function of only three variables which is the canonical number of variables to describe t'_{pd}. There are several ways to select these three variables. The three variables chosen here are R_T, C_T, and ζ since these variables are physically intuitive. The variables R_T and C_T characterize the relative significance of the gate parasitic impedances with respect to the interconnect parasitic impedances. Increasing R_T and C_T demonstrates that the gate parasitic impedances further affect the propagation delay. The third variable ζ is the coefficient of S^1 in the denominator of the transfer function. ζ is chosen as the third variable since the 50% delay is primarily dependent upon the coefficients of S^1 in the denominator and the numerator [13]. This characteristic is used to reduce the number of variables that affect the propagation delay from three to one (ζ). Note that the three variables R_T, C_T, and ζ are not independent since ζ is a function of R_T and C_T.

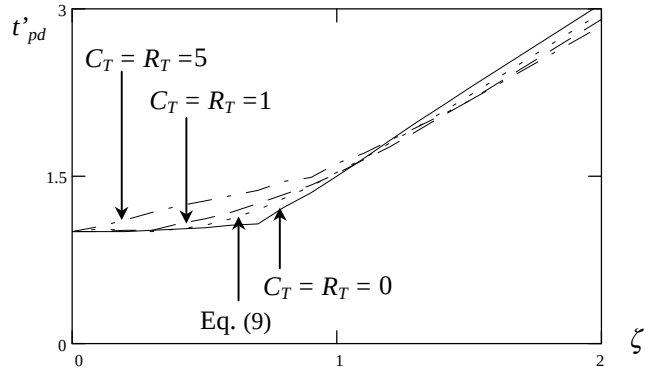

Fig. 2. Comparison of the accuracy of (9) to AS/X [14] simulations of the time scaled 50% propagation delay t'_{pd} of an *RLC* transmission line with a source resistance R_{tr} and a load capacitance C_L. The propagation delay is plotted versus ζ for different values of R_T and C_T.

AS/X [14] simulations of the time scaled 50% propagation delay of a gate driving an *RLC* transmission line t'_{pd} as a function of ζ, R_T, and C_T are shown in Fig. 2. Note in Fig. 2 that the propagation delay is primarily a function of ζ. The dependence on R_T and C_T is fairly weak. This characteristic does not imply that the transistor driving the interconnect and the load capacitance has a minor effect on the propagation delay since ζ includes the effects of R_T and C_T. Note also that this effect is particularly weak in the range where R_T and C_T are between zero and one. This range is most important for global interconnect and long wires in current deep submicrometer technologies. Thus, the propagation delay is primarily a function of ζ, which collects the five impedances that affect the propagation delay, R_t, L_t, C_t, R_{tr}, and C_L, into a single parameter. A curve fitting method is used to minimize the error when R_T and C_T are between zero and one, as illustrated in Fig. 2.

Using this approach, the propagation delay in the linear region can be modeled by the following function,

$$t_{pd} = (e^{-2.9\zeta^{1.35}} + 1.48\zeta)/\omega_n. \quad (9)$$

AS/X [14] simulations of the propagation delay of an *RLC* transmission line as compared to t_{pd} in (9) are shown in Table 1. Note that the solution exhibits high accuracy (the error is less than 5%) for a wide range of interconnect (R_t, L_t, and C_t) and gate impedances (R_{tr} and C_L). Note also that the simulation data listed in Table 1 include those cases where the response is underdamped and overshoots occur (high inductive effects), and those cases where the response is overdamped (low inductive effects). All of these operating modes are described by one continuous equation, (9).

Table 1. Comparison of t_{pd} in (9) to AS/X simulations characterizing the propagation delay of a CMOS gate driving an *RLC* transmission line. C_t = 1 pF and R_{tr} = 500 Ω.

R_T	L_t H	C_T = 0.1			C_T = 0.5			C_T = 1.0		
		(9)	ASX	Error	(9)	ASX	Error	(9)	ASX	Error
0.1	10^{-5}	3389	3287	3.3%	3893	3782	2.9%	4469	4344	2.8%
	10^{-6}	1062	1071	0.8%	1277	1328	3.8%	1553	1627	4.5%
	10^{-7}	532	552	3.6%	848	881	3.7%	1248	1269	1.6%
	10^{-8}	508	496	2.4%	850	883	3.7%	1239	1261	1.7%
0.5	10^{-5}	3397	3304	2.8%	4086	3940	3.8%	4504	4518	0.3%
	10^{-6}	1145	1108	3.3%	1489	1509	1.3%	1946	2030	4.1%
	10^{-7}	854	861	0.8%	1297	1300	0.2%	1812	1830	1.0%
	10^{-8}	841	850	1.0%	1277	1283	0.5%	1811	1825	0.8%
1.0	10^{-5}	3397	3291	3.0%	3897	3773	3.3%	4496	4383	2.6%
	10^{-6}	1070	1076	0.6%	1323	1345	1.6%	1712	1702	0.6%
	10^{-7}	634	609	4.1%	930	910	2.2%	1297	1281	1.2%
	10^{-8}	630	622	1.2%	936	913	2.5%	1294	1271	1.8%

An interesting special case is when the gate parasitic impedances (C_L and R_{tr}) are neglected. This case is particularly important since it describes the propagation delay characteristics of a distributed *RLC* line without the distortion of the gate impedances. For the limiting case where $L \rightarrow 0$, (9) reduces to $0.37RCl^2$. This expression is the same formula for the propagation delay of a distributed *RC* line as described in [3] and [11]. Also note the well known square dependence on the length of the wire. For the other limiting case where $R \rightarrow 0$, the propagation delay is given by $l\sqrt{LC}$. Note the linear dependence on the length of the line. Thus, the traditional quadratic dependence of the propagation delay on the length of an *RC* line approaches a linear dependence as inductance effects increase.

III. Repeater Insertion in *RLC* Interconnect

Traditionally, repeaters are inserted into *RC* lines to partition an interconnect line into shorter sections, *e.g.*, [9]-[11], thereby

reducing the total propagation delay. Applying the same idea to the general case of an *RLC* line, repeaters are used to divide the interconnect line into *k* sections as shown in Fig. 3. The buffers are each uniformly the same size and *h* times larger than a minimum size buffer. The buffer output impedance R_{tr} is R_0/h and the input capacitance of the buffer C_L is hC_0.

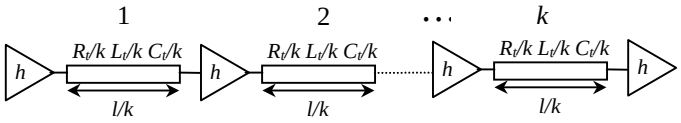

Fig. 3. Repeaters inserted in an *RLC* line to minimize the propagation delay.

The total propagation delay of a repeater system is the sum of the individual propagation delays of the *k* sections and is a function of *h* and *k* for a given interconnect line. The values of *h* and *k* at which the total delay $t_{pdtotal}$ is a minimum are determined by simultaneously solving the following two differential equations,

$$\frac{\partial t_{pdtotal}(h,k)}{\partial h}=0 \qquad \text{and} \qquad \frac{\partial t_{pdtotal}(h,k)}{\partial k}=0. \tag{10}$$

For the special case of an *RC* line ($L_t \rightarrow 0$), the solution for these equations is

$$h_{opt}(RC)=\sqrt{\frac{R_0C_t}{R_tC_0}} \qquad \text{and} \qquad k_{opt}(RC)=\sqrt{\frac{R_tC_t}{2R_0C_0}}. \tag{11}$$

These equations are the same as described by Bakoglu in [11].

Solving (10) for the general case of an *RLC* line is analytically intractable. However, as described in the appendix, h_{opt} and k_{opt} for an *RLC* line have the form,

$$h_{opt}=\sqrt{\frac{R_0C_t}{R_tC_0}}\bullet h'(T_{L/R}) \qquad \text{and} \qquad k_{opt}=\sqrt{\frac{R_tC_t}{2R_0C_0}}\bullet k'(T_{L/R}), \tag{12}$$

where $h'(T_{L/R})$ and $k'(T_{L/R})$ are error factors that account for the effect of the inductance and $T_{L/R}$ is

$$T_{L/R}=\sqrt{\frac{L_t/R_t}{R_0C_0}}. \tag{13}$$

The closed form solution for the propagation delay in (9) is used to characterize the delay of the repeater system shown in Fig. 3 as described in the appendix. The resulting expression is partially differentiated with respect to *h* and *k* and the two derivatives are equated to zero. The resulting two equations are solved numerically for the optimum values of *h* and *k*. Numerical solutions for h_{opt} and k_{opt} in (10) for different values of $T_{L/R}$ are plotted in Fig. 4.

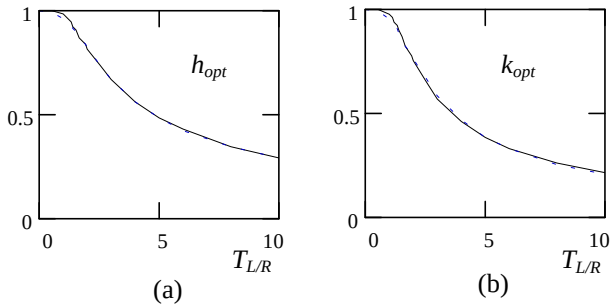

Fig. 4. Numerical solutions of (10) as compared to eqs. (14) and (15). a) h_{opt} as compared to (14). b) k_{opt} as compared to (15). Numerical solutions are shown by the solid line while (14) and (15) are shown by the dashed line.

Curve fitting is employed to determine a function that accurately characterizes h_{opt} and k_{opt}. These functions are

$$h_{opt}=\sqrt{\frac{R_0C_t}{R_tC_0}}\frac{1}{\left[1+0.16(T_{L/R})^3\right]^{0.24}}, \tag{14}$$

and

$$k_{opt}=\sqrt{\frac{R_tC_t}{2R_0C_0}}\frac{1}{\left[1+0.18(T_{L/R})^3\right]^{0.3}}. \tag{15}$$

These closed form expressions are highly accurate with an error of the total propagation delay of the repeater system of less than 0.05% as compared to numerical analysis. These formulae can therefore be considered exact for all practical purposes.

Upon examination of (14) and (15), h_{opt} and k_{opt} are equal to $h_{opt}(RC)$ and $k_{opt}(RC)$ in (11) for the special case of an *RC* impedance when $L_t \rightarrow 0$ (or $T_{L/R} \rightarrow 0$). Note that the error between the two cases increases as $T_{L/R}$ increases. This behavior is understandable since inductance effects are more significant as $T_{L/R}$ increases (which increases the error of neglecting L_t). Also note that as $T_{L/R}$ increases (or the inductance effects increase), the number of sections k_{opt} decreases. The improvement achieved by partitioning the line into shorter sections in the *RC* case is primarily due to the quadratic dependence of the propagation delay on interconnect length. In the other extreme case of an *LC* line, the propagation delay is linear with interconnect length and therefore no speed improvement is achieved by partitioning the line into shorter subsections. Actually, adding repeaters in this case would only increase the total propagation delay because of the additional gate delay of the repeaters. Thus, as inductance effects increase, the optimum number of repeaters to insert to minimize the total interconnect delay decreases.

The per cent increase in $t_{pdtotal}$ caused by neglecting inductance and treating an *RLC* line as an *RC* line as compared to including inductance based on (14) and (15) for h_{opt} and k_{opt}, respectively, is

$$\%\text{Increase}=\frac{100*\left|(t_{pdtotal})_{RC}-(t_{pdtotal})_{RLC}\right|}{(t_{pdtotal})_{RLC}}. \tag{16}$$

$(t_{pdtotal})_{RC}$ is calculated by substituting the solution for $h_{opt}(RC)$ and $k_{opt}(RC)$ in (11) into $t_{pdtotal}$. $(t_{pdtotal})_{RLC}$ is calculated by substituting the solution for h_{opt} and k_{opt} in (14) and (15), respectively, into $t_{pdtotal}$. The resulting solution is a function of $T_{L/R}$ only and can be accurately approximated by

$$\%\text{Increase}=\frac{30}{\sqrt{\left(1+\frac{0.5}{T_{L/R}}+23e^{-0.8T_{L/R}}+10^4e^{-4T_{L/R}}\right)}}. \tag{17}$$

Note that $(t_{pdtotal})_{RC}$ is larger than $(t_{pdtotal})_{RLC}$ as $T_{L/R}$ increases. For $T_{L/R}$ = 3, $t_{pdtotal}$ increases by 10%, for $T_{L/R}$ = 5, $t_{pdtotal}$ increases by 20%, and for $T_{L/R}$ = 10, $t_{pdtotal}$ increases by 30%.

The total area of the buffers in the repeater system is given by $A_{RLC}=h_{opt}*k_{opt}*A_{min}$ and $A_{RC}=h_{opt}(RC)*k_{opt}(RC)*A_{min}$ for the *RLC* and the *RC* case, respectively. A_{min} is the area of a minimum size buffer. The per cent area increase %*AI* is characterized by $100*(A_{RC}-A_{RLC})/A_{RLC}$ and is

$$\%AI=100\cdot\left\{\left[1+0.18(T_{L/R})^3\right]^{0.3}\cdot\left[1+0.16(T_{L/R})^3\right]^{0.24}-1\right\}. \tag{18}$$

The per cent area increase for $T_{L/R}$ = 3 is 154% and for $T_{L/R}$ = 5 is 435%. From the impedance values described in [7], it can be shown that $T_{L/R}$ = 5 is common for a current 0.25 μm technology. Thus, neglecting inductance not only increases the total delay of the repeater system but significantly increases the buffer area as well. This trend is expected since treating the interconnect as an *RC* line and neglecting inductance requires more repeaters. These additional repeaters add to the total delay and buffer area without reducing the line delay because significant inductance makes the dependence of the delay on the length of the interconnect become sub-quadratic. Note that $T_{L/R}$ increases as R_0C_0 decreases. This relation means that as the gate delay decreases, inductance becomes more important.

Thus, the effects of inductance in next generation design methodologies will become fundamentally important as technologies scale.

IV. Conclusions

Closed form solutions for the propagation delay of a CMOS gate driving a distributed *RLC* load are presented that are within 5% of AS/X simulations. It is shown that the traditional quadratic dependence of the propagation delay on the length of an *RC* line tends to a linear dependence as inductance effects increase. This behavior is expected to have a profound effect on future high speed CMOS technologies.

Closed form solutions are presented for inserting repeaters into *RLC* lines that are highly accurate with respect to numerical solutions. Inserting repeaters based on an *RC* model into *RLC* lines as compared to applying a distributed *RLC* impedance model of the interconnect increases the propagation delay by up to 30%, and the repeater area by up to 435% for common VLSI interconnect. The power consumption of the repeater system is also expected to be much less in the case of an *RLC* model as compared to an *RC* model due to the increased repeater area for the *RC* case. Thus, incorporating inductance into the interconnect impedance model is of crucial importance for accurately estimating the propagation delay of on-chip interconnect as well as for minimizing the propagation delay. This importance is expected to increase as the gate parasitic impedances decrease and as technologies increase in speed.

Appendix
Optimum Repeater Insertion in *RLC* Lines

As shown in section II, the propagation delay of a gate driving a single section of interconnect with an impedance of R_t, C_t, and L_t has the form given by (8). If repeaters are inserted to partition the line into k sections and each repeater is h times greater than a minimum size inverter, the total propagation delay of the system is the summation of the propagation delays of each of the individual sections. Since the sections are each equal, the total delay can be expressed as $t_{pdtotal} = kt_{pdsec}$, where t_{pdsec} is the propagation delay of a single section. Each section has an interconnect impedance equal to R_t / k, C_t / k, and L_t / k. Since each repeater is h times larger than a minimum size buffer, each repeater has an output resistance $R_{tr} = R_0 / h$ and a load capacitance of $C_L = C_0 h$. Thus, the total propagation delay of the repeater system is

$$t_{pdtotal} = k \cdot \frac{t_{pd}'(\zeta_{\sec}, R_{T\sec}, C_{T\sec})}{\omega_{n\sec}}, \tag{19}$$

where R_{Tsec} and C_{Tsec} are

$$R_{T\sec} = \frac{k}{h}\frac{R_0}{R_t} \quad \text{and} \quad C_{T\sec} = kh\frac{C_0}{C_t}. \tag{20}$$

ζ_{sec} and ω_{nsec} are

$$\zeta_{\sec} = \frac{R_t}{2k}\sqrt{\frac{C_t}{L_t}} \cdot \frac{R_{T\sec} + C_{T\sec} + R_{T\sec}C_{T\sec} + 0.5}{\sqrt{(1 + C_{T\sec})}}, \tag{21}$$

$$\omega_{n\sec} = \frac{k}{\sqrt{L_t C_t}\sqrt{1 + C_{T\sec}}}. \tag{22}$$

Guided by the solution of h and k for the special case of an *RC* line, the solution for an *RLC* line is in the form of

$$h = \sqrt{\frac{R_0 C_t}{R_t C_0}} \bullet h' \quad \text{and} \quad k = \sqrt{\frac{R_t C_t}{2R_0 C_0}} \bullet k', \tag{23}$$

where h' and k' are error factors that incorporate the existence of inductance and approach one as the inductance approaches zero. Substituting these values for h and k into (20), (21), and (22), the variables R_{Tsec}, C_{Tsec}, ζ_{sec}, and ω_{nsec} become

$$R_{T\sec} = \frac{k'}{h'\sqrt{2}}, \qquad C_{T\sec} = \frac{h'k'}{\sqrt{2}}, \tag{24}$$

$$\zeta_{\sec} = \frac{1}{\sqrt{2}k'T_{L/R}} \cdot \frac{R_{T\sec} + C_{T\sec} + R_{T\sec}C_{T\sec} + 0.5}{\sqrt{(1 + C_{T\sec})}}, \tag{25}$$

and

$$\omega_{n\sec} = \frac{k}{\sqrt{L_t C_t}\sqrt{(1 + C_{T\sec})}}, \tag{26}$$

where $T_{L/R}$ is given by

$$T_{L/R} = \sqrt{\frac{L_t / R_t}{R_0 C_0}}. \tag{27}$$

Thus, the total propagation delay has the form,

$$t_{pdtotal} = \sqrt{L_t C_t} \cdot f(h', k', T_{L/R}) \cdot \tag{28}$$

Determining the values of k' and h' that minimize the total propagation delay requires the simultaneous solution of the following two differential equations,

$$\frac{\partial f(h', k', T_{L/R})}{\partial h'} = 0 \quad \text{and} \quad \frac{\partial f(h', k', T_{L/R})}{\partial k'} = 0. \tag{29}$$

The solution of these equations demonstrates that h' and k' are only functions of $T_{L/R}$. Thus, the optimum number of sections k_{opt} and the optimum repeater size h_{opt} for an *RLC* interconnect is

$$h_{opt} = \sqrt{\frac{R_0 C_t}{R_t C_0}} \bullet h'(T_{L/R}) \quad \text{and} \quad k_{opt} = \sqrt{\frac{R_t C_t}{2R_0 C_0}} \bullet k'(T_{L/R}). \tag{30}$$

Note that this solution is characteristic of an *RLC* line and that no approximations have been made in deriving this result.

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