# Fast Algorithms for *IR* Voltage Drop Analysis Exploiting Locality *

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## ABSTRACT

Closed form expressions and related algorithms for fast power grid analysis are proposed in this paper. The *IR* voltage drop at an arbitrary point in a power distribution network is determined. Two algorithms are described for non-uniform voltage supplies and non-uniform current loads distributed throughout a power grid. The principle of spatial locality is exploited to accelerate the proposed power grid analysis method. Analysis of the non-uniform power grids utilizes the principle of spatial locality. Since no iterations are required for the proposed *IR* drop analysis, the proposed algorithms are over 70 times faster for smaller power grids composed of less than five million nodes and over 180 times faster for larger power grids composed of more than 25 million nodes as compared to existing methods. The proposed method exhibits less than 0.5% error.

## Categories & Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles;
B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

## General Terms

Algorithms, Design, Verification

## Keywords

Power grid analysis, Effective resistance, Voltage drop, Design verification

## 1. INTRODUCTION

With reduced power supply levels in modern microprocessors, *IR* drop analysis has become a crucial part of the circuit design process [1–4] since the performance of each individual circuit block depends upon the voltage within the power distribution network. Efficient analysis of the *IR* drops, however, is a difficult task due to the large physical dimensions of the power distribution network and the complex global interactions among the loads.

The *IR* drop analysis process can be formulated as a linear system with a conductance matrix modeling the power grid impedance. This matrix is solved by assigning a source vector for the voltage sources and another vector for the current loads. Although the formulation of the *IR* drop analysis process is straightforward, a solution of this linear system is infeasible for a typical power distribution network due to the large size. For example, if the power distribution system is composed of N rows and N columns, the total number of nodes is $N^2$, and the resulting conductance matrix to solve this power distribution network is $N^2 \times N^2$ [5]. The size of the conductance matrix thereof increases quadratically with increasing power network size. Due to the large size of power distribution networks in modern high complexity circuits, traditional linear solvers are incapable of solving this large linear system in reasonable time.

Several methods have been proposed for efficient power grid analysis; 1) reduce the size of the linear system, 2) iteratively solve the linear system, and 3) apply advanced linear algebraic techniques to exploit the sparse nature of the power grid. Conventional interconnect model order reduction techniques [6] are applicable for tree structured interconnects; however, these methods are inappropriate for mesh structured power distribution networks. The power grid can be reduced to a simpler structure where this coarse structure is later mapped into the original grid [1]. In [7], the power grid is partitioned into a number of smaller parts where each partition is analyzed separately. Random walk techniques are used to analyze a power grid in [8] to iteratively solve the *IR* drop problem without computing large matrix operations. Two efficient iterative algorithms are proposed in [5] to compute the *IR* drop within a power grid. Although these algorithms are faster than conventional linear solvers, significant computational time is required to iteratively apply these algorithms. An accurate closed form expression would effectively solve this problem.

Uniform current loads are generally assumed in power distribution networks to exploit symmetry in a linear system. In [9], an *IR* drop analysis is described for a power grid structure with semi-uniform current loads (*e.g.*, uniform load currents are assumed within each quadrant of the distribution network). Closed form expressions for the maximum *IR* drop are described in [10] assuming a uniform current distribution. To the authors' knowledge, no closed form expressions exist to describe the voltage drop at any point in a non-uniform power distribution network with non-uniform current loads and non-uniform voltage supplies.

In this paper, closed form expressions for the *IR* drop in a non-uniform power grid with non-uniform current loads and non-uniform voltage supplies are provided. The proposed method exploits the impedance characteristics of the power distribution network and the effective impedance between the active circuit blocks to provide these closed form expressions. Since no iteration is required to compute the *IR* drop at any particular node, the proposed algorithm outperforms previously proposed techniques. The principle of locality is also implemented in the proposed algorithm to accelerate the analysis process.

The rest of the paper is organized as follows. The power grid model used in the analysis is decribed and the *effective resistance* concept is explained in Section 2. In Section 3, the closed form expressions and related algorithms are reviewed. The principle of spatial locality is further explained and exploited to accelerate the proposed power grid analysis

*This research is supported in part by the National Science Foundation under Grant Nos. CCF-0811317 and CCF-0829915, grants from the New York State Office of Science, Technology and Academic Research to the Center for Advanced Technology in Electronic Imaging Systems, and by grants from Eastman Kodak Company, Intel Corporation, and Qualcomm Corporation.


*DAC '11, Jun 05-10 2011, San Diego, CA, USA*

**Table 1: Validity of the Effective Resistance Model in [12].**

| | $R_{1,0}$ | $R_{1,1}$ | $R_{3,4}$ | $R_{5,0}$ | $R_{10,10}$ |
|---|---|---|---|---|---|
| Exact solution (2) | 0.5 | 0.636 | 1.028 | 1.026 | 1.358 |
| Approximation (3) | 0.515 | 0.625 | 1.027 | 1.027 | 1.358 |
| Error (%) | 3 | 1.8 | 0.1 | 0.1 | 0 |

process in Section 4. Experimental results are provided in Section 5. The paper is concluded in Section 6.

## 2. BACKGROUND

The *IR* voltage drop at an arbitrary node depends upon the distance among the voltage sources, current loads, and analysis nodes. These distances are incorporated into the closed form expressions by the effective resistance concept since the effective resistance between any two nodes in a uniform grid structure depends upon the euclidean distance between these two nodes and the power grid resistance. The effective resistance supports the development of closed form expressions for use within the power grid analysis process.

Since this paper focuses on resistive voltage drop analysis, only a resistive network is considered. Two effective resistance models are considered in this paper. First, the effective resistance in a non-uniform power grid is considered [11] utilizing Green's function. The effective resistance between nodes $m$ and $n$ is

$$R_{m,n} = \sum_{i=2}^{N} \frac{1}{\lambda_i} |\psi_{im} - \psi_{in}|, \quad (1)$$

where $\lambda_i$ is the nonzero eigenvalues and $\boldsymbol{\psi}_i = (\psi_{i1}, \psi_{i2},...,\psi_{iN})$ are the orthonormal eigenvectors of the corresponding Kirchhoff matrix.

Venezian in [12] provides an exact solution for the effective resistance between any two points, $N_1(x_1, y_1)$ and $N_2(x_2, y_2)$, in an infinite grid as

$$R_{m,n} = \int_0^{\pi} \frac{(2 - e^{-|m|\alpha} cos(n\beta) - e^{-|n|\alpha} cos(m\beta))}{sinh(\alpha)} d\beta. \quad (2)$$

Venezian also provides a closed form approximation for (2) as

$$R_{m,n} = \frac{1}{2\pi} * ln(n^2 + m^2) + 0.51469, \quad (3)$$

where

$$m = |x_1 - x_2| \text{ and } n = |y_1 - y_2|. \quad (4)$$

$\alpha$ and $\beta$ are used to rewrite Kirchhoff's node equations as difference equations. The interested reader is urged to read [12] for a complete explanation.

While (1) provides an exact solution for the effective resistance in a non-uniform power grid, (3) provides a faster approximate solution for a uniform power grid. The error of the approximation in (3) is less than 3% as compared to the exact solution in (2). A few examples that demonstrate the validity of (3) are listed in Table 1 [12]. The error quickly approaches zero with increasing distance between two points. For instance, the average error when calculating all of the resistances in a 50×50 grid is less than 0.01%. Power grids in modern integrated circuits generally exhibit a locally uniform, globally non-uniform structure. (3) is used when the power grid has a uniform structure to reduce the runtime of the power grid analysis process. Alternatively, when the power grid exhibits a non-uniform structure, (1) is used to determine the effective resistance.

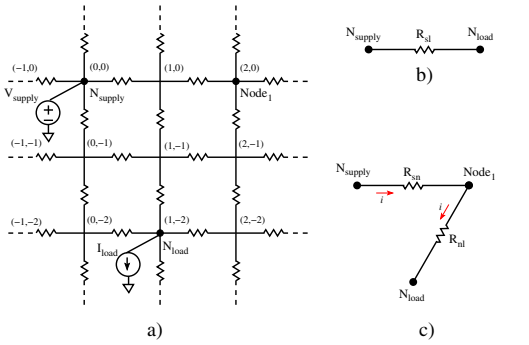


**Figure 1: Power distribution grid model a) one power supply connected at (0,0) and one current load connected at (1,-2), b) corresponding reduced effective resistance model between the power supply and the load, and c) the effective resistance model to determine the voltage at an arbitrary node Node$_1$ in the power grid.**

## 3. ANALYTIC VOLTAGE DROP ANALYSIS

Two algorithms are described in this section to determine the *IR* drop at an arbitrary node within a uniform power grid:

- Algorithm I: One power supply and one current load placed arbitrarily within the distribution network.
- Algorithm II: Multiple power supplies and multiple current loads placed arbitrarily within the distribution network.

Algorithm I is the basic algorithm and is used to explain Algorithm II. Algorithm II is the complete algorithm which can be used in the analysis of *IR* drop within practical power grids. The distance between two nodes does not affect the computational complexity of determining the effective impedance between these nodes. The computational complexity of the proposed algorithms therefore does not depend upon the size of the power grid.

### 3.1 One power supply and one current load

In this section, the *IR* voltage drop at an arbitrary node Node$_1$, shown in Fig. 1a, is determined when one power supply and one current load exist within the power grid [13]. The power grid model shown in Fig. 1a reduces to the effective resistance model to determine the voltage at the load and at an arbitrary node, as illustrated, respectively, in Figs. 1b and 1c. The effective resistance between N$_{supply}$ and Node$_1$, Node$_1$ and N$_{load}$, and N$_{supply}$ and N$_{load}$ is denoted, respectively, as $R_{sn}$, $R_{nl}$, and $R_{sl}$. The voltage at N$_{load}$ is

$$V_{load} = V_{supply} - I_{load} * R_{sl}. \quad (5)$$

After determining the voltage at N$_{load}$ (see Fig. 1b), the voltage at Node$_1$ can be found as follows. Assume that all of the load current $I_{load}$ flows from N$_{supply}$ to N$_{load}$ along the path $R_{sn}$ - Node$_1$ - $R_{nl}$. Since the voltage at N$_{supply}$ and N$_{load}$ is known *a priori*, the voltage at Node$_1$, $V_{Node_1}$, can be found with respect to either N$_{supply}$ or N$_{load}$. $V_{Node_1}$ is

$$V_{Node_1} = V_{supply} - I_{load} * R_{sn} \quad (6)$$

with respect to N$_{supply}$ and

$$V_{Node_1} = V_{load} + I_{load} * R_{nl} \quad (7)$$

*IR* Drop: One Power Supply and One Current Load
1. Given: Supply voltage ($V_{supply}$), load current ($I_{load}$)
   Locations of voltage supply ($N_{supply}$),
   current load ($N_{load}$), and $Node_1$.
2. Calculate the effective resistances between
   a) $N_{supply}$ and $Node_1$, $R_{sn}$
   b) $Node_1$ and $N_{load}$, $R_{nl}$
   c) $N_{supply}$ and $N_{load}$, $R_{sl}$.
3. Calculate the voltage at $N_{load}$, (5).
4. Calculate the voltage at $Node_1$ $V_{Node_1}$, (8).
5. Calculate the *IR* drop at $Node_1$, (10).

**Figure 2: Algorithm I. *IR* voltage drop at an arbitrary node within a power grid with one power supply and one current load.**

with respect to $N_{load}$. The voltage at $Node_1$ is the arithmetic mean of the voltages found using (6) and (7) [13]. The voltage at $Node_1$ is therefore

$$V_{Node_1} = [V_{supply} + V_{load} + I_{load} * (R_{nl} - R_{sn})]/2. \quad (8)$$

Substituting (5) into (8), the voltage at $Node_1$ can be written as

$$V_{Node_1} = [2 * V_{supply} + I_{load} * (R_{nl} - R_{sn} - R_{sl})]/2. \quad (9)$$

The *IR* voltage drop at $Node_1$ is equal to $V_{supply}$ - $V_{Node_1}$,

$$IR_{Node_1} = I_{load} * (R_{sn} + R_{sl} - R_{nl})/2. \quad (10)$$

Pseudo-code of Algorithm I is summarized in Fig. 2.

## 3.2 Multiple power supplies and current loads

In this section, the *IR* voltage drop at an arbitrary node within a power distribution network is determined when multiple voltage supplies and multiple current loads exist, as shown in Fig. 3a. To determine the *IR* voltage drop for this system, superposition is applied in two steps. First, the current that each individual voltage supply contributes to each individual current load is determined by removing all but one of the current loads [14]. After determining the individual current contributions, the equivalent current source of a voltage supply is

$$I_{source}(i) = \sum_{j=1}^{m} I_{source(i,j)}, \quad (11)$$

where $I_{source(i)}$ is the equivalent current source of the $i^{th}$ voltage supply, $I_{source(i,j)}$ is the current contribution of the $i^{th}$ voltage supply to the $j^{th}$ current load, and $m$ is the number of current loads. Since the total current sourced by the voltage supplies is equal to the total current sunk by the current sources, the following expression is satisfied,

$$\sum_{i=1}^{n} I_{source}(i) = \sum_{j=1}^{m} I_{load(j)}. \quad (12)$$

All but one of the voltage supplies are replaced with an equivalent current source, as illustrated in Fig. 3b. The *IR* voltage drop at an arbitrary node within a power distribution network can be found as

$$IR_{Node_1} = \frac{1}{2}\sum_{i=1}^{m}[I_{load(i)} * (R_{sn(1)} + R_{sl(1)} - R_{nl})] - \frac{1}{2}\sum_{i=2}^{n}[I_{supply(i)} * (R_{sn(1)} + R_{sl(i)} - R_{nl(i)})], \quad (13)$$

*IR* Drop: Multiple Power Supplies and Multiple Current Loads
1. Given: Supply voltage ($V_{supply}$), load currents ($I_{load(j)}$)
   Locations of voltage supplies ($N_{supply(i)}$),
   current loads ($N_{load(j)}$), and $Node_1$.
2. **for** each voltage supply, $V_{supply(i)}$, **do**
3. **for** each current load, $I_{load(j)}$, **do**
4. Calculate the effective resistances between
   $N_{supply(i)}$ and $I_{load(j)}$, $R_{(i,j)}$.
5. **for** each voltage supply, $V_{supply(i)}$, where i≠1, **do**
6. **for** each current load, $I_{load(j)}$, **do**
7. Find the corresponding current, $I_{supply(i,j)}$.
8. Sum up $I_{supply(i,j)}$ for all $j$ to calculate $I_{supply(i)}$, (11).
9. Replace $V_{supply(i)}$ with $I_{supply(i)}$.
10. **for** each current load, $I_{load(j)}$, **do**
11. Remove all current supplies, $I_{supply(i)}$.
12. Calculate the effective resistances between
   a) $N_{supply(1)}$ and $Node_1$, $R_{sn}$
   b) $Node_1$ and $N_{load(j)}$, $R_{nl(j)}$
   c) $N_{supply(1)}$ and $N_{load(j)}$, $R_{sl(1,j)}$.
13. Calculate the *IR* drop at $Node_1$ due to all $I_{load(j)}$, (10).
14. **for** each current supply, $I_{supply(i)}$, **do**
15. Remove all other current supplies, $I_{supply(k)}$, where k≠1.
16. Remove all current loads, $I_{load(j)}$.
17. Calculate the effective resistances between
   a) $N_{supply(1)}$ and $Node_1$, $R_{sn}$
   b) $Node_1$ and $N_{supply(i)}$, $R_{nl(i)}$
   c) $N_{supply(1)}$ and $N_{supply(i)}$, $R_{sl(i)}$.
18. Calculate the voltage difference at $Node_1$ due to $I_{supply(i)}$, (10).
19. Calculate the total *IR* drop at $Node_1$ by subtracting
   the result of step 18 from the result of step 13, (13).
20. Calculate the voltage at $Node_1$, $V_{node_1}$, (14).

**Figure 4: Algorithm II. *IR* voltage drop at an arbitrary node $Node_1$ within a power grid with multiple power supplies and current loads, as shown in Fig 3a.**

and the corresponding voltage at $Node_1$ is

$$V_{Node_1} = V_{supply(1)} - \frac{1}{2}\sum_{i=1}^{m}[I_{load(i)} * (R_{sn(1)} + R_{sl(1)} - R_{nl})] + \frac{1}{2}\sum_{i=2}^{n}[I_{supply(i)} * (R_{sn(1)} + R_{sl(i)} - R_{nl(i)})], \quad (14)$$

where $m$ is the number of current loads and $n$ is the number of voltage supplies. Pseudo-code of Algorithm II is provided in Fig. 4.

# 4. LOCALITY IN POWER GRID ANALYSIS

Practical power grids in high performance integrated circuits can be treated as a locally uniform, globally non-uniform grid. To apply the proposed algorithms to the analysis of realistic power grids, the principle of spatial locality [2,15,16] is applied. This principle for a resistive power grid is described in Section 4.1. The effect of utilizing spatial locality on the power grid analysis process is explained in Section 4.2. In Section 4.3, the principle of spatial locality is exploited and integrated into the proposed power grid analysis method.

## 4.1 Principle of spatial locality in a power grid

Flip-chip packages are widely used in high performance integrated circuits, increasing the number of voltage supply connections to the integrated circuit. C4 (controlled collapse chip connect) bumps connect the integrated circuit to external circuitry from the top side of the wafer using solder bumps. A large number of power supply connections is provided to the power grid via these C4 bumps. Most of the current to the load devices is provided from those power supply connections in close proximity due to the smaller effective impedance. This phenomenon can be explained using the principle of spatial locality in a power grid [2, 15, 16].

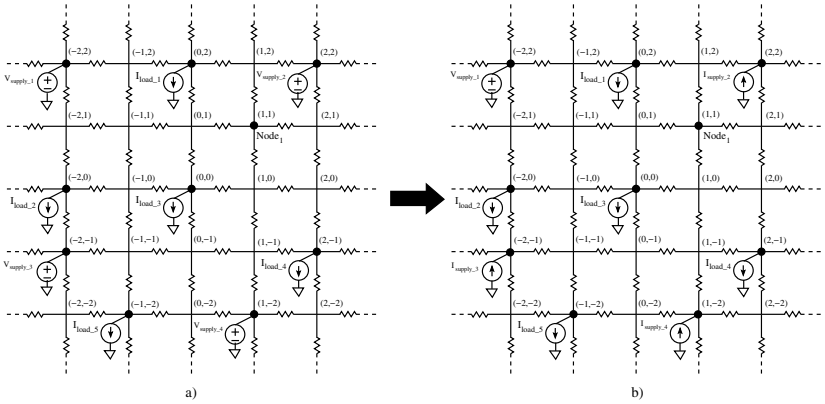


**Figure 3: Power distribution grid model a) multiple power supplies and current loads are connected to several nodes and b) all but one of the voltage sources are replaced with an equivalent current source.**

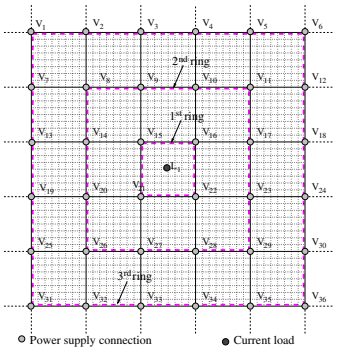


**Figure 5: A portion of a typical power grid with C4 bumps illustrated with light dots and the load device, $L_1$, with a dark dot. Most of the load current is supplied by the supply connections forming the first ring. Power supply connections within the third ring contribute less than 1% of the total current.**

A power grid for a flip-chip package with C4 connections is illustrated in Fig. 5. To exemplify the principle of spatial locality in a power grid, a current load is connected to the power grid as depicted in Fig. 5 to analyze the current contributions from each supply connection. The current contributed from each of the C4 connections to $L_1$ is as illustrated in Fig. 6. Most of the current is provided by the close power supplies. The current contribution of a supply connection decreases significantly with distance. The current contribution from most of the supply connections within the third ring is less than 1% of the total load current. The principle of locality is therefore applicable to power grids with multi-power supply connections such as flip-chip packages. Locality can also be applied to power distribution networks with tens of on-chip voltage regulators [17]. In this case, most of the current is supplied by the closest on-chip power supplies rather than the closest C4 connections.

## 4.2 Effect of spatial locality on computational complexity

The computational complexity of the power grid analysis process can be significantly reduced by introducing spatial locality since the voltage fluctuations at a specific node are primarily determined by the power grid impedance and

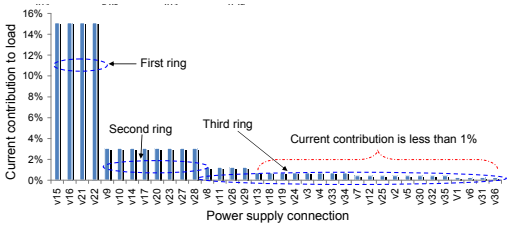


**Figure 6: Per cent current provided to $L_1$ placed in the middle of a uniform power grid from the power supplies. Note that most of the current is provided by the power supplies within the closest two rings.**

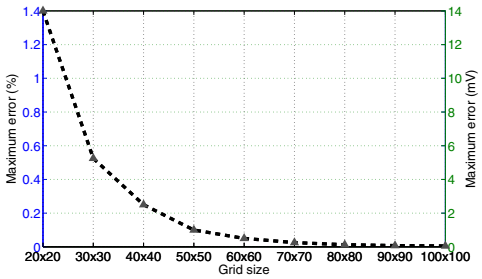


**Figure 7: Maximum error for different grid size. The per cent error in terms of the supply voltage and the absolute error are shown, respectively, in the left and right axes. Note that the error decreases significantly with increasing grid size.**

placement of those supply connections in close proximity [15]. The complex global interactions among distant circuit components, which typically have a negligible effect on the *IR* drop, is not considered with spatial locality.

## 4.3 Exploiting spatial locality in the proposed method

A power grid is divided into smaller partitions [15, 16] to exploit the principle of spatial locality. Each partition is analyzed individually and a complete solution is obtained by combining the results of each partition. For each partition, the error is smallest in the middle of the partition and increases towards the boundaries. A partitioning approach divides the power grid into several overlapping win-

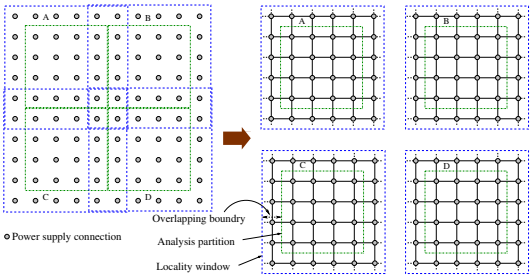


**Figure 8: Power grid divided into smaller partitions. Each partition consists of an analysis partition and overlapping boundary.**

dows where only the middle of each window is analyzed. The boundaries of each partition overlap with the adjacent partitions. This method of overlapping windows has been shown to be effective in industrial power grids to accelerate the power grid analysis process [15]. This partitioning approach is illustrated in Fig. 8 where a flip-chip power grid with several C4 connections is partitioned into four overlapping windows. When the size of the overlapping boundary is sufficiently large, the effect of the adjacent power grid partition is minimized. In this paper, the size of each partition and the overlapping boundary are maintained larger than 100×100 and 20, respectively, making the approximation error less than 0.1%. The partitioning approach also considers the locally uniform, globally non-uniform nature of the power grid. When the power grid in the partition exhibits a highly uniform structure, (3) is used to speed up the analysis, otherwise (1) is used for non-uniform power grid partitions.

## 5. EXPERIMENTAL RESULTS

The validity of the proposed algorithms to efficiently analyze a power grid for several scenarios is presented in this section. The algorithms are implemented using MATLAB and the computations are performed on a Unix workstation with a 3 GHz CPU and 10 GB of RAM. The accuracy of Algorithms I, II, and III is compared with SPICE simulations. For simplicity, the resistance between two adjacent nodes in the power grid is assumed to be 1 Ω and the voltage sources are assumed to be 1 volt. The current loads are between 1 mA and 100 mA.

The validity of the proposed closed form expression for one voltage supply and one current load is analyzed with a 1 volt supply connected at $N_{3,3}$ and the load sinking 100 mA at $N_{5,4}$. The maximum error is 1.44 mV, less than 0.2% of the supply voltage. The error of the corresponding node voltages as compared to SPICE is listed in Table 2. The light-grey box is the supply node and the dark-grey box is the node where the current load is connected.

Algorithm II is validated for a larger power grid with multiple voltage supplies and multiple current loads arbitrarily placed within a 17 x 17 power grid. The results of Algorithm II are compared with SPICE and the error is tabulated in Table 3. The current loads sink between 1 mA to 100 mA from the grid and the voltage supplies are 1 volt. The maximum error is 4.03 mV which is less than 0.5% of the supply voltage.

The computational complexity of the random walk method is *O(LMN)* [18] where $N$ is the number of nodes without

**Table 2: Error of Algorithm I as compared to SPICE. The voltage supply is connected at $N_{3,3}$ (light gray) and the load device is connected at $N_{5,4}$ (dark gray). The maximum error is less than 0.2% of the supply voltage.**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| 1 | -0.12 | -0.05 | 0.46 | -0.27 | -0.49 | -0.26 | -0.125 | -0.15 |
| 2 | -0.09 | -0.55 | 0.79 | 0.152 | -0.68 | -0.37 | -0.554 | -0.14 |
| 3 | 0.33 | 0.62 | 0 | 1.13 | -0.52 | 0.52 | 0 | -0.26 |
| 4 | -0.31 | -0.83 | 0.21 | -1.44 | -0.31 | -0.93 | -0.64 | -0.41 |
| 5 | -0.25 | -0.27 | 0.37 | 0.24 | -1.10 | 0.24 | -0.22 | -0.38 |
| 6 | -0.18 | -0.04 | 0.18 | -0.04 | -0.77 | -0.25 | -0.18 | -0.30 |
| 7 | -0.13 | -0.01 | 0 | -0.23 | -0.50 | -0.36 | -0.28 | -0.30 |
| 8 | -0.14 | -0.04 | -0.08 | -0.27 | -0.32 | -0.34 | -0.34 | -0.34 |

power supply connections, $L$ is the number of steps in a single walk, and $M$ is the number of walks to determine the voltage at a node. The random walk method is faster for flip chip power grids as compared to wire-bond power grids or power grids with a limited number of on-chip power supplies since $M$ is significantly larger. The computational complexity of the random walk method can however be decreased with hierarchical methods [18, 19], although the property of locality is sacrificed.

Alternatively, the computational complexity of the proposed method is linear with the size of the power grid. Since no iterations are required (*i.e.*, $L = 1$) and the voltage is determined with closed form expressions (*i.e.,* $M = 1$), the computational complexity is *O(N)*. The computational complexity does not depend on the type of power grid (*e.g.*, the same computational complexity for flip chip, wire-bond power grids, and power grids with on-chip power supplies).

To compare the computational runtime of the proposed method with previously proposed techniques, five differently sized circuits with evenly distributed C4 bumps 25 nodes away from each other are considered. The partition size for all of the circuits when utilizing locality is larger than 100×100 to maintain the approximation error less than 0.1%. The runtime of the proposed algorithm is compared with the random walk method in [8], as shown in Table 4. The random walk method is run for 20,000 iterations on each circuit to accurately determine the node voltages. The number of iterations of the random walk method is chosen to maintain a maximum error of less than 10 mV as compared to the results with 20,000 iterations. The error of the proposed method is also less than 10 mV for each circuit. The proposed method without utilizing locality is over 26 times faster than the random walk method for circuits smaller than five million nodes. The proposed method with locality is over 70 times faster for power grids smaller than five million nodes. For circuit sizes greater than 25 million nodes (*e.g.*, Circuits IV and V in Table 4), the proposed algorithm with locality is over 180 times faster than the random walk method.

## 6. CONCLUSIONS

Closed form expressions for fast *IR* voltage drop analysis of large power grids with non-uniform current loads and voltage supplies are proposed in this paper. Since the proposed algorithms utilize closed form expressions, the runtime is significantly lower than previously proposed power grid analysis methods while exhibiting reasonable error (*i.e.*, 4.03 mV for Algorithm II, an error of less than 0.5% of the supply voltage). Previously proposed *IR* drop analysis methods iteratively solve the power grid to determine the node volt-

**Table 3: Error of Algorithm II as compared to SPICE. Power supplies are connected at the corners (light gray) and current loads are connected at different nodes (dark gray). The maximum error is 4.03 mV (less than 0.5% of the power supply voltage).**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0.36 | 0.10 | -0.25 | -0.32 | -0.43 | -0.57 | -0.53 | -0.28 | 0.07 | 0.39 | 0.87 | 1.1 | 1.71 | 2.26 | 3.06 | 4.03 |
| 2 | 0.4 | -0.52 | -0.4 | -0.29 | -0.45 | -0.67 | -0.93 | -1.15 | -0.68 | -0.18 | 0.22 | 0.65 | 1.08 | 1.43 | 1.76 | 1.87 | 3.3 |
| 3 | 0.18 | -0.27 | -0.39 | -0.45 | -0.58 | -0.85 | -1.31 | -2.35 | -1 | -0.32 | 0.19 | 0.62 | 0.91 | 1.28 | 1.56 | 1.94 | 2.5 |
| 4 | -0.12 | -0.24 | -0.36 | -0.44 | -0.49 | -0.73 | -1.09 | -1.17 | -0.64 | -0.2 | 0.24 | 0.56 | 0.84 | 1.22 | 1.55 | 1.75 | 2.1 |
| 5 | -0.2 | -0.26 | -0.31 | -0.36 | -0.42 | -0.46 | -0.93 | -0.56 | -0.25 | 0.01 | 0.28 | 0.55 | 0.89 | 1.19 | 1.42 | 1.65 | 1.83 |
| 6 | -0.28 | -0.3 | -0.38 | -0.38 | -0.31 | -0.07 | -0.9 | -0.01 | -0.07 | 0.09 | 0.23 | 0.58 | 0.89 | 1.12 | 1.37 | 1.48 | 1.66 |
| 7 | -0.33 | -0.29 | -0.31 | -0.44 | -0.56 | -0.83 | -0.27 | -0.54 | -0.17 | 0.14 | 0.2 | 0.69 | 0.93 | 1.12 | 1.25 | 1.44 | 1.61 |
| 8 | -0.34 | -0.3 | -0.34 | -0.22 | -0.15 | -0.11 | -0.28 | 0.43 | 0.2 | 0.57 | 0.18 | 0.96 | 0.91 | 1.06 | 1.25 | 1.43 | 1.48 |
| 9 | -0.36 | -0.33 | -0.35 | -0.23 | 0.18 | -0.4 | 0.03 | 0.11 | -0.16 | 0.12 | 0.59 | 0.39 | 0.67 | 0.99 | 1.18 | 1.35 | 1.52 |
| 10 | -0.46 | -0.47 | -0.4 | -0.48 | -0.54 | -0.2 | -0.46 | 0.15 | -0.06 | 0.99 | 0.3 | 1.05 | 1 | 1.15 | 1.19 | 1.38 | 1.51 |
| 11 | -0.44 | -0.48 | -0.36 | -0.24 | 0.07 | -0.62 | 0.05 | -0.11 | 0.37 | 0.16 | 0.21 | 0.75 | 1.02 | 1.25 | 1.28 | 1.55 | 1.56 |
| 12 | -0.48 | -0.5 | -0.35 | -0.3 | -0.14 | -0.36 | 0.17 | 0.6 | 0.13 | 0.81 | 0.58 | 0.84 | 1.05 | 1.18 | 1.37 | 1.44 | 1.67 |
| 13 | -0.55 | -0.48 | -0.48 | -0.37 | -0.27 | -0.18 | 0.1 | 0.3 | 0.26 | 0.7 | 0.68 | 1.02 | 1.14 | 1.38 | 1.39 | 1.74 | 1.84 |
| 14 | -0.6 | -0.65 | -0.64 | -0.53 | -0.24 | -0.12 | 0.12 | 0.2 | 0.28 | 0.51 | 0.87 | 0.97 | 1.15 | 1.37 | 1.55 | 1.8 | 2.06 |
| 15 | -0.7 | -0.93 | -0.77 | -0.55 | -0.25 | -0.09 | 0.09 | 0.24 | 0.44 | 0.68 | 0.82 | 1.09 | 1.29 | 1.44 | 1.66 | 1.91 | 2.39 |
| 16 | -0.95 | -1.58 | -0.94 | -0.56 | -0.32 | -0.11 | 0.03 | 0.25 | 0.46 | 0.72 | 0.88 | 1.12 | 1.35 | 1.57 | 1.83 | 1.89 | 3.04 |
| 17 | -2.49 | -0.84 | -0.46 | -0.51 | -0.16 | -0.03 | 0.16 | 0.3 | 0.52 | 0.65 | 0.84 | 1.14 | 1.37 | 1.73 | 2.21 | 2.92 | 3.47 |

**Table 4: Runtime comparison**

| | #nodes | Random walk [8] (min:sec) | Proposed algorithm | | | |
|---|---|---|---|---|---|---|
| | | | No partitioning (min:sec) | Speed enhancement | Utilizing locality (min:sec) | Speed enhancement |
| Circuit I | 250K | 4:22 | 0:10 | 26x | 0:03 | 87x |
| Circuit II | 1M | 15:08 | 0:32 | 28x | 0:12 | 76x |
| Circuit III | 4M | 59:46 | 2:19 | 26x | 0:51 | 70x |
| Circuit IV | 25M | 1,156:14 | 17:13 | 67x | 6:22 | 181x |
| Circuit V | 49M | 3,418:05 | 38:55 | 88x | 12:47 | 267x |

ages. These methods require the voltages at all of the nodes adjacent to the analysis node to be determined. Evaluating the voltage at a particular node therefore requires the computation of the voltages at nearby nodes which may not be of interest. Alternatively, the proposed algorithms presented in this paper can compute the voltage at any particular node in a non-uniform power grid without determining the voltage at the adjacent nodes. The proposed algorithm can therefore be applied to localized power grid analysis.

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