Thermal Coupling in TSV-Based 3-D Integrated Circuits

Ioannis Savidis[1] and Eby G. Friedman[2]

[1]Department of Electrical and Computer Engineering, Drexel University , Philadelphia, Pennsylvania 19104 , isavidis@coe.drexel.edu

[2]Department of Electrical and Computer Engineering, University of Rochester , Rochester, New York 14627 , friedman@ece.rochester.edu

***Abstract*— A three-dimensional (3-D) test circuit examining thermal propagation within a 3-D integrated stack has been designed, fabricated, and tested. Design insight into thermal coupling in 3-D ICs through experimental means is provided, and suggestions to mitigate thermal effects in 3-D ICs are offered. Intra- and inter-plane thermal coupling is investigated through single point heat generation using resistive thermal heaters and temperature monitoring through four-point resistive measurements. The peak steady state temperature due to die location within a 3-D stack is described.**

***Index Terms*— 3-D IC, thermal propagation, 3-D IC heat transfer, 3-D thermal effects.**

I. Introduction

Although extensive theoretical work [1] has provided an understanding of heat flow in 3-D ICs, there has been limited experimental results quantifying the flow of heat between device planes. Meindl *et al.* experimentally characterized the impact of microfluidic cooling techniques on both 2-D and 3-D circuits [2]. Numerical and experimental characterization of thermal hot spots of a packaged DRAM on logic 3-D IC has also been described [3]. Similar to this work, inter-plane thermal propagation has been investigated. The primary purpose of the results described in this paper however is to characterize intra- and inter-plane thermal coupling to improve design methodologies and techniques for stacked ICs. The experimental results discussed herein provide insight into the effects of the location of the heat source and active cooling on heat flow within 3-D ICs.

The test circuit has been fabricated by Tezzaron Semiconductor in a 130 nm CMOS technology with 1.2 μm diameter TSVs. A face-to-face bonding technique to vertically stack the two logic device planes is used. This test circuit is designed to also evaluate the effects of inter- and intra-plane thermal resistance on hot spot formation. A schematic depiction of a two die stack with a hot spot on one die affecting the second die is shown in Fig. 1.

The 3-D test circuit is described in the following section. Experimental characterization of thermal coupling and a discussion of experimental results for a set of test configurations are presented in Section III. Some conclusions are offered in Section IV.

II. Thermal Propagation Test Circuit

A microphotograph of the 5 mm by 5 mm 3-D test circuit depicts two locations from which thermal data are collected. The center-to-center distance between the back metal sensors is 1.1 mm, while the on-chip sensors are 1.3 mm apart. Each device plane includes a thermal sensor on metal 3 and a resistive heater on metal 2. The backside metal heaters and sensors are at the top of the stack.

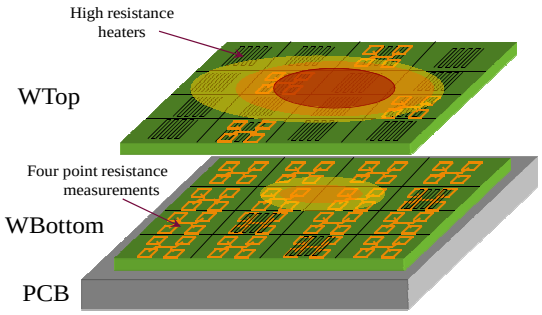


Fig. 1: Heat propagation from one device plane spreading into a second stacked device plane.

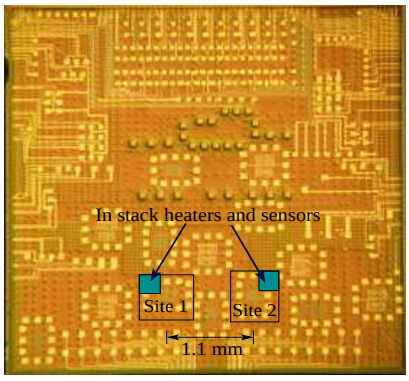
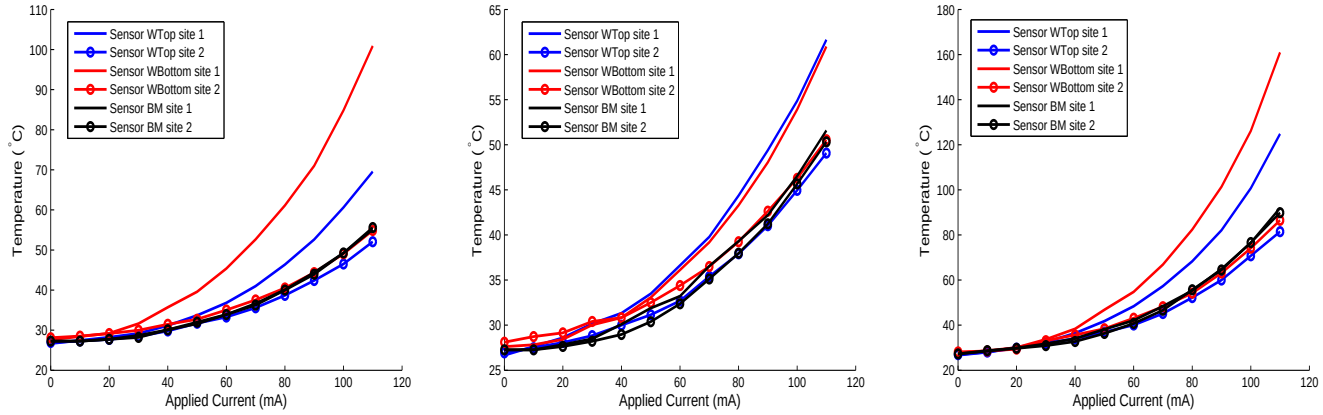


Fig. 2: Microphotograph of the test circuit depicting the back metal pattern with an overlay indicating the location of the on-chip thermal test sites.

The test structures are used to investigate thermal coupling between adjacent planes and include both resistive thermal sources and thermal sensors. The thermal sensors use four-point voltage measurements. Each thermal source is paired with a resistive thermal sensor on an adjacent metal level. The heaters are 200 μm by 210 μm and are in metal 2. Within this area, the total length of the heater is 2,120 μm. The resistance of the heaters is therefore 18.7 Ω. Joule heating through the resistive heater is adjusted by controlling the current flow, and therefore the I^2R power consumed within the 200 by 210 μm^2 area. The thermal sensors, with dimensions of 200 μm by 86 μm, are placed directly above the heaters in metal 3. The total length of the sensors is 4,442 μm. The resistance of the sensors is 117.7 Ω based on a width of 2 μm, a metal 3 thickness of 0.42 μm, and a nominal sheet resistance of 0.053 Ω/□. The temperature sensor provides a calibrated four point measurement tested at a low current to avoid joule heating.



(a) WBottom site 1; no fan (b) WTop site 1; no fan (c) WBottom site 1, WTop site 1; no fan

Fig. 3: Experimental results for the different test conditions. Each label describes the device plane, site location of the heater, and whether active cooling is applied.

III. Experimental Results and Design Considerations

The resistive heaters are controlled to provide different test conditions to investigate thermal propagation within the 3-D stack. A current is individually supplied to the heaters on WBottom and WTop. These results are shown in Figs. 3(a) and 3(b). A second experiment examines the effects of placing two highly active device blocks directly above each other, as described by comparing Figs. 3(a) and (b) to Fig. 3(c).

The experimental test conditions described in Section III provide insight into thermal propagation and hot spot formation in 3-D ICs. Design considerations to minimize hot spot formations are discussed below.

A. Effects and mitigation of placement on hot spot formation

The effects of stacking two dies on the temperature profile of a 3-D IC are significant, as shown in Figs. 3(a) and 3(b). The maximum observed temperature on WBottom site 1 increases by 65.7% when the resistive heater is active on WBottom as compared to an active heater on WTop (from 60.9° C to 100.9° C). The maximum observed temperatures occur for an applied current of 110 mA. For heater currents less than 110 mA, the per cent increase in temperature for WBottom as compared to WTop decreases due to the exponential drop in temperature as the current is reduced. Data from the remaining five thermal sensors reveal a temperature increase of 6.1% to 13.0%, with the 13.0% increase occurring on the sensor located directly above the active heater on WTop. Placing a highly active device block in WBottom requires special consideration as the thermal resistance along the path to the top of the 3-D stack is higher than to a block placed in WTop.

B. Multiple aligned active blocks

The placement of two highly active circuit blocks aligned directly above one another has a significant effect on the thermal profile of an entire 3-D IC. Placing an active block on WBottom produces a higher thermal resistive path than a block placed on WTop. An analysis of two vertically aligned active circuit blocks has been performed by comparing the temperature for a single heater placed on WBottom with the increase in temperature caused by placing two active heaters located at WTop and WBottom site 1. The largest temperature increase occurs at WTop site 1, where a 79.4% increase in temperature is observed (from 69.6° C to 124.8° C) for an applied current of 110 mA. The maximum on-chip temperature occurs on WBottom site 1, where the maximum temperature increases from 100.9° C to 161.0° C when a current of 110 mA flows through one active heater and two active heaters, producing a 59.6% increase in temperature. The magnitude of the current has a significant effect on the thermal profile within a 3-D IC.

IV. Conclusions

The performance and reliability of a 3-D integrated circuit is greatly affected by large heat gradients. Thermal effects can potentially alter the performance of the clock and power networks due to hot spots. Proper block placement and active and passive heat removal techniques are critical to ensure a 3-D IC operates within the specified thermal design power envelope.

A three-dimensional test circuit examining thermal propagation within a 3-D stack has been designed, fabricated, and tested. Two test conditions, the location and the relative vertical alignment of the two active circuits, are examined to characterize thermal propagation in 3-D integrated circuits. Design suggestions are provided to better manage hot spot formation while reducing the effects on neighboring circuit blocks. The position of a block relative to a heat sink significantly affects the thermal resistance and therefore the flow of heat from the hot spots. This test circuit provides enhanced understanding of thermal hot spot formation and propagation within 3-D integrated circuits.

References

[1] A. Jain, R. E. Jones, R. Chatterjee, and S. Pozder, "Analytical and Numerical Modeling of the Thermal Performance of Three-Dimensional Integrated Circuits," *IEEE Transactions on Components and Packaging Technologies*, Vol. 33, No. 1, pp. 56–63, March 2010.

[2] B. Dang, M. S. Bakir, D. C. Sekar, C. R. King Jr., and J. D. Meindl, "Integrated Microfluidic Cooling and Interconnects for 2D and 3D Chips," *IEEE Transactions on Advanced Packaging*, Vol. 33, No. 1, pp. 79–87, February 2010.

[3] H. Oprins, V. O. Cherman, B. Vandevelde, G. Van der Plas, P. Marchal, and E. Beyne, "Numerical and Experimental Characterization of the Thermal Behavior of a Packaged DRAM-on-Logic Stack," *Proceedings of the IEEE Electronic Components and Technology Conference*, pp. 1081–1088, June 2012.