Physical Design Issues and Technology Trends in Networks-on-Chips

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Abstract

This presentation focuses on the physical level of the NoC design process. At this level, the global interconnects and routers are critical to NoC communication. Synchronization, clock distribution, and power delivery in complex on-chip systems are also primary areas that must be addressed in NoC-based systems. Possible trends in NoC development include merging 3-D integration and optical interconnect with NoC architectures.