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Low Power CMOS Bi-Directional Voltage Converter

Volkan Kursun, Radu M. Secareanu, and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627-0231

Abstract - A bi-directional CMOS voltage interface circuit is proposed for applications that require an interface between two circuits operating at different voltage levels. The circuit can also be used as a level converter at the driver and receiver ends of long interconnect lines for low swing applications. The proposed interface circuit operates at high speed while consuming very little power. Operation of the interface circuit is verified by both simulation and experimental test circuits.

I. INTRODUCTION

The dominant component of power consumption in CMOS circuits is dynamic power [1]. The most effective way of reducing dynamic power consumption is to reduce the supply voltage. Since lowering the supply voltage also degrades the speed of a circuit [1], it is advantageous for different regions to operate at different voltages in high complexity integrated circuits [2], [3], [4], [7]. Blocks that require high throughput operate at a higher voltage while those blocks for which speed is less critical operate at a lower voltage. In order to transfer signals among these regions operating at different voltage levels, specialized voltage interface circuits are required [2], [7].

Another issue in modern integrated systems is the significant amount of on-chip interconnect capacitance. In many recent systems, charging and discharging the interconnect lines can require more than 50% of the total power consumption [5], [6]. In certain programmable devices, more than 90% of the total power consumption is due to the interconnect wires [5].

As shown in [1], [4], [5], and [6], decreasing the voltage swing can significantly decrease the power consumed when driving long interconnect lines. The circuit architecture proposed in [6] for interconnect voltage swing reduction is shown in Figure 1. In this scheme, the circuit blocks operate at a high voltage for high throughput, while a low voltage swing signal is transmitted along the interconnect to decrease the power consumption. Voltage interface circuits are therefore required at the driver and receiver ends of this low swing interconnect architecture to convert the voltage levels.

A simple interface circuit composed of two cascaded CMOS inverters is a standard circuit approach for converting voltage levels. This circuit suffers from static power consumption and a non-full rail output voltage swing when converting a low voltage swing input to a high voltage swing output (the receiver end shown in Figure 1) [2], [3], [6], [7]. More efficient circuit structures are therefore needed to accomplish this voltage level conversion.

A bi-directional CMOS voltage interface circuit that drives high capacitive loads to full swing at high speed while consuming no static power is presented in this paper. Operation of the circuit is described in Section 2, simulation results are presented in Section 3, and results from experimental test circuits are presented in Section 4. Finally, some conclusions are provided in Section 5.

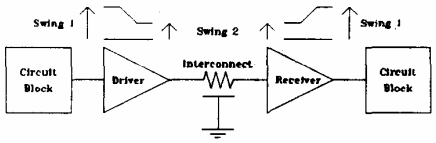

Figure 1. Circuit architecture for interconnect voltage swing reduction

II. CIRCUIT OPERATION

The interface circuit proposed here is shown in Figure 2. The voltage interface circuit provides bi-directional voltage level conversion. Therefore, without any change in circuit configuration, the interface circuit can be used at both the driver and receiver ends of a low voltage swing circuit architecture (such as shown in Figure 1) to convert voltage levels from high to low and low to high.

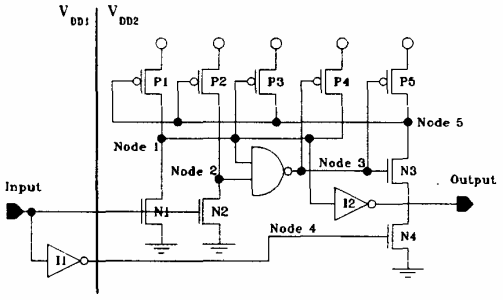

Figure 2. The proposed voltage interface circuit.

In the proposed interface circuit, P1 is isolated from the input to minimize both the static power consumption and the propagation delay. As the pull-up and pull-down networks are never on simultaneously, the circuit dissipates no static power while driving high capacitive loads to full swing at high speed.

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In this circuit, only I1 is supplied by V_{DD1}. The rest of the circuit (to the right of the demarcation line) is supplied by V_{DD2}. The circuit operates in the following manner. With a 0 → 1 transition at the input, nodes 1 and 2 are discharged through N1 and N2, respectively. When node 1 becomes sufficiently low, the output transitions high. The positive feedback path from node 1, node 3, and across the P4 transistor increases the rate of discharge at node 1, minimizing the short-circuit power consumption and output transition time. With a 1 → 0 transition at the input, node 4 goes high, turning on N4. Node 5 is pulled down to ground through N3 and N4, turning on P1 and P2 (N3 is on before the input changes). Nodes 1 and 2 are charged through P1 and P2, respectively. When node 1 becomes sufficiently high, the output transitions low. P2 is sized smaller than P1 such that node 1 is charged much faster than node 2. This sizing ensures that the NAND gate does not switch before I2 switches. After the NAND gate switches, P1 is cut-off, and P4 is turned on, preserving the state of node 1.

III. SIMULATION RESULTS

The circuit has been simulated for a 0.18 μm CMOS technology. A capacitive load of 20 pF is assumed. The input signal applied to the interface circuit is a 1 MHz square wave signal with a 50% duty cycle. The input to output delay is calculated from the 50% of the input swing to the 50% of the output swing. The average power consumption is calculated for a full cycle of the input waveform. The two power supply levels are 3.3 volts and 1.8 volts. Simulation results characterizing the circuit are listed in Table 1.

Table 1. Propagation delay and average power consumption of the voltage interface circuit for both the 3.3 V → 1.8 V and 1.8 V → 3.3 V interfaces.

Voltage Levels	Output 1 → 0 (ns)	Output 0 → 1 (ns)	Pavg (μW)
3.3 V → 1.8 V	7	6	66.9
1.8 V → 3.3 V	5	3	228.6

IV. EXPERIMENTAL RESULTS

The interface circuit has been fabricated in a 3 μm CMOS technology. A microphotograph of the circuit is shown in Figure 3.

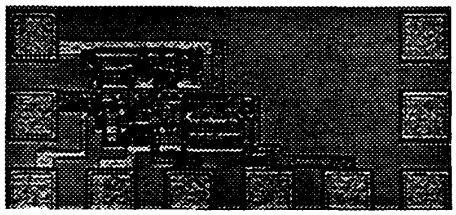

Figure 3. Microphotograph of the interface circuit.

The circuit has been experimentally evaluated with 5 volt and 10 volt power supplies. The experimental results are listed in Table 2. The waveforms obtained from the circuit tests are shown in Figure 4 (the time axis is 500 ns/division, and the voltage axis is 5 volts/division).

Table 2. Experimentally measured test results.

Voltage Levels	Output 1 → 0 (ns)	Output 0 → 1 (ns)
10 V → 5 V	200	70
5 V → 10 V	120	90

The functional operation of the proposed interface circuit has also been experimentally verified. As listed in Table 2, the propagation delays from the input to the output are greater than the simulation results (see Table 1) due to the different voltage levels and feature sizes (3 μm vs. 0.18 μm).

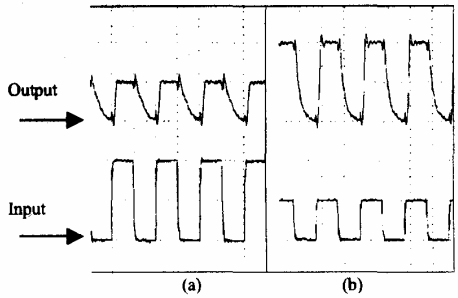

Figure 4. Experimentally derived input and output voltage waveforms of the voltage interface circuit. (a) 10 V → 5 V interface. (b) 5 V → 10 V interface.

V. CONCLUSIONS

A bi-directional CMOS voltage interface circuit for signal transfer between circuits operating at different voltage levels is presented in this paper. The circuit can also be used at the driving and receiving ends of long interconnect lines so as to dissipate lower power by propagating a smaller voltage swing signal along the line. The circuit operates at high speed while consuming no static power.

VI. REFERENCES

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