Optimum Wire Sizing and Repeater Insertion in Distributed *RLC* Interconnect

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Abstract

Repeaters are often used to drive high impedance interconnects. These lines are becoming highly inductive which can affect signal behavior in long interconnects. The line inductance should, therefore, be considered in determining the optimum number and size of the repeaters driving a line. A tradeoff exists, however, between the transient power dissipation and the propagation delay in sizing long interconnects driven by a repeater system as shown in Fig. 1.

A repeater system, as shown in Fig. 2, is an efficient technique to drive long interconnects [1]. For different line lengths l, the optimum number of repeaters $k_{opt-RLC}$ decreases with the line width. Unlike $k_{opt-RLC}$, the optimum repeater size $h_{opt-RLC}$ is an increasing function of line width as the line capacitance C_{int} also increases with line width.

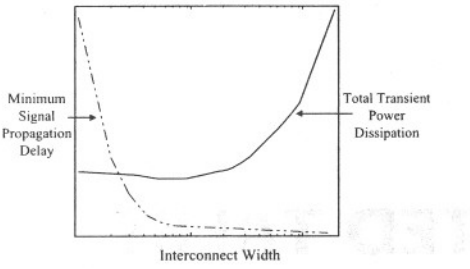

Figure 1: Minimum signal propagation delay and transient power dissipation as a function of line width for a repeater system

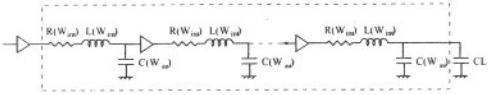

Figure 2: Uniform repeater system driving distributed *RLC* interconnect

For a distributed *RC* line, repeater insertion has been shown to outperform wire sizing [2]. For an *RLC* model, however, wider wires with no repeaters achieves a smaller signal propagation delay. In a repeater system, increasing the line width decreases the minimum propagation delay and the optimal number of repeaters. The minimum delay decreases with increasing line width since the total gate delay decreases. For an inductive interconnect line, the total signal propagation delay is $t_{pd-total} = k_{opt-RLC}\, t_{pd-section}$ where $t_{pd-section}$ is the signal delay of each *RLC* section [3].

Increasing the width of a distributed *RLC* interconnect line reduces the total transient power dissipation. The reduction in both short-circuit and dynamic power of the inserted repeaters overcomes the increase in dynamic power dissipation of the line until the line capacitance dominates the overall line impedance [4].

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A single expression for the power-delay product as a function of the interconnect width is

$$PDP(W_{int}) = P_{total}(W_{int})^{w_p}\, t_{pd-total}(W_{int})^{w_d}, \qquad (1)$$

where w_p and w_d are the weights of the cost functions. A local minimum for the power delay product exists for each line length. The minimum power delay product is obtained by numerically solving the nonlinear equation, $\frac{\partial PDP}{\partial W_{int}} = 0$.

Three criteria can be used to size the interconnect. The first criterion is for minimum power while sacrificing performance. The second criterion is for minimum delay. This criterion is achieved with the maximum repeater size available for the technology (or no repeaters). The optimum line width and number of repeaters are determined from [3] based on the maximum driver size. Otherwise, no repeaters are used and the design problem reduces to choosing the width of a single section of interconnect. The third criterion satisfies both power dissipation and performance. The weights w_p and w_d determine which design objective is more highly valued.

The three criteria are compared for an example circuit assuming a 0.24 μm CMOS technology. For a repeater system with the following characteristics, $C_0 = 1$ fF and $w_p = w_d = 1$, the optimum solution obtained by applying each criterion is listed in Table 1.

Table 1: Uniform repeater system for different optimization criteria

l = 15 mm		Min. Power	No Repeaters	Min. PDP
W_{int} (μm)		0.8	20	3.9
# of Repeaters		5	0	1
Repeater Size (μm)		43.2	225.6	80.7
Min. Delay	Total	3.87	0.19	0.43
(nsec)	Increase	1936 %	0 %	126.3 %
Power	Total	5.20	21.31	7.58
(mW)	Increase	0 %	310 %	45.7 %

For l = 15 mm, the optimum solution for minimum power delay product increases the delay by 126% as compared to 1936% for the solution for minimum power. The power increases by 45% as compared to 310% for the no repeater solution. Optimizing the interconnect to produce a minimum power delay product produces a much smaller increase in both the power and delay as compared to separately optimizing either the power or delay. The choice of PDP as a design criterion can satisfy current high performance, low power design objectives.

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