Power Efficiency of 14 nm MCML Near Threshold Circuits

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***Abstract*—Near threshold circuits (NTC) are an attractive and promising technology that provides significant power savings with some delay penalty. The feasibility of NTC technology with MOS Current Mode Logic (MCML) based on a 14 nm FinFET process is examined in this work. A 32 bit Kogge Stone adder is chosen as a demonstration vehicle for simulation and feasibility analysis. MCML is shown to yield enhanced power efficiency when operated with a 100% activity factor above 1 GHz as compared to CMOS. Standard CMOS does not achieve frequencies above 9 GHz without a dramatic increase in power consumption. MCML is most efficient beyond 9 GHz over a wide range of activity factors. MCML also exhibits significantly lower noise levels as compared to standard CMOS. The results of the analysis demonstrate that pairing NTC and MCML is efficient when operating at high frequencies and activity factors.**

I. Introduction

Near threshold circuits (NTC) consume an order of magnitude less power than circuits operating under nominal voltages while not suffering from the significant delay penalty found in subthreshold circuits. NTC has therefore become an attractive methodology for sub-30 nm CMOS circuits [1]. In this work, NTC [2] is paired with MOS Current Mode Logic (MCML) to compensate for the vulnerable aspects of each technology.

MCML is a differential circuit topology driven by a constant tail current. The lack of switching transients contributes to a low noise environment as compared to standard CMOS. The low noise environment is particularly beneficial for NTC due to the low voltage operation.

II. Simulation Results

The simulations are based on 14 nm low power FinFET predictive technology models [3]. A standard threshold voltage of $V_{th} = 350$ mV is assumed. The supply voltage is set to 400 mV to operate near the threshold voltage with an MCML input/output voltage swing of 100 mV. A 32 bit Kogge Stone adder is evaluated in both standard CMOS and MCML.

III. Conclusions

The combination of NTC and MCML exploits the advantages of each technology [4]. Unlike standard CMOS, MCML circuits operating near the threshold voltage perform better at higher frequencies and higher activity factors. Unlike standard CMOS, 14 nm MCML circuits operating near the threshold voltage can achieve high operating frequencies and power efficiencies at frequencies above 9 GHz.

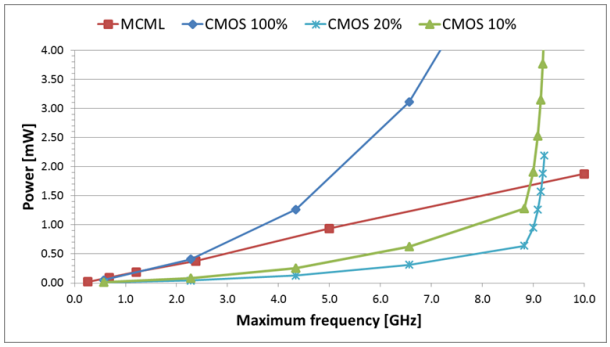

Fig. 1. Power vs maximum frequency of MCML and standard CMOS for activity factors of 100%, 20%, and 10%

TABLE I
Comparison of Noise in CMOS and MCML Circuits

Power network parasitic impedances			Noise induced on power network [mV]		
			MCML	CMOS	
PN Res [ohm]	PN Cap [fF]	PN Ind [nH]	Absolute value	Absolute value	Ratio
2	50	1	0.56	6.27	11
2	50	2	0.94	9.92	11
2	50	4	0.70	14.64	21
2	100	1	1.28	6.19	5
2	100	2	0.95	9.14	10
2	100	4	1.81	13.51	7
2	200	1	0.55	6.21	11
2	200	2	0.93	9.96	11
2	200	4	0.66	12.56	19
5	50	1	1.32	6.50	5
5	50	2	0.84	9.75	12
5	50	4	1.71	14.63	9
5	100	1	0.51	6.52	13
5	100	2	0.93	9.29	10
5	100	4	0.72	13.24	18
5	200	1	1.25	6.60	5
5	200	2	0.83	10.02	12
5	200	4	1.61	12.16	8

References

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[4] A. Shapiro and E. G. Friedman, "Performance Characteristics of 14 nm Near Threshold MCML Circuits," *Proceedings of the IEEE S3S Conference*, pp. 79–80, October 2013.