# Field-Enhanced STT-MRAM Switching for Reduced Write Latency and Energy


Ravi Patel, Engin Ipek, and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester



Spin torque transfer magnetoresistive RAM (STT-MRAM) is a modern CMOS compatible memory technology with the promise of becoming the mainstream on-chip memory. Key features of STT-MRAM are non-volatility, no static power consumption, and unlimited write endurance. A key issue constraining the use of STT-MRAM, however, is the switching latency of the magnetic tunnel junction (MTJ) within each memory cell. The long latency causes the switching energy of an MTJ to be much greater than traditional CMOS SRAM.

To address these issues, the classic first generation MRAM cell topology is utilized with an STT-MTJ where an additional field current destabilizes the MTJ prior to switching, thereby reducing the switching latency. As illustrated in Fig. 1a, classical MRAM cells utilize two large orthogonal currents to generate magnetic fields within the MTJ located at the intersection of the metal lines. These fields are sufficiently strong to induce a torque on the magnetization, which induces a reversal in the device state. In modern spin torque transfer MTJs, the internal ferromagnetic layers generate a torque on the magnetization by passing a current through the device. STT-MTJs can be switched using a smaller current applied directly to each cell, allowing many MTJs to be written in parallel, as shown in Fig 1b. By leveraging both the STT effect and a current induced magnetic field, in the manner shown in Fig 1c, the write latency for a single MTJ can be reduced. Moreover, the additional field current is amortized over many cells within a row, leading to a significant reduction in energy per bit.

An MRAM array model is presented to determine the switching energy and maximum achievable reduction in energy using the field driven approach and constraints on the memory system size. MTJ switching is evaluated via the Landau–Lifshitz–Gilbert (LLG) expression in conjunction with a macrospin approximated free layer to determine the effect of the applied field on the write latency. The switching latency per bit is reduced by more than a factor of ten. The resultant switching energy per bit is reduced by 82% as compared to standard STT-MRAM.


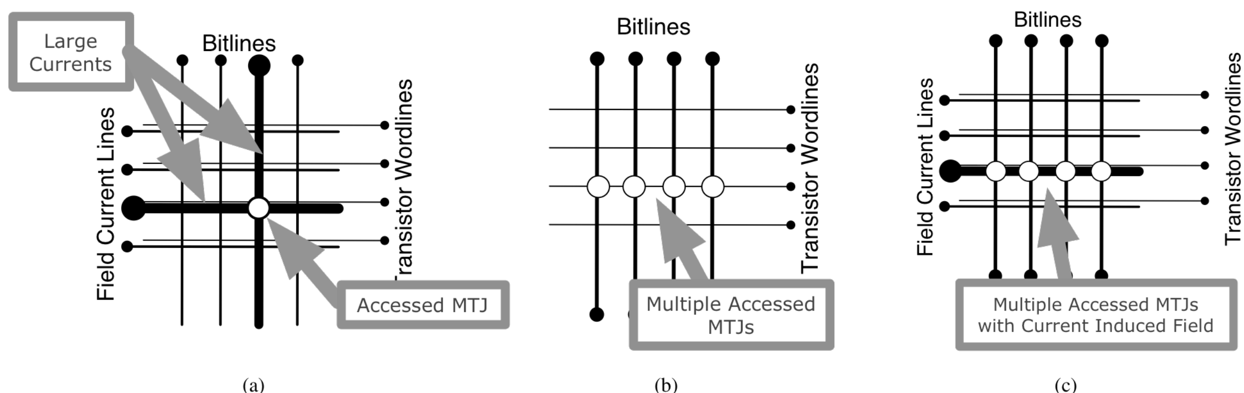


Fig. 1 Current biasing scheme for a) classical MRAM, b) standard STT-MRAM, and c) the proposed STT-MRAM