A Design Environment for Single Flux Quantum Circuits*

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Introduction

Two important figures of merit that describe a circuit technology are speed and power. With a junction switching speed on the order of picoseconds and power consumption of approximately one microwatt per junction, superconductive Single Flux Quantum (SFQ) circuits have superior performance characteristics as compared with most other technologies [1]. However, due to the immaturity of this technology, not only does the process complexity impede the development of large scale circuits, but the lack of a design infrastructure slows progress as well.

An efficient design environment for superconductive technology is currently under development at the University of Rochester. A minimum capability for efficiently designing SFQ circuits includes layout, simulation, and verification. We are currently extending this capability to automatically manage many of the more difficult and time consuming elements of the SFQ design flow.

At present, a significant turn around time exists from circuit concept to physical layout in the development of SFQ circuits. By improving the existing design methodology, composed of the Magic layout system coupled with the SPICE circuit simulator JSIM, the turn around time and circuit accuracy will be greatly improved. Our primary objective is to develop a top-down design methodology in which an SFQ circuit is developed from schematic description down to physical layout. Highlights of this methodology include circuit simulation, design verification, and physical synthesis.

SFQ Design Methodology

In order to realize the goal of improved design efficiency, a more powerful and flexible integrated design environment is required. An industry standard IC CAD tool, Cadence, has been acquired for the development of this new design capability. These Cadence tools support physical layout, circuit extraction, circuit verification, and schematic entry. The flow of the calibration effort is shown in Figure 1 and described below.

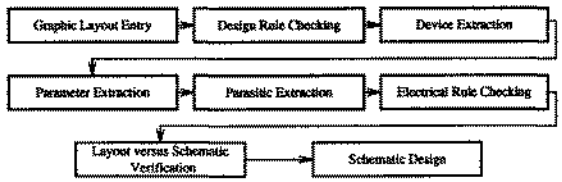

Figure 1: Flow graph for Cadence-based design environment

Graphic layout is the lowest level used to describe a circuit. At this level, the circuit is described in terms of geometric data used in producing masks. Our superconducting technology is foundried at HYPRES Inc., and is composed of a niobium/aluminum oxide/niobium tri-layer requiring ten mask layers. Therefore, the graphic layout environment supported by Cadence Diva has been calibrated for this superconductive technology using ten layers. A sample layout is displayed in Figure 2 [2].

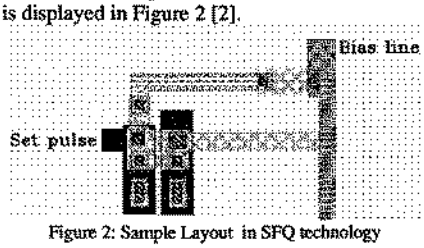

Figure 2: Sample Layout in SFQ technology

The next level of the design methodology is design rule checking (DRC). DRC is used to evaluate the graphic layout data for any physical design rule violations. In an interactive process, any errors are flagged during physical layout, permitting the violations to be immediately corrected. The design rules are calibrated for same-layer spacing, different-layer spacing, minimum width, and layer enclosure.

Special design rules have been developed for a sloped via structure. With a sloped via, the physical path for the carriers to travel from the shunt resistor to the metal 1 level and back to the ground plane is substantially shortened. This reduces the total inductance of the path, thereby improving the performance characteristics of the junction.

Once the circuit has been physically laid out and checked for physical design errors, certain characteristics can be extracted from the graphical data. The device extraction process recognizes a specific junction by a combination of mask layers. The location of each specified device is noted. After a device is extracted, its physical parameters are attached to its instance through parameter extraction. Examples of parameters are the junction area (of a Josephson Junction device), the ohms per square of a resistor, and the ohms per square bend of a resistor.

One of the more important steps in developing a CAD-based design infrastructure for SFQ circuits is parasitic device extraction. Parasitic impedances are always present in integrated circuits, whether superconductive or semiconductor, and cannot be neglected. These impedances are a function of geometric and material properties. In the case of SFQ technology, the parasitic inductance of the metal layers is of primary concern. A look-up table approach is being utilized in which an inductance value for a variety of different geometries is predetermined given the length and width of a metal line. Curve fitting of these inductance values has been computed for several ranges of metal widths [3]. This look-up table has been integrated into Cadence, permitting the extraction of the line inductance for a variety of widths. The curve fit function for the inductance of metal 1 over metal 0 is shown in Figure 3. These inductance values are quite close to those derived from FastHenry [4], a three dimensional finite analysis tool used for determining the inductance in specific circuit structures.

Inductance (pH) = A(w)*length-B(w)
For Metal 1 over Metal 0 (w = width of line)

w=2	A=0.148	B=0.035	w=4	A=0.081	B=0.024
w=6	A=0.057	B=0.019	w=8	A=0.043	B=0.014
w=10	A=0.036	B=0.012	w=12	A=0.031	B=0.010
w=14	A=0.027	B=0.009	w=16	A=0.024	B=0.008

valid for lengths from 2 to 40 μm

Figure 3: Curve fit function for inductance

Electrical rule checking (ERC) is performed to assure that the circuit does not contain electrical errors (e.g., power/ground overlaps and unconnected floating nets). ERC is a precursor to layout versus schematic (LVS) verification. With LVS, the physical layout is compared directly against a schematic description generated from both the schematic and its corresponding layout. This permits a circuit at the schematic level to be compared with a custom physical layout to ensure that proper connectivity is maintained.

Conclusions

This paper briefly reviews recent advances in the development of a design methodology for SFQ circuits. Graphic layout entry, design rule checking, device extraction, parameter extraction, parasitic extraction, electrical rule checking, and layout-vs.-schematic verification have each been implemented in the Cadence-based CAD environment targeted specifically to an SFQ technology. Future plans for our SFQ design infrastructure include building a library of schematics with an associated physical layout for fast semi-custom design, timing analysis, and behavioral simulation.

References

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[3] Private communications, Dr. Boran Guan.

[4] M. Kamon, C. Smithhisler, and J. White, "FastHenry Users Guide", Research Laboratory of Electronics, Department of Electrical Engineering and Computer Science, MIT, January 1993.

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