A Delay Expression for a Short-Channel CMOS Inverter Driving a Resistive-Capacitive Load

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Abstract – A delay model of a CMOS inverter driving a resistive-capacitive load is presented. The model is derived from Sakurai's alpha power law and exhibits good accuracy over a wide range of RC loads. Expressions are provided for estimating the propagation delay and transition time for a CMOS inverter driving resistive-capacitive interconnect lines.

I. Introduction

As the size of CMOS integrated circuits increases, interconnections have become increasingly significant. With a linear increase in length, interconnect delay increases quadratically due to the linear increase in both interconnect resistance and capacitance [1].

An analytical expression is presented for the transient response of a CMOS inverter driving an RC load rather than a simple capacitive load. Sakurai's alpha power law [2] is used to describe the circuit operation of the CMOS transistors rather than the classical Shichman-Hodges model [3]. The alpha power law model considers short channel behavior, permitting increased accuracy and generality in the design expressions. These expressions are used to estimate the propagation delay and the rise and fall times (or transition times) of a CMOS inverter.

II. General Solution

When the input to a CMOS inverter (see Figure 1) is a unit step, V_{out} is initially large. The circuit operates in the linear region for a greater portion of the total transition time for a large RC load. If the input function increases more slowly, or the load impedance is small, the inverter operates in the saturation region for a longer time before switching into the linear region.

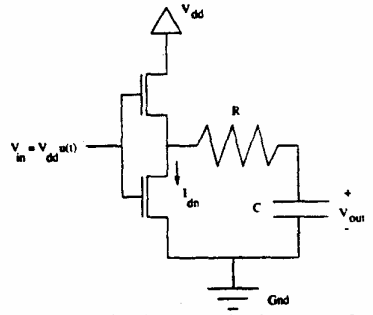

Figure 1. CMOS inverter driving an RC load

The following delay expressions are equally applicable to a rising output (falling input) waveform. The N-channel linear drain current is given by

$$-C\frac{dV_{out}}{dt} = i_d = \frac{I_{do}}{V_{do}}\left(\frac{V_{gs}-V_T}{V_{DD}-V_T}\right)^{\alpha} V_{ds}, \quad V_{gd} \geq V_T \qquad (1)$$

In the alpha power law model, I_{do} represents the drive current of the MOS device and is proportional to W/L, V_{do} represents the drain-to-source voltage at which velocity saturation occurs with $V_{GS} = V_{DD}$, and α models the process dependent degree to which the velocity saturation affects the drain-to-source current. V_{DD} is the supply voltage, and V_T is the MOS threshold voltage.

Assuming a unit step input is applied to the circuit shown in Figure 1, V_{out} is

$$V_{out}(t) = V_{out}(0)e^{\frac{-\mathfrak{U}_{do}}{\mathfrak{U}_{do}RC+\frac{C}{K}}t} \qquad (2)$$

where $\mathfrak{U}_{do} = \frac{I_{do}}{V_{do}}$ is the saturation conductance, and K is a technology dependent constant.

From (2), the propagation delay of a CMOS inverter calculated at the 50% point t_{PD} is

$$t_{PD} = .693\frac{\frac{C}{K}+\mathfrak{U}_{do}RC}{\mathfrak{U}_{do}} \qquad (3)$$

The transition time of a CMOS inverter driving a lumped RC load calculated at the 90% point t_t is

$$t_t = 2.3\frac{\frac{C}{K}+\mathfrak{U}_{do}RC}{\mathfrak{U}_{do}} \qquad (4)$$

The maximum error of the analytic model versus SPICE is listed in Table I. Note that both the 50% propagation delay and the 10% to 90% transition time are shown. The maximum error as compared with SPICE of the transition time is 8%, and of the propagation delay is 27%.

Table I. Propagation delay and rise time of CMOS inverter driving an RC load.

Load Resistance	Load Capacitance	t_t		t_{PD}		Error	
		Analytic	SPICE	Analytic	SPICE	t_t	t_{PD}
10 Ω	.001 pF	26 ps	25 ps	7.9 ps	9.7 ps	4%	20%
10 Ω	.01 pF	60 ps	60 ps	18 ps	25 ps	0%	27%
10 Ω	.1 pF	383 ps	365 ps	117 ps	147 ps	2%	20%
10 Ω	1 pF	3.4 ns	3.4 ns	1 ns	1.3 ns	0%	21%
100 Ω	.001 pF	27 ps	25 ps	8.2 ps	9.8 ps	8%	15%
100 Ω	.01 pF	58 ps	58 ps	17 ps	23 ps	0%	25%
100 Ω	.1 pF	370 ps	377 ps	112 ps	146 ps	2%	23%
100 Ω	1 pF	3.5 ns	3.5 ns	1 ns	1.3 ns	0%	27%
1000 Ω	.001 pF	29 ps	27 ps	8.6 ps	11.4 ps	3%	26%
1000 Ω	.01 pF	74 ps	75 ps	22 ps	27 ps	1%	16%
1000 Ω	.1 pF	564 ps	540 ps	174 ps	180 ps	2%	2%
1000 Ω	1 pF	5.4 ns	5.2 ns	1.7 ns	1.7 ns	4%	2%

III. Conclusions

A simple yet accurate expression for the output of a CMOS inverter driving a resistive-capacitive load is presented. With this expression, equations characterizing the propagation delay and transition time of a CMOS inverter driving an RC load are presented.

References

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[3] H. Shichman and D. A. Hodges, "Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-3, No. 3, pp. 285–289, September 1968.

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