Crosstalk Between Loosely Coupled Interconnect

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Abstract— **Interconnect in VLSI circuits is best modeled as a lossy transmission line in high speed integrated circuits [1]. An analytical expression for the coupling noise between interconnect is presented to estimate the peak noise voltage on a quiet line based on the assumption of the interconnections being loosely coupled. The closed form expressions are also applied to the condition of varying load impedance. The estimated error of the peak noise amplitude at the near end of the quiet line is less than 15% with a high loss and non-matching load conditions.**

I. Introduction

An analysis of two coupled lossy transmission lines in a homogeneous medium is presented in this paper. The analytical equations are derived from time domain differential equations using Laplace transforms and the assumption of a loosely coupled interconnect, *i.e.*, the coupling capacitance and the mutual inductance are assumed to be less than 30% of the self-capacitance and the self-inductance, respectively. The peak noise (or crosstalk) voltage is predicted based on these analytical equations. The coupling noise on the quiet (or victim) line reaches a steady state value over a period of time. However, if the peak noise voltage is greater than the threshold voltage of the logic circuit, the crosstalk noise may cause a circuit malfunction and/or dissipate extra power. In practice, the peak noise voltage (or maximum amplitude) is more important than the detailed shape of the noise waveform, since the peak noise voltage must be less than the logic threshold voltage to avoid a logic malfunction, particularly for noise sensitive digital circuits. Therefore, this analysis is focused on peak noise voltage (or maximum amplitude) estimation rather than modeling the complete noise waveform. The derived expressions are also applied to lossy transmission lines, where the error is within 15% for the near end coupling noise and 25% for the far end coupling noise. The accuracy of the maximum noise amplitude predicted at the near end is within 15% for a variety of load impedances.

II. Derivation of Closed Form Expressions

Consider two loosely coupled lossy transmission lines (shown in Figure 1), with similar impedance characteristics, *i.e.*, R, L, and C are the same for each line. Line 1 is the active (or aggressor) line and line 2 is the quiet (or victim) line. L_m and C_m are the coupling inductance and capacitance per unit length, respectively, between line 1 and line 2.

Laplace transforms are used to solve the time domain differential equations characterizing this structure [2].

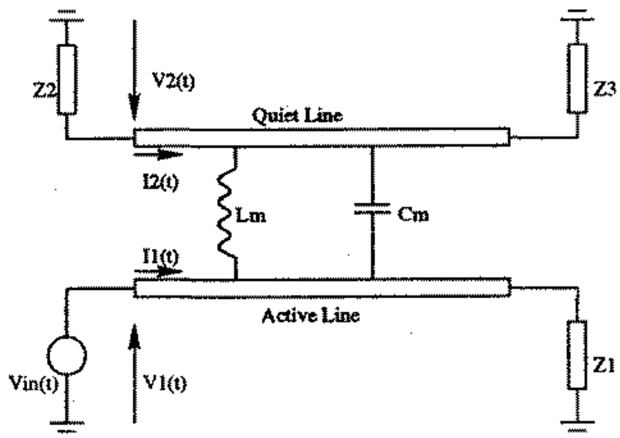

Fig. 1. Two coupled lossy transmission lines

A. Near-end noise voltage

For the near end coupling noise voltage, *i.e.*, $x = 0$.

$$V_{NE}(s) = \frac{1}{4}\left(\frac{sL_m}{R+sL} + \frac{C_m}{C}\right)(1-e^{-2\gamma l})V_{in}(s). \qquad (1)$$

Assume the input is a fast ramp signal $v_{in}(t) = V_{dd}/\tau_r[tu(t) - (t-\tau_r)u(t-\tau_r)]$. The first constraint for τ_r is $\tau_r \leq \tau_0$, where τ_0 is the time of flight delay of the signal through the transmission line and $\tau_0 = \sqrt{LC}l$. This constraint requires that the interconnect inductance cannot be neglected. The second constraint is from the assumption of $\omega L \gg R$. The frequency corresponding to this rise time is $\omega = 2\pi * 0.33/\tau_r = 2.0/\tau_r$. The requirement becomes $2\tau_1/\tau_r \gg 1$, where $\tau_1 = L/R$. $e^{-2\gamma l} \approx e^{-2s\tau_0 l - Rl/Z_0}$, where Z_0 is $\sqrt{L/C}$.

Using an inverse Laplace transform, the near end noise voltage $V_{NE}(t)$ in the time domain is

$$\begin{aligned} V_{NE}(t) &= 0.25(V_o(t) - e^{-Rl/Z_0}V_o(t-2\tau_0)), \\ V_o(t) &= \frac{V_{dd}}{\tau_r}\frac{L_m}{L}(V_p(t) - V_p(t-\tau_r)) + \frac{C_m}{C}V_{in}(t), \\ V_p(t) &= \tau_1(1-e^{-t/\tau_1})u(t). \end{aligned} \qquad (2)$$

B. Far-end noise voltage

For the far end noise voltage, where $x = l$,

$$V_{FE}(s) = -\frac{1}{2}\frac{s^2L_mC - sRC_m - s^2LC_m}{\gamma} le^{-\gamma l}V_{in}(s). \qquad (3)$$

For a fast ramp input signal, $V_{in}(s)$ is inserted into (3), permitting an inverse Laplace transform to be used to determine the far end coupling noise voltage $V_{FE}(t)$ in the time domain.

$$\begin{aligned} V_{FE}(t) \;=\; & -\frac{1}{2}\tau_0 e^{-\frac{Rl}{2Z_0}} \frac{V_{dd}}{\tau_r}(\frac{L_m}{L}(e^{-\frac{t-\tau_0-\tau_1}{2\tau_1}} \\ & u(t-\tau_0-\tau_1) - e^{-\frac{t-\tau_0}{2\tau_1}} u(t-\tau_0)) \\ & -\frac{C_m}{C}(u(t-\tau_0) - u(t-\tau_0-\tau_1)) \\ & -\frac{R}{2L}((t-\tau_0)u(t-\tau_0) - \\ & (t-\tau_1-\tau_0)u(t-\tau_0-\tau_1)))). \end{aligned} \quad (4)$$

III. Comparison with Simulation

To verify the accuracy of these analytical expressions, a criterion is defined to measure the error of these closed form approximations. This criterion quantifies the degree to which the predicted peak noise voltage deviates from the simulated peak noise voltage. This criterion can be used to evaluate the accuracy of these analytical equations. The criteria is defined mathematically as

$$\epsilon_{peak} = |V_p - V_s|/|V_s|, \quad (5)$$

where V_p is the value of the peak noise voltage predicted by the analytical expressions, and V_s is the peak noise voltage obtained from a circuit simulator (SPICE).

The parameters used in the SPICE simulation are $R = 5\ \Omega/cm$, $C = 1\ pF/cm$, $L = 2\ nH/cm$, $L_m/L = 0.2$, $C_m/C = 0.1$, $l = 2\ cm$, $V_{dd} = 5.0\ V$, $\tau_r = 80\ ps$ and $N = 20$. The load at each end is $Z_1 = Z_2 = Z_3 = Z_0 = \sqrt{L/C} = 44.72\ \Omega$. Both the analytical and simulation results are depicted in Figures 2 and 3 for the near end and the far end coupling noise voltage, respectively. The analytically derived noise waveform exhibits error at the far end since the phase difference is neglected. The numerical (SPICE) solution predicts the effect of the phase difference but requires significant computation time.

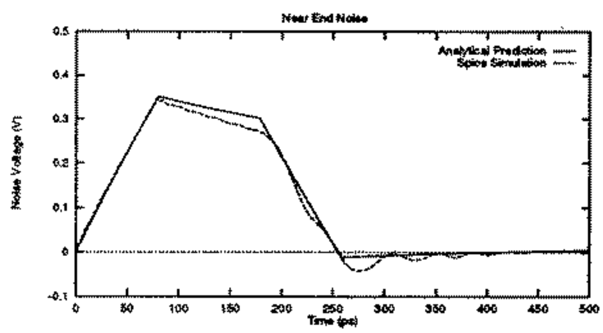

Fig. 2. Near end noise

IV. Discussion

In the design of high speed VLSI circuits, it is important to be able to predict coupling noise at the system (or chip) level. This information permits certain techniques to be used to avoid circuit malfunction or extra power consumption caused by the coupling crosstalk noise. The design cycle and cost can therefore be reduced as well as improving circuit reliability.

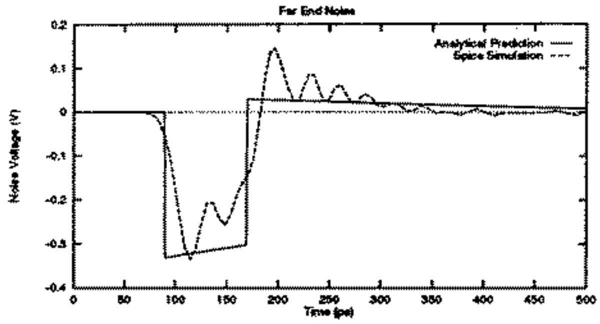

Fig. 3. Far end noise

Two assumptions are made in the development of these closed form expressions. The first assumption is that the adjacent interconnect is loosely coupled. The loosely coupling condition is typically accurate in VLSI interconnect structures of practical interest.

The constraint that the rise time is less than the time of flight is the second assumption, *i.e.*, $2\tau_1/\tau_r \gg 1$ and $\tau_r < \tau_0$. If $\tau_r < \tau_0$, interconnect inductance must be considered in the interconnect model. If $2\tau_1/\tau_r \gg 1$, *i.e.*, $\omega L > R$, the interconnect should be modeled as a low loss transmission line. Three different regions of operation are defined: condition 1: $\tau_1/\tau_r = 1$, condition 2: $\tau_1/\tau_r = 2$, and condition 3: $\tau_1/\tau_r = 4$. The total line resistance (Rl) changes from 0 to $0.5Z_0$ for each condition. The error is within 15% at the near end and 25% at the far end for the worst case, *i.e.*, $Rl/Z_0 = 0.5$ and $\tau_1/\tau_r = 1$. The total line resistance affects the predicted peak noise voltage at the far end more than at the near end. If the interconnect is modeled as a high loss transmission line ($Rl \leq 0.5Z_0$), these analytical equations remain highly accurate.

If the load impedance does not match the line impedance, the coupling noise will oscillate before the signal reaches a steady state voltage because the signal is reflected back from the load. The maximum amplitude of the crosstalk voltage (the absolute value of the peak noise voltage) is used to measure the error between the simulation and the analytical results. Both the load end impedances of line 1 and line 2 are varied, where Z_1/Z_0 is in the range of 0.2 to 50 and Z_3/Z_0 is in the range of 0.5 to 10. The worst case error is within 15% except for small load impedances, a situation not typically seen in CMOS VLSI circuits.

V. Conclusion

Analytical equations are presented in this paper to serve as a means for efficiently and accurately estimating the peak noise voltage in lossy interconnects with CMOS gate terminations. Worst case errors within 15% are demonstrated at the near end and 25% at the far end of the victim interconnect line.

References

[1] H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Addison-Wesley Publishing Company, 1990.

[2] K. T. Tang and E. G. Friedman "Peak Noise Prediction in Loosely Coupled Interconnect," submitted to *1999 IEEE International Symposium on Circuits and Systems*.