Substrate Noise Distribution and Placement of Substrate Contacts to Alleviate Substrate Noise in Epi and Non-Epi Technologies (Draft)

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Abstract— **An analysis of substrate noise distributions in epi and non-epi technologies is presented. A strategy for placing substrate contacts in epi and non-epi technologies in order to control substrate noise spreading, reduce noise, and maintain uniform noise is developed. This strategy is particularly applicable to improving the noise immunity of digital circuits in mixed-signal smart-power systems.**

I. The problem and the solution

The noise immunity of digital circuits in a mixed-signal smart-power environment requires analysis and improvement in order to make possible reliable systems-on-a-chip (SOC) integration. The magnitude of the substrate noise together with related nonuniformities within the substrate have been shown to be the two primary factors that influence the noise behavior of a digital circuit [1, 2].

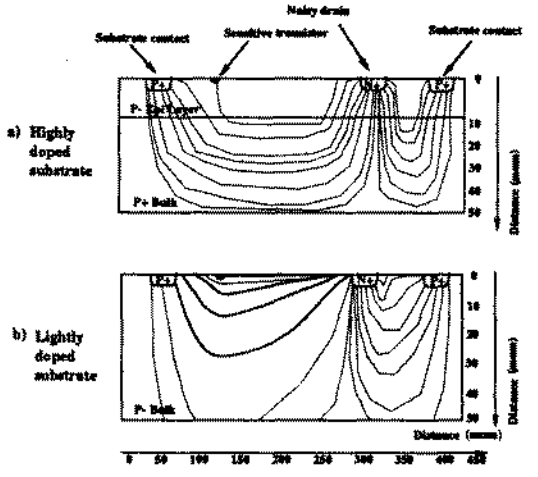

Fig. 1. The current flow lines for a lightly and highly doped substrate.

If the noise within the substrate is uniform, it has been shown that only a large noise amplitude, as compared to the case where the noise is nonuniform, may affect the correct operation of a digital circuit [2]. Accordingly, in smart-power applications, for the improved noise immunity of digital circuits, the noise within the substrate should be uniform and below a certain catastrophic level for both epi and non-epi technologies.

Several strategies at different levels in the design process can be used to obtain a uniform and low substrate noise, such as technology, circuit, or physical design levels. The focus of this paper is physical design, with the principal objective of evaluating the influence of substrate contacts placement in obtaining a uniform and low magnitude substrate noise distribution in both epi and non-epi technologies.

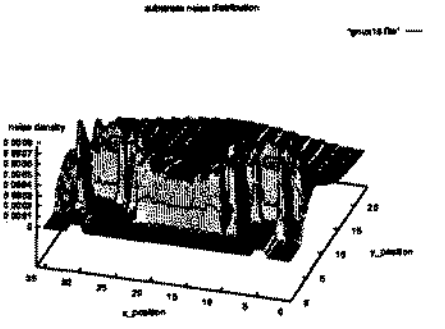

Fig. 2. A magnified front view of a noise distribution for a non-epi technology

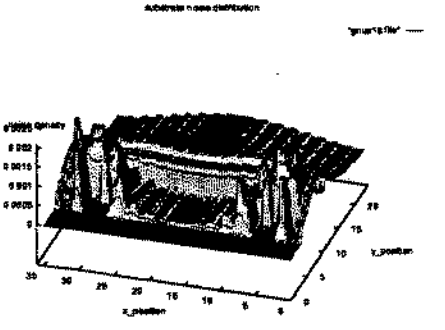

Fig. 3. An example of a substrate noise distribution for an epi technology

To achieve this objective, a thorough analysis of the substrate noise distributions corresponding to significant practical placement of the substrate contacts has been performed. The basis of this analysis consists of a methodology developed for generating three-dimensional substrate noise distributions in a two-dimensional section of the substrate. The substrate is modeled as a resistive mesh and the noise source is modeled as a constant current source. The procedure to determine the distribution of the substrate noise is as follows: Several substrate contact placement configurations have been analyzed using the Cadence Spectre [3] simulator. A program has been developed to process the files generated by the simulator in order to determine the current through each resistor of

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the substrate resistive mesh. These currents are plotted to obtain a distribution of the substrate noise. The flow of the substrate noise into the substrate has been qualitatively described by Wooley [4] (see Fig. 1). Note that for a non-epi technology, the substrate noise travels primarily at the substrate surface, while for an epi technology, the substrate noise travels primarily at the epi-bulk interface. Examples of the derived three-dimensional noise distributions for epi and non-epi technologies are shown in Figs. 2 and 3. The major difference between the two technologies are primarily due to the low resistivity bulk of an epi technology, which greatly affects the placement of the substrate contacts in the two technologies so as to reduce the noise magnitude and improve the noise uniformity.

Fig. 4. Efficient multiple substrate contacts placement in a non-epi technology

In order to minimize substrate noise in non-epi technologies, two substrate contacts SC1 and SC2 must satisfy the following rule: the associated resistances $R1$ and $R2$ to the L1 and L2 distances, as shown in Fig. 4, must satisfy

$$\frac{R_1}{R_2} \ll 1. \tag{1}$$

To minimize $R1$, SC1 must be placed as close as possible to the noisy drain, as shown in Fig. 5. A wide substrate contact is beneficial.

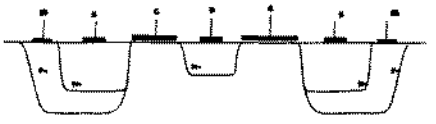

Fig. 5. Placement of a ring surrounding a noisy drain

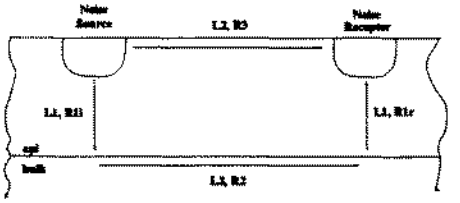

Fig. 6. Resistance distribution between the noise source and a substrate contact for an epi technology

For an epi technology, two methods are presented to reduce the noise level. The first method reduces the noise injected into the bulk by the noise source. Referring to Fig. 6, reducing the noise injected into the bulk is equivalent to placing a substrate contact between the noise source and the noise receptor (substrate contact) in order to maximize the noise that travels along the substrate surface.

The necessary condition is (see Fig. 6):

$$kL_2 \ll 2kL_1 + L_2, \tag{2}$$

where L_1 is the thickness of the epi layer and $\rho_{epi}/\rho_{bulk} = k$ (the doping of the epi layer is k times the doping of the bulk). Multiple substrate contacts that satisfy these conditions are beneficial.

The noise level in an epi technology is reduced according to a second method by collecting a major portion of the noise from the bulk with two substrate contacts placed as shown in Fig. 7. The objective is for SC1 to collect significantly more noise than SC2. Note that between the noise source and SC1, the noise may travel either mostly through the epi layer if (2) is satisfied, or mostly through the bulk. Defining R_m as the smallest resistance between the two resistances of the two noise paths, the condition for SC1 to collect a large noise from the bulk is

$$R_m \ll R_5 + R_1. \tag{3}$$

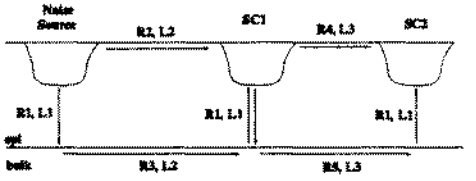

Fig. 7. Efficient multiple substrate contacts placement in an epi technology

Note that in order to satisfy (3), L_3 must be significantly larger than either L_2, or L_1 and L_2. Due to the low resistivity of the bulk, L_3 must be larger than ρ_{epi}/ρ_{bulk} times the equivalent distance through the epi layer. A large L_3 translates into an inefficient use of on-chip area. However, this solution is viable for certain applications.

II. Conclusions

The placement of substrate contacts in epi and non-epi technologies has been analyzed. A methodology to derive three-dimensional substrate noise distributions has also been developed. Major differences between the two technologies have been noted. First order expressions for efficient substrate contact placement in both epi and non-epi technologies in order to minimize the noise while obtaining a uniform noise distribution have also been presented.

References

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