The Next Bottleneck in High Speed VLSI: Interconnect Noise

Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, NY

Abstract

This presentation will summarize a series of active research topics on interconnect noise in high speed digital integrated circuits. The focus of this presentation is on interpreting, designing, and compensating for the effects of RLC interconnect impedances rather than developing RLC extraction and simulation algorithms.

In order to ascertain whether a section of interconnect should be modeled as either an RC or an RLC impedance, figures of merit will be described to determine how best to model either a line or a tree. One result of this effort is evidence demonstrating that there is a range of interconnect length for which inductance effects becomes significant. Also, the traditional quadratic dependence of the propagation delay on the length of the interconnect for RC lines approaches a linear dependence as inductance effects increase which dramatically affects the repeater insertion process in on-chip interconnect. Closed form solutions for the propagation delay, rise time, overshoots, and settling time of signals in an RLC tree will also be presented. These solutions maintain the same accuracy characteristics as the Elmore delay for RC trees while preserving the simplicity and recursive characteristics of the Elmore delay and considers all damping conditions of an RLC circuit. These closed form solutions permit the development of figures of merit to characterize the effects of inductance at a specific node in an RLC tree rather than an RLC line.

Closed form expressions for the peak coupling noise voltage (or crosstalk) between adjacent RLC interconnect driven and loaded by CMOS circuits will also be presented. These expressions can be used to estimate the near end and far end peak voltages between aggressor and victim lines, permitting the avoidance of power consuming glitches, the latching of incorrect states, and degraded reliability. Design strategies to reduce the signal propagation delay across the line, minimize the reflections at the driver end of the line, and decrease the relaxation time of the coupled noise voltage on the quiet line will also be discussed.

Simultaneous switching noise (SSN) has become an important issue in the design of the internal on-chip power distribution networks in current integrated circuits. An inductive model is used to characterize the power supply rails when a transient current is generated by simultaneously switching the on-chip registers and logic gates in a synchronous CMOS circuit. Analytical expressions characterizing the waveform and peak noise of the simultaneous switching noise voltage will be presented. Circuit and physical layout-based design techniques to minimize the effects of the peak value of the simultaneous switching noise voltage will also be discussed.

Time permitting, additional topics related to on-chip interconnect coupling noise in high speed digital circuits will also be discussed.

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Bio: Eby G. Friedman received the B. S. degree from Lafayette College, Easton,Pennsylvania in 1979, and the M. S. and Ph. D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering. From 1983 to 1991, he was employed at Hughes Aircraft Company, Carlsbad, California, rising to the position of the manager of the Signal Processing Design and Test Department. He has been in the Department of Electrical and Computer Engineering at the University of Rochester, Rochester, New York, since 1991, where he is a Professor and Director of the High Performance VLSI/IC Design and Analysis Laboratory. His current research and teaching interests are in high performance microelectronic design and analysis with application to high speed portable processors and low power wireless communications.

Dr. Friedman has authored two book chapters and many papers in the fields of high speed and low power CMOS design techniques, pipelining and retiming, and the theory and application of synchronous clock distribution networks, and has edited three books, Clock Distribution Networks in VLSI Circuits and Systems (IEEE Press, 1995), High Performance Clock Distribution Networks (Kluwer Academic Publishers, 1997), and Analog Design Issues in Digital VLSI Circuits and Systems (Kluwer Academic Publishers, 1997). Dr. Friedman is a Senior Member of the IEEE, a Member of the editorial board of Analog Integrated Circuits and Signal Processing, a member of the IEEE Circuits and Systems (CAS) Society Board of Governors, CAS liaison to the IEEE Solid-State Circuits Society (SSCS), and a Member of the technical program committee of a number of conferences.