Domino Logic with Dynamic Body Biased Keeper

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Abstract

A dynamic body biased keeper circuit technique is proposed for simultaneous power reduction and speed enhancement of domino logic circuits. The threshold voltage of the keeper transistor is dynamically modified during circuit operation to reduce contention current without sacrificing noise immunity. The proposed circuit technique is applied to wide fan-in domino OR gates. With the proposed dynamic body biased keeper circuit technique, circuit evaluation speed is increased by up to 66% while reducing power dissipation by 43% as compared to standard domino logic circuits.

1. Introduction

Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [1]. Domino logic circuits, however, are highly sensitive to noise as compared to static gates. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge [1]-[3].

Threshold voltage reduction has emerged as a popular method accompanying the scaling of the supply voltage, providing enhanced speed while maintaining dynamic power consumption within acceptable levels. Scaling the threshold voltage, however, further reduces the noise immunity of domino logic gates [1]. Moreover, exponentially increasing subthreshold leakage currents with reduced threshold voltages have become an important issue threatening the reliable operation of deep submicrometer domino logic circuits [1]-[3].

In standard domino logic gates, a feedback keeper is employed to maintain the state of the dynamic node against coupling noise, charge sharing, and subthreshold leakage current. The keeper transistor is fully turned on at the beginning of the evaluation phase in domino logic circuits. Provided that the necessary input combination to discharge the dynamic node is applied, the keeper and pulldown network transistors compete to determine the state of the dynamic node during the evaluation phase. This contention between the keeper and the pulldown network transistors degrades the circuit speed and power characteristics. A typical method for increasing noise immunity is to increase the size of the keeper. Increasing the keeper size, however, also increases the contention current. There is, therefore, a trade off between high noise immunity and high speed/energy efficient operation of domino logic gates.

To reduce contention current, a multi-phase keeper technique has been proposed in [2]. Employing two keeper transistors (an unconditional keeper and a conditional keeper), one of which is conditionally turned on if the dynamic node is not discharged during the evaluation phase, permits the contention current to be reduced. The unconditional keeper, however, needs to be sized closer to a standard domino (SD) keeper to maintain comparable noise immunity, thereby reducing the speed and power advantages of this technique. A similar technique which turns off the keeper at the beginning of the evaluation phase has been proposed in [3]. The dynamic node floats at the beginning of the evaluation phase. Therefore, although the contention current is reduced with the technique proposed in [3], reliable operation cannot be maintained in an increasingly noisy and noise sensitive on-chip environment.

A domino logic structure with a dynamic body biased keeper is proposed in this paper for simultaneous power reduction and speed enhancement in domino logic circuits. The threshold voltage of the keeper transistor is dynamically modified during circuit operation to reduce the contention current without degrading the noise immunity. The proposed circuit technique has been applied in this paper to wide fan-in domino OR gates. With the proposed dynamic body biased keeper circuit technique, the evaluation speed is enhanced by up to 66% while reducing the power dissipation by 43% as compared to standard domino logic circuits.

The operation of the proposed domino logic with a dynamic body biased keeper (DDBBK) is described in Section 2. Simulation results characterizing the delay, power, and noise immunity of the DDBBK technique as

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compared to SD are presented in Section 3. Finally, some conclusions are offered in Section 4.

2. Domino Logic with a Dynamic Body Biased Keeper

Domino logic with a dynamic body biased keeper is proposed in this paper for simultaneous evaluation delay and power reduction in domino logic circuits with little impact on noise immunity. The DDBBK circuit technique is introduced in Section 2.1. Operation of the body bias generator is described in Section 2.2.

2.1. Variable Threshold Voltage Keeper

A K input domino OR gate implemented with the proposed circuit technique is shown in Fig. 1. The DDBBK circuit technique assumes two supply voltages, V_{DD1} and V_{DD2}, where $V_{DD1} < V_{DD2}$. A representative waveform to describe the circuit operation is shown in Fig. 2.

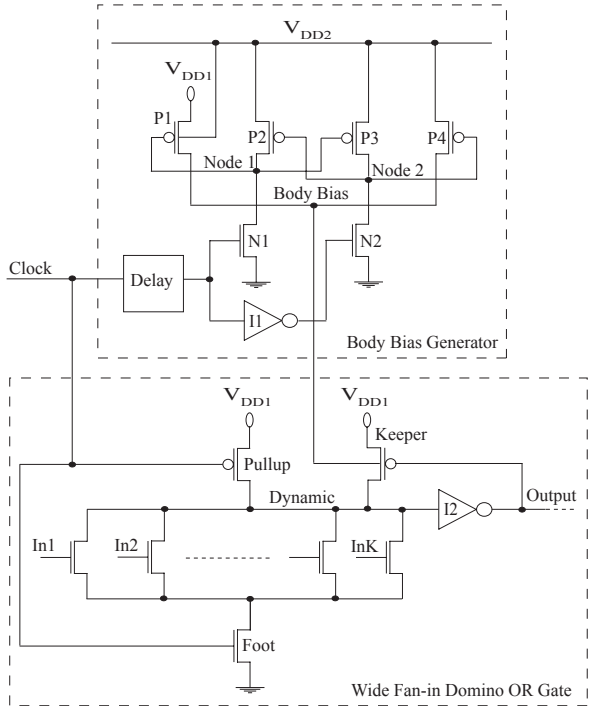

Fig. 1. K input domino OR gate with dynamic body biased keeper.

The operation of the DDBBK circuit behaves in the following manner. When the clock is low, the pullup transistor is on and the dynamic node is charged to V_{DD1}. The substrate of the keeper is charged to V_{DD2} by the body bias generator, increasing the keeper threshold voltage. The value of the high threshold voltage (high-V_t) of the keeper is determined by the reverse body bias voltage (V_{DD2} - V_{DD1}) applied to the source-to-substrate p-n junction of the keeper. The current sourced by the high-V_t keeper is reduced, lowering the contention current when the evaluation phase starts. A reduction in the current drive of the keeper does not degrade the noise immunity during precharge as the dynamic node voltage is maintained during this phase by the pullup transistor rather than the keeper.

When the clock goes high (the evaluation phase), the pullup transistor is cutoff and only a high-V_t keeper current contends with the current from the evaluation path transistor(s). Provided that the appropriate input combination that discharges the dynamic node is applied in the evaluation phase, the contention current due to the high-V_t keeper is significantly reduced as compared to standard domino. After a delay determined by the worst case evaluation delay of the domino gate, the body bias voltage of the keeper is reduced to V_{DD1}, zero biasing the source-to-substrate p-n junction of the keeper. The threshold voltage of the keeper is, therefore, lowered to the zero body bias level, thereby increasing the keeper current. The DDBBK keeper has the same threshold voltage of a standard domino keeper, offering the same noise immunity during the remaining portion of the evaluation stage (assuming the SD and DDBBK keepers are the same size).

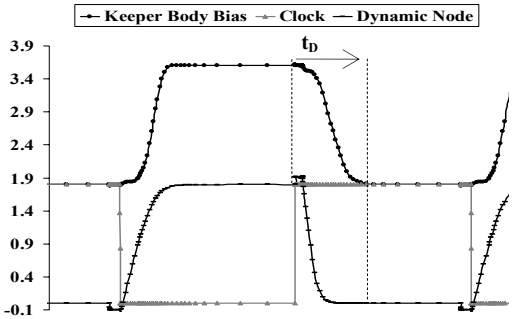

Fig. 2. Example waveform to describe the operation of the proposed DDBBK circuit technique (V_{DD1} = 1.8 volts and V_{DD2} = 3.6 volts).

2.2. Dynamic Body Bias Generator

The dynamic body bias generator (DBBG) produces an output signal swinging between V_{DD1} and V_{DD2} from an input signal swinging between ground and V_{DD1}. The DBBG generates the proper body bias voltages for the keeper with an appropriate delay, ensuring that the contention current is reduced without sacrificing noise immunity.

The operation of the DBBG is controlled by the clock signal that also controls the operational phases of the domino logic circuit. When the clock goes low, node 2 is discharged through N2, turning on P2 and P4. P1 and P3 are cutoff and the body bias voltage is increased to V_{DD2}. When the clock goes high, the domino logic circuit enters the evaluation phase. The DBBG must ensure during this stage that the keeper current is increased to the low-V_t level for higher noise immunity if the dynamic node is not discharged by the evaluation path transistors. After a delay determined by the worst case evaluation delay of the domino gate, node 1 is discharged through N1, turning on P1 and P3. P2 and P4 are cutoff and the body bias voltage is (eventually)

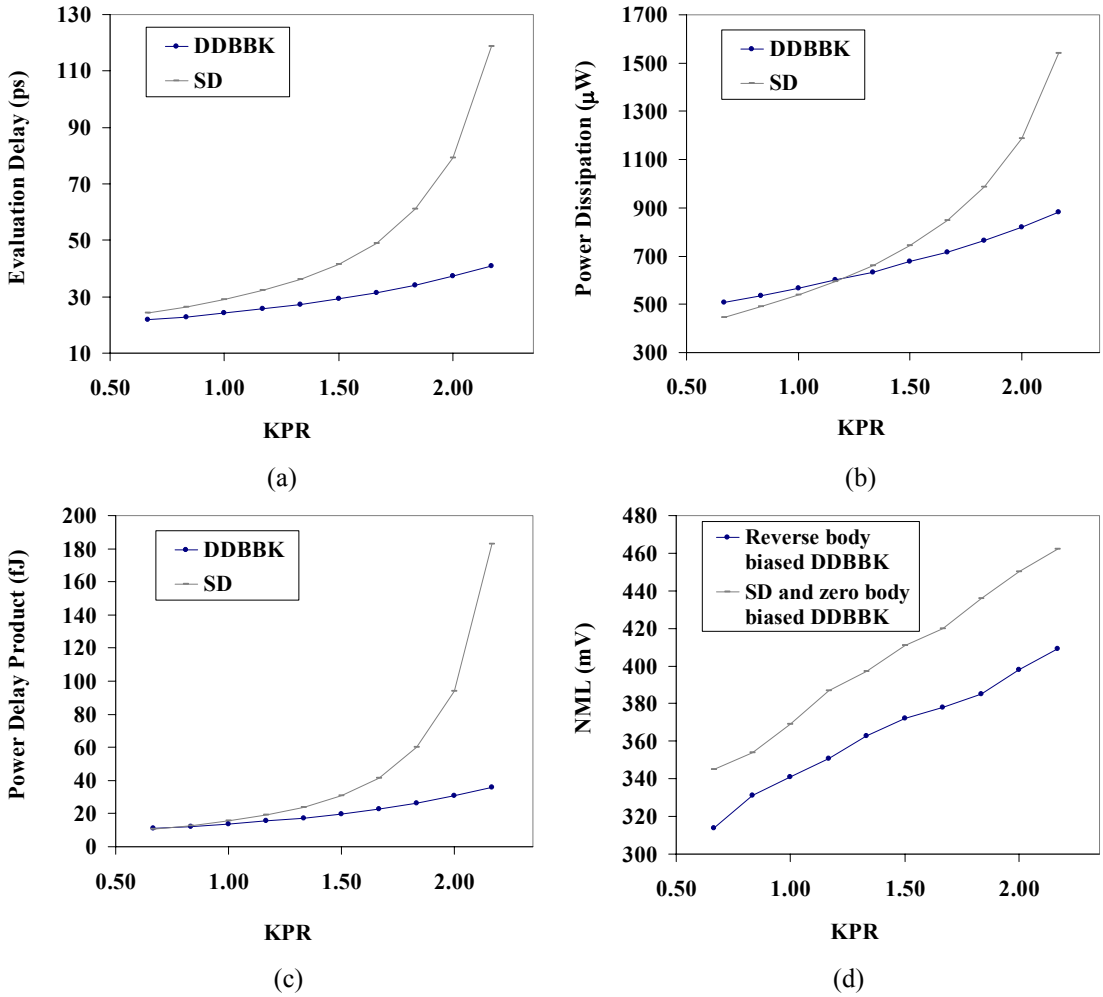

Fig. 3. SD and DDBBK simulation results for different keeper to pulldown transistor width ratios (KPR). (a) Evaluation delay. (b) Power dissipation. (c) Power delay product. (d) Noise margin low (NML).

reduced to V_{DD1} (see Fig. 2). Hence, with a time delay t_D after the clock edge, the threshold voltage of the keeper is reduced to the zero body bias level, increasing the keeper current. During the remaining portion of the evaluation phase, therefore, the noise immunity characteristics of the SD and DDBBK circuit techniques are identical.

The proposed dynamic body bias generator is operational for a wide range of values of V_{DD1} and V_{DD2}. Reductions in the delay and power can be increased by increasing V_{DD2} as compared to V_{DD1}. This change, however, also degrades the noise immunity characteristics of the domino circuit at the beginning of the evaluation phase. The appropriate reverse body bias that is applied to the keeper is determined by the target delay/power objectives while satisfying the lowest acceptable noise immunity requirement during the worst case evaluation delay of the domino gate. The highest reverse bias that can be applied to the source-to-substrate junction of a PMOS transistor for a specific technology is another factor that determines V_{DD2}. In the following analysis, V_{DD2} is chosen to be twice V_{DD1}, making the maximum keeper reverse body bias voltage equal to V_{DD1}. Significant delay and power savings are achieved with a small degradation in noise immunity of less than 12% at the beginning of the evaluation phase.

3. Simulation Results

The SD and DDBBK circuit techniques are evaluated for an eight input OR gate assuming a 0.18 μm CMOS technology. Each domino gate drives a capacitive load of 18 fF. A 1 GHz clock with a 50% duty cycle is applied to the domino logic circuits. All of the common transistors in the SD and DDBBK circuits are sized the same. All of the transistors in the dynamic body bias generator are minimum size. V_{DD1} and V_{DD2} are 1.8 volts and 3.6 volts, respectively.

To evaluate the noise immunity, a DC analysis of each circuit configuration has been evaluated. The low noise margin (NML) is used as the noise immunity metric during this analysis. The NML is defined as

$$NML = V_{IL} - V_{OL}\,, \tag{1}$$

where V_{IL} is the input low voltage defined as the DC input voltage at which the dynamic node voltage is equal to the input voltage (the unity gain point on the voltage transfer characteristic). V_{OL} is the output low voltage.

Table 1. A comparison of the evaluation delay, power dissipation, power-delay product (PDP), and NML (for maximum reverse body biased keeper) of SD and DDBBK for KPR = 2.2.

	Evaluation Delay (ps)	Power (μW)	PDP (fJ)	NML (mV)
SD	119	1540	183	462
DDBBK	41	883	36	409
Improvement	66%	43%	80%	-12%

The keeper width is a multiple of the width of a single NMOS transistor in the pulldown network and is varied to evaluate the delay, power, and noise immunity tradeoffs. During evaluation of the delay and power characteristics, only one input of the eight input OR gate is asserted while the remaining inputs are grounded. This situation represents the worst case delay condition. During evaluation of the noise immunity, the same input noise signal is applied to all eight inputs as this situation represents the worst case noise condition for a domino OR gate. The evaluation delay, power, power-delay product (PDP), and NML for SD and DDBBK as a function of the keeper to pulldown transistor width ratio (KPR) are shown in Fig. 3. The gain in delay, power, and PDP achieved by the proposed technique together with the degradation in noise margin at the beginning of the evaluation phase while a maximum reverse body bias is applied to the keeper are listed in Table 1.

The proposed dynamic body biased keeper technique is effective for enhancing the evaluation speed of domino logic circuits. As listed in Table 1, DDBBK improves the evaluation delay by 66% as compared to SD (for a KPR = 2.2). As shown in Fig. 3a, the effectiveness of the proposed technique increases with larger keeper size as the degradation in circuit speed becomes more severe due to increased contention. The enhancement in circuit speed is reduced to 10% as the KPR is reduced to 0.6.

As shown in Fig. 3b, the proposed circuit technique also lowers the power consumption for a wide range of keeper sizes. As listed in Table 1, DDBBK reduces the power by 43% as compared to SD (for a KPR = 2.2). As the keeper size is decreased, the effect of the keeper contention on the evaluation delay and circuit energy dissipation becomes smaller. The reduction in power with small keeper sizes, therefore, diminishes. Due to the energy overhead of the dynamic body bias generator circuit, the power consumption increases by 14% as compared to SD when the KPR is reduced to 0.6.

The PDP of the circuits is also illustrated in Fig. 3 to better compare the effect of the proposed dynamic body biased circuit technique on circuit performance and energy dissipation. As listed in Table 1, DDBBK offers 80% lower PDP as compared to SD (for a KPR = 2.2). As shown in Fig. 3c, the only configuration at which SD has a smaller PDP as compared to DDBBK is for a KPR = 0.6 (3% lower).

Another important metric for domino circuits is noise immunity. The proposed circuit technique slightly degrades the noise immunity as compared to SD only at the beginning of the evaluation phase. This degradation occurs for a brief amount of time until the threshold voltage of the keeper is lowered for increased noise immunity. The time delay (t_D) at the beginning of the evaluation cycle, after which the keeper current drive is increased to the low-V_t level, is determined by the worst case evaluation delay of the domino gate. The degradation in noise immunity changes between 6% and 12% under maximum reverse body bias conditions as the KPR is increased from 0.6 to 2.2. As shown in Fig. 3d, the noise immunity of DDBBK is identical to the noise immunity of SD whenever a zero body bias is applied to the keeper.

4. Conclusions

A high speed, low power domino logic circuit technique is proposed. The proposed technique dynamically changes the threshold voltage of the keeper transistor at the beginning of each cycle by biasing the body of the keeper transistor. The keeper contention current is reduced by increasing the keeper threshold voltage by applying a reverse body bias to the keeper at the beginning of the evaluation phase. Similarly, the degradation in noise immunity of DDBBK as compared to SD is avoided by reducing the keeper threshold voltage to the zero body bias level after a delay greater than the worst case evaluation delay of the domino logic circuit. Significant speed enhancement and power reductions are observed when the keeper is sized for increased noise immunity.

The DDBBK technique is shown to operate at up to a 66% higher speed while consuming 43% less power as compared to SD. DDBBK also offers reductions in PDP of up to 80% as compared to SD. The degradation in noise immunity of DDBBK as compared to SD, observed when a reverse body bias is applied to the keeper, is less than 12%.

5. References

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