Efficiency Analysis of a High Frequency Buck Converter for On-Chip Integration with a Dual-V_{DD} Microprocessor

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Abstract

An analysis of the power characteristics of a buck converter is presented in this paper. A high switching frequency is the key design parameter that simultaneously permits monolithic integration and high efficiency. A parasitic model of the buck converter is developed. With this model, a design space is determined that allows integration of active and passive devices on the same die for a target technology. An efficiency of 88.4% at a switching frequency of 477 MHz is demonstrated for a voltage conversion from 1.2 volts to 0.9 volts while supplying 9.5 amperes average current assuming an 80 nm CMOS technology. The area occupied by the buck converter is 12.6 mm^2. An analytic estimate of the efficiency is shown to be within 2.4% of simulation at the target design point. Full integration of a high efficiency buck converter on the same die with a dual-V_{DD} microprocessor is shown to be feasible.

1. Introduction

Decreasing the overall power dissipation and current demand of high performance microprocessors are the two primary reasons for implementing a dual-V_{DD} microprocessor [1]. In order to fully exploit the expected reductions in power and current, the energy overhead of a DC-DC converter while producing a second voltage level must be minimized.

Buck converters are popular due to the high efficiency and good output voltage regulation characteristics of these circuits [2]-[4]. In single power supply microprocessors, the primary power supply is typically an external (non-integrated) buck converter which converts the voltage supplied by the main power supply to a lower voltage level. In a dual-V_{DD} microprocessor, the choices are either a second external DC-DC converter, or a monolithic (both active and passive devices on the same die with the load) DC-DC converter.

Integrating a DC-DC converter with a microprocessor can potentially lower the parasitic losses as the interconnect between (and within) the DC-DC converter and the microprocessor is reduced. Additional energy savings can be realized by utilizing advanced deep submicrometer device fabrication techniques with lower parasitic energy dissipation. The efficiency attainable with a monolithic DC-DC converter is, therefore, higher as compared to an off-chip DC-DC converter.

Fabrication of a monolithic switching DC-DC converter, however, imposes a challenge as the on-chip integration of inductive and capacitive devices is required for energy storage and output signal filtering [3], [4]. Integrated capacitors and inductors above certain values are not acceptable due to the tight area constraints that exist within high performance microprocessor ICs. Another issue with integrated inductors is the poor parasitic impedance characteristics which can degrade the efficiency of the voltage regulator. The value and physical size of the passive devices required to implement a buck converter, however, are reduced with increasing switching frequencies [2]-[4]. Therefore, employing switching frequencies higher than the typical switching frequency range found in conventional DC-DC converters permits the on-chip integration of the active and passive devices of a buck converter onto the same die as a high performance microprocessor.

The efficiency characteristics of a buck converter, however, change dramatically as the switching frequency is increased. A parasitic model of a buck converter is presented in this paper. A closed form expression that characterizes the power consumption of a buck converter is proposed. The effects of scaling active and passive devices and the varying switching and conduction losses on the total power characteristics of a buck converter are examined in detail. With the proposed buck converter circuit model, a design space is presented which characterizes the integration of both active and passive devices on the same die as a dual-V_{DD} microprocessor while maintaining high efficiency for an 80 nm CMOS technology. An efficiency of 88.4% is shown for a voltage conversion from 1.2 volts to 0.9 volts while supplying 9.5 amperes maximum current.

The proposed parasitic circuit model and the closed form expression of the average power dissipation of a buck converter are presented in Section 2. With the proposed analytical model, the efficiency characteristics of the buck converter are analyzed in Section 3. Simulation results at a target design point are presented in Section 4. Finally, some conclusions are offered in Section 5.

2. Circuit Model of a Buck Converter

A circuit model has been developed to analyze the frequency dependence of the efficiency characteristics of a buck converter. The proposed circuit model for the parasitic impedances of a buck converter is shown in Fig. 1.

The buck converter output voltage is [2]

$$V_{DD2}(t) = DV_{DD1} + V_{ripple}(t), \quad (1)$$

where D is the duty cycle, V_{DD1} is the amplitude of the AC waveform generated at node 1, and $V_{ripple}(t)$ is the voltage ripple waveform observed at the output due to the non-ideal characteristics of the output filter. The inductor current $i_L(t)$, output voltage $V_{DD2}(t)$, and capacitor current $i_C(t)$ waveforms are shown in Fig. 2.

Expressions for the inductor current ripple Δi and the amplitude of the output voltage ripple ΔV_{DD2} (see Fig. 2), respectively, are [2]

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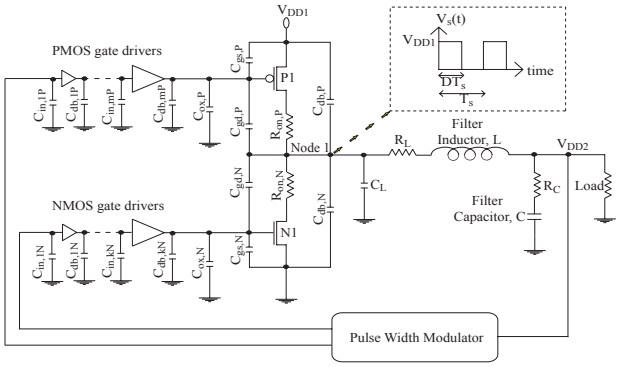

Fig. 1. Circuit model of the parasitic impedances of a buck converter.

$$\Delta i = \frac{(V_{DD1} - V_{DD2})D}{2Lf_s}, \tag{2}$$

$$\Delta V_{DD2} = \frac{(V_{DD1} - V_{DD2})D}{16LCf_s^2} = \frac{\Delta i}{8Cf_s}, \tag{3}$$

where L is the filter inductance, C is the filter capacitance, and f_s is the switching frequency.

The power consumption of a buck converter is a combination of the conduction losses caused by the resistive parasitic impedances and the switching losses due to the capacitive parasitic impedances of the circuit components. The power consumption of the pulse width modulation feedback circuit is typically small as compared to the power consumption of the power train (the power MOSFETs, MOSFET gate drivers, the filter inductor, and the filter capacitor) [2]-[4]. Therefore, only the power dissipation of the power train components is considered in the efficiency analysis.

MOSFET related power losses are analyzed in Section 2.1. An analysis of the filter inductor related losses is presented in Section 2.2. The filter capacitor related losses are discussed in Section 2.3. An analytical expression for the total buck converter power dissipation is presented in Section 2.4.

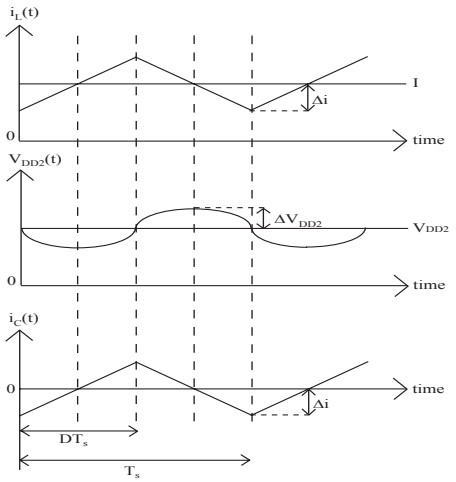

Fig. 2. Inductor current $i_L(t)$, output voltage $V_{DD2}(t)$, and capacitor current $i_C(t)$ waveforms.

2.1. MOSFET Related Power

The total power loss of a MOSFET is a combination of conduction losses and dynamic switching losses. The conduction power is dissipated in the series resistance of the transistors operating in the active region. The dynamic power is dissipated each switching cycle while charging/discharging the gate oxide, gate-to-source/drain overlap, and the drain-to-body junction capacitances of the MOSFETs.

The MOSFET width is optimized to minimize the MOSFET related power dissipation. The total optimized MOSFET related power consumption of a buck converter $P_{tot,MOS}(opt)$ is

$$P_{tot,MOS}(opt) = a\sqrt{(I^2 + \frac{\Delta i^2}{3})f_s}, \tag{4}$$

$$a = 2\left(\sqrt{R_{0NMOS}(1-D)E_{NMOS}} + \sqrt{R_{0PMOS}DE_{PMOS}}\right), \tag{5}$$

$$E = 2(C_{ox} + C_{gs} + 2C_{gd} + C_{db})V_{DD1}^2, \tag{6}$$

where R_0 is the equivalent series resistance of a 1 μm wide transistor, C_{ox}, C_{gs}, C_{gd}, and C_{db} are the gate oxide, gate-to-source overlap, gate-to-drain overlap, and the drain-to-body junction capacitances, respectively, of a 1 μm wide MOSFET.

2.2. Filter Inductor Related Power

Some portion of the total energy consumption of a buck converter occurs due to the series resistance and the stray capacitance of the filter inductor. Integrated spiral inductors have a high series resistance and other intrinsic problems associated with the planar design which makes these inductors area inefficient [5]. Therefore, integration of a spiral inductor with sufficient inductance is not feasible for a high performance microprocessor. A novel low resistance inductor has been recently reported [5]. Assuming the inductor parasitic impedances scale linearly with the inductance [6], the total inductor power loss is

$$P_{tot,inductor} = b\left[\frac{I^2}{\Delta i f_s} + \frac{\Delta i}{3f_s} + \frac{C_{L0}V_{DD1}^2}{R_{L0}\Delta i}\right], \tag{7}$$

$$b = \frac{(V_{DD1} - V_{DD2})DR_{L0}}{2}, \tag{8}$$

where C_{L0} and R_{L0} are, respectively, the parasitic stray capacitance and parasitic series resistance per nH inductance.

2.3. Filter Capacitor Related Power

The filter capacitance effects the total power consumption of a buck converter due to the effective series resistance (esr) R_C. Assuming the integrated capacitor is implemented utilizing the gate oxide capacitance of a MOSFET, the total power dissipation of a filter capacitor is

$$P_{tot,capacitor} = df_s\Delta i, \tag{9}$$

$$d = \frac{8R_{0cap}L_{cap}C_0\Delta V_{DD2}}{3}, \tag{10}$$

where R_{0cap} is the series resistance of a MOSFET with a 1 μm width, C_0 is the gate oxide capacitance per μm^2, and L_{cap} is the channel length of the MOSFET.

2.4. Total Power Consumption of a Buck Converter

Combining (4), (7), and (9), the total power consumption of a buck converter is

$$P_{buck} = a\sqrt{(I^2 + \frac{\Delta i^2}{3})f_s} + b\left[\frac{I^2}{\Delta i f_s} + \frac{\Delta i}{3f_s} + \frac{C_{L0}V_{DD1}^2}{R_{L0}\Delta i}\right] + df_s\Delta i, \tag{11}$$

where a, b, and d are given by (5), (8), and (10), respectively.

The power dissipation of a buck converter is a strong function of the switching frequency and the inductor current ripple. As given by (11), depending upon the ratio of the inductor and MOSFET related components of the total buck converter power dissipation, the efficiency can actually increase with increased switching frequency and current ripple within a specified (f_s, Δi) range. This observation agrees with the mathematical analysis presented in Section 3.

3. Efficiency Analysis of a Buck Converter

The efficiency of a buck converter is

$$\eta = 100 \times \frac{P_{load}}{P_{load} + P_{buck}}, \quad (12)$$

where P_{load} is the average power delivered to the load and P_{buck} is the average total internal power consumption of a buck converter as given by (11).

In the following analysis, it is assumed that the two power supply voltage levels used in a microprocessor are 1.2 volts (V_{DD1}) and 0.9 volts (V_{DD2}). The average load current demand (I) is assumed to be 9.5 amperes. A mathematical analysis assuming an 80 nm CMOS technology is performed. The allowable output voltage ripple ΔV_{DD2} is assumed to be 5 mV. The global maximum efficiency point is discussed in Section 3.1. An analysis of the buck converter efficiency with a limited allowable on-chip integrated filter capacitance is presented in Section 3.2.

3.1. Circuit Analysis for Global Maximum Efficiency

The efficiency variation of the buck converter is shown in Fig. 3 for 0.1 amperes < Δi < 9.5 amperes and 10 MHz < f_s < 4 GHz. The "z" axis represents the efficiency in Fig. 3. The MOSFET, inductor, and filter capacitor components of the total power dissipation of the buck converter are shown in Fig. 4. The "z" axis represents the power (in watts) in Fig. 4.

As shown in Fig. 4, the MOSFET and capacitor related power increases while the inductor power decreases monotonically with increasing switching frequency and inductor current ripple. The capacitor power, however, is negligibly small (less than 1%) as compared to the inductor and MOSFET power over the entire (f_s, Δi) range of analysis. The capacitor losses, although included in the analysis, are therefore not further discussed. The efficiency behavior of the buck converter is characterized by the competing inductor and MOSFET losses. At low f_s and Δi, the buck converter power is primarily dissipated in the filter inductor. As the switching frequency and current ripple are increased, the inductance is dramatically reduced, lowering the parasitic losses of the inductor. The MOSFET power increases, however, with increased f_s and Δi. At a certain range of (f_s, Δi), the inductor losses dominate the total losses; hence, the total power dissipation of the converter decreases with increasing switching frequency and inductor current ripple. After the peak efficiency point is reached, increasing MOSFET losses begin to dominate the total buck converter power dissipation. Hence, the efficiency degrades with further increases in f_s and Δi.

An optimum switching frequency and inductor current ripple pair exists that maximizes the efficiency of the buck converter. The global maximum efficiency point is 92% at a switching frequency of 114 MHz and a current ripple of 9.5 amperes. The required filter capacitance and inductance at this operating point are 2083 nF and 104 pH, respectively. This filter capacitance would occupy an unacceptably large area on a microprocessor die for the target technology. Therefore, fabrication of a monolithic DC-DC converter at this maximum efficiency operating point is not feasible.

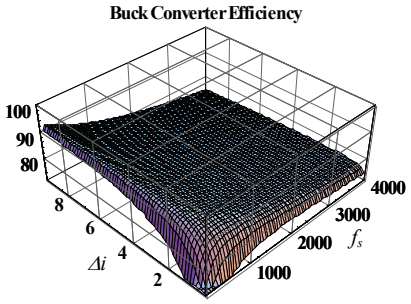

Fig. 3. Buck converter efficiency as a function of f_s and Δi.

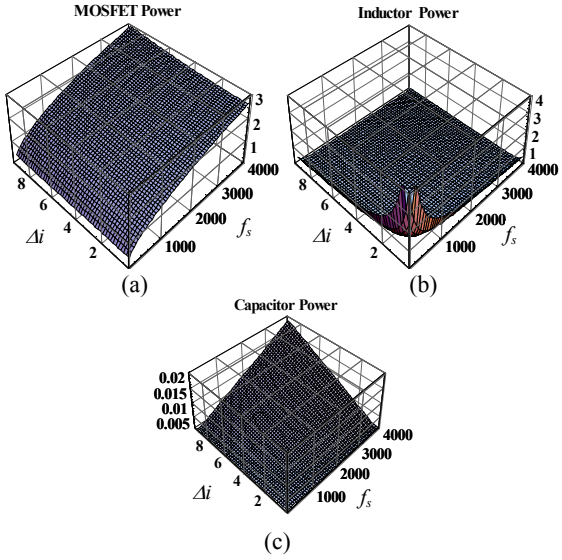

Fig. 4. Distribution of the total power dissipation of the buck converter among different circuit components. (a) MOSFET related power. (b) Filter inductor related power. (c) Filter capacitor related power.

3.2. Circuit Analysis with Limited Filter Capacitance

Because of the area overhead of an integrated capacitor, the filter capacitance that can be integrated on a microprocessor die is limited. The filter capacitance is swept between 100 nF and 1 nF to evaluate the effect of a reduced filter capacitance on the circuit configuration and the resulting efficiency characteristics of a buck converter. The circuit configurations at each operating point offering the highest efficiency (η) are listed in Table 1.

As listed in Table 1, an efficiency of 88.4% is achievable with a 100 nF filter capacitance. The area occupied by the maximum efficiency configuration with a 100 nF filter capacitance is 12.6 mm^2. The maximum achievable efficiency reduces to 74.7% as the filter capacitance is lowered to 1 nF. As the filter capacitance is reduced, the filter inductance and switching frequency are both increased to satisfy the output voltage and current requirements. Therefore, both the switching and conduction power dissipation of the power MOSFETs and the filter inductor increases with reduced filter

capacitance, thereby degrading the efficiency.

With this analysis, a design space is presented that supports full integration of a high efficiency buck converter onto a microprocessor die. Note that with increased capacitor space available on the microprocessor die, the attainable efficiency increases towards the global maximum value of 92%. Another advantage of a higher filter capacitance is the lower switching frequency requirement which improves circuit reliability and makes the design of the pulse width modulation circuitry less complicated.

Table 1. Variation of the buck converter circuit parameters with different filter capacitances.

C (nF)	η (%)	f_s (MHz)	L (pH)	W_{P1} (mm)	W_{N1} (mm)
1	74.7	3174	279	50.8	20.2
10	82.8	1227	187	81.7	32.5
100	88.4	477	124	131.9	52.5

4. Simulation Results

The buck converter circuit configuration that produces the maximum efficiency (see Table 1) with a filter capacitance of 100 nF and an output voltage ripple of 5 mV is evaluated assuming an 80 nm CMOS technology. The analytical expression [see (11)] for the total power consumption of a buck converter is effective in estimating the efficiency characteristics. The buck converter efficiency determined by simulation at the target design point is 86% which is only 2.4% different than the efficiency determined from the analytical expression as listed in Table 1.

The converter output voltage (while supplying 9.5 amperes of DC current to the load) is shown in Fig. 5a. The peak-to-peak output voltage ripple is actually lower than the analytical expectation of 10 mV. This behavior is observed since the voltage drop across the equivalent parasitic resistances of the power MOSFETs and the filter inductor have been neglected during the steady-state analysis applied in the development of (2) and (3).

The response of the buck converter to sudden changes in current demand at the load from the minimum to the maximum is evaluated. A 10% output voltage window is allowed as the average current demand of the microprocessor swings from a minimum (I_{min} = 0.25*I) to a maximum (I). The waveforms for the DC-DC converter output response for a current step from I_{min} (standby leakage current) to I are illustrated in Figs. 5b and 5c. As shown in Fig. 5b, the response time for the buck converter to settle within the allowed 10% voltage window after the microprocessor transitions to the maximum current mode from the idle mode is 87 nS. One solution that provides a stable voltage to the microprocessor until the buck converter output settles within the 10% window is to use several high speed linear regulators distributed around the microprocessor die that are activated whenever the buck converter output voltage drops below the lower limit of the 10% window. The overall impact of these low efficiency linear regulators [2] on the energy dissipation of the microprocessor is small as the current steps between the two extremes do not frequently occur.

5. Conclusions

An analysis of the power characteristics of a standard DC-DC converter topology, a buck converter, is provided in this paper. A parasitic model of the buck converter is presented. With this model, a closed form expression for the total power dissipation of a buck converter is proposed. An analysis over a range of design parameters is evaluated, permitting the development of a design space for full integration of active and passive devices on the same die as a microprocessor for a target technology. Two major challenges for a monolithic switching DC-DC converter are the area occupied by the integrated filter capacitor and the effect of the parasitic impedance characteristics of the integrated inductors on the overall efficiency characteristics of a switching DC-DC converter. A high switching frequency is the key design parameter that enables the integration of a high efficiency buck converter on the same die as a dual-V_{DD} microprocessor.

It is shown that an optimum switching frequency and inductor current ripple pair that maximizes the buck converter efficiency exists for a target technology. The global maximum efficiency point is 92% at a switching frequency of 114 MHz and a current ripple of 9.5 amperes. The required filter capacitance and inductance at this operating point are 2083 nF and 104 pH, respectively.

The effects of reducing the filter capacitance due to the tight area constraints on a microprocessor die have been examined. An efficiency of 88.4% (82.8%) is shown at a switching frequency of 477 MHz (1.23 GHz) with a total area of 12.6 mm^2 (1.3 mm^2), primarily occupied by the filter capacitance of 100 nF (10 nF). The analytic model for the converter efficiency is within 2.4% of the simulation results at the target design point (C = 100 nF).

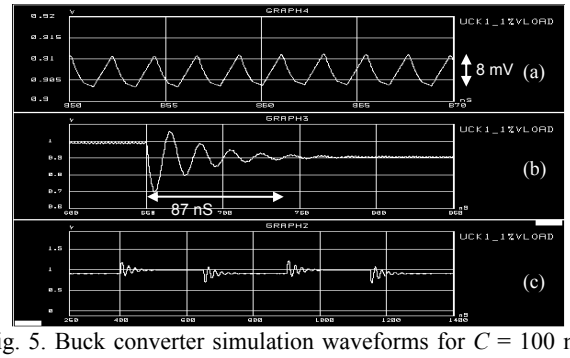

Fig. 5. Buck converter simulation waveforms for C = 100 nF. (a) Output voltage ripple $V_{ripple}(t)$. (b) Buck converter response to a change in load current from I_{min} to I. (c) Buck converter response to the step current changing between I_{min} and I.

6. Acknowledgement

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