steady state bit error probability performance and the bit error probability learning curves. Both conventional and differential decoding are considered.

Decision-directed implementation of these phase estimation algorithms are also investigated utilizing Markov chain theory. The output of the decision-directed EW estimator is shown to be a first order Markov chain. The corresponding theory is developed for the AWGN channel resulting in a description of the phase error process by the Chapman-Kolmogorov equation. Numerical results are obtained for the steady state phase error probability density function and the resulting bit error probability.

A rigorous Markov analysis revealed several anomalies of open loop phase estimation of digitally modulated signals. These anomalies for the decision-directed structures are a hangup condition and a phenomeon similar to cycle slipping, and for nonlinear structures an equivocation phenomenon. The probability of occurrence and the effect on bit error probability are considered for each of these anomalies. Differential encoding is considered as a partial solution to the problems caused by these anomalies in decision-directed structures. (Copies available exclusively from Micrographics Department, Doheny Library, USC, Los Angeles, CA 90089-0182.)

Augmentable object-oriented parallel processor architectures for real-time computer-generated imagery. Fleischman, Ross Morris, Ph.D. *University of Florida*, 1988. 168pp. Chairman: John Staudhammer **Order Number DA8923962**

The hardware architecture of a system for real-time computer-generated imagery (CGI) is presented that combines augmentability, modularity, organizational simplicity, and parallelism. This architecture is a functional, highly-modular, parallel processor approach that is well suited for employing VLSI technology. It is a generic structure that can grow with technological advances and can accommodate a full range of CGI systems that demand different performance requirements through one basic set of modules.

The CGI process contains five fundamental components: input, modeling, rendering, compositing, and output. This architectural approach extends specialized hardware into both the compositing and output components, which allows the definition of a generic framework for building systems appropriate for many simulations. The system architecture performs image synthesis in parallel by partitioning the image generation task in object space with each partition assigned to an individual autonomous object generator. Objects are rendered independently from each other, and when complete they are automatically composited by the hardware for display. This process is repeated at a rate suitable for real-time animation.

The picture representation accepts transparent, semitransparent, and fully opaque surfaces. Hardware facilities perform automatic hidden surface removal with antialiasing and atmospheric attenuation inclusion. An approximation for surface intersection is performed, and a subpixel control mechanism is provided.

The parallel hardware algorithm is classified as a compute-aggregate-broadcast paradigm: a compute phase generates objects, an aggregate phase combines the objects into a scene, and a broadcast phase displays the scene. Its system framework maintains a synchronous feed-through structure that allows enlargement by either dynamic or static additions. System improvement is accommodated by adding modules that incrementally improve system performance and scope. This reduces difficulties associated with the incorporation of new systems to introductions of new modules, thereby lengthening system life.

Multidimensional signal set design for transmission over parallel channels. Fortier, Paul, Ph.D. *Stanford University*, 1989. 136pp. Adviser: John M. Cioffi **Order Number DA8925865**

The design of efficient multidimensional signal sets has gained importance with the development of coded modulation systems. The total coding gain of such systems is a function of their fundamental coding gain and their shaping gain. The fundamental coding gain depends on the encoder, while the shaping gain depends on the region of N-dimensional space in which the signal set is contained. While coding gains of 3–5 dB are relatively easy to obtain, it might be better to invest further complexity in trying to improve the shaping gain of a system. In all approaches, the improvements in shaping gain come at the expense of increased encoder complexity. We present a very efficient encoder implementation, called the "Shell Construction", that permits practically the maximum (N-sphere) shaping gain to be realized with low complexity in 4, 8, and even 16 dimensions. We also specifically consider the important case where parallel channels with different gains and number of transmitted bits may be coordinated, as in the "vector" or "frequency-designed" codes.

The objective of this research is to attain the shaping gain of a high dimensionality signal set while maintaining relatively low computational complexity. The problem is that the description of an N-dimensional signal set can be very complex. Recently, Wei has used a method based on the "generalized cross constellation" construction. While this construction gives signal sets with the desired properties for voiceband-modem applications they are not the best possible in terms of the average energy per point. Nevertheless, to increase the shaping gain further, most approaches exhibit significant loss in peak-to-average ratio (*PAR*) and constellation expansion ratio (*CER*). For such cases we will consider the Shell Construction which achieves the same or better shaping gain at less *PAR* and *CER*, but still more than the generalized cross constellation.

The constraints of real time implementations of the Shell Construction and, more generally, of coded modulation systems is also studied. The complexity of an implementation is dominated by the Viterbi Algorithm. We propose ways to improve the throughput of a coded modulation system.

Performance limitations in synchronous digital systems. Friedman, Eby Gershon, Ph.D. *University of California, Irvine*, 1989. 204pp. Chair: James H. Mulligan, Jr.

Order Number DA8923070

Synchronous digital systems consist of functional blocks operating under the influence of a global clock signal. Fundamental performance limitations exist within these systems due to the necessary requirements of propagating data signals through logic and interconnect and synchronizing the data flow between functional blocks. These limitations depend upon the properties of the device and interconnect technologies as well as the design approach. The underlying principles necessary for the optimum design of high performance synchronous digital systems are based on these properties and have been applied to representative engineering problems.

The underlying design principles were developed by analyzing the signal transport properties of interconnect and device technologies, the transient response and latching characteristics of data registers, and the relations in time between data and clock signals. In the course of this research, these elements were investigated in detail and analytic equations were developed describing their behavior. These results were applied to the systems level problem of optimal data throughput in high speed pipelined data paths.

In order to determine the fundamental performance limitations of the complete synchronous digital system, the interdependent elements were analyzed as a single integrated system; specifically, how the clock distribution network, the registers, and the data path affect the performance of each other. This permitted the development of an integrated approach for designing and analyzing high performance synchronous systems and represents one of the fundamental results of this research effort.

Thus, this research describes: (1) The inherent limitations of technology and design methodology on maximum synchronous performance. (2) Guidelines for designing clock and data timing relationships to maximize synchronous performance. (3) An approach for designing high performance synchronous digital systems by applying the characteristics of the interconnect delay, clock distribution network, logic path, and register latching conditions to both determine and optimize the data throughput and clock frequency.

In summary, the research results presented in this dissertation provide quantitative insight into how the performance of a synchronous digital system is limited and how to design a system in order to maximize its data throughput and clock frequency.

Reactive effects in impedance imaging. Fuks, Luiz Felipe, Ph.D. *Rensselaer Polytechnic Institute*, 1989. 212pp. Adviser: Kenneth A. Connor **Order Number DA8926573**

Biological tissue has significant reactive components, or displacement currents at the frequencies utilized in impedance imaging. This