Dynamic and Short-Circuit Power of CMOS Gates Driving Lossless Transmission Lines

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Abstract

The dynamic and short-circuit power consumption of a CMOS gate driving an LC *transmission line as a limiting case of an* RLC *transmission line is investigated in this paper. Closed form solutions for the output voltage and short-circuit power of a CMOS gate driving an* LC *transmission line are presented. These solutions agree with AS/X circuit simulations within 11% error for a wide range of transistor widths and line impedances. The ratio of the short-circuit to dynamic power is shown to be less than 7% for CMOS gates driving* LC *transmission lines where the line is matched or underdriven. The total power consumption is expected to decrease as inductance effects becomes more significant as compared to an* RC *dominated interconnect.*

I. Introduction

Historically, interconnect has been modeled as a single lumped capacitance in the performance analysis of on-chip interconnects [1]-[6]. With the scaling of technology and increasing chip size, the crosssectional area of wires has scaled down while interconnect length has increased. The resistance of the interconnect has therefore become significant, requiring more accurate *RC* delay models [7]. Initially, the interconnect was modeled as a lumped *RC* circuit. To further improve accuracy, the interconnect is often modeled as a distributed *RC* circuit (as multiple T or Π sections) for those nets requiring increased accuracy [8], [9].

Currently, inductance is becoming more important with decreasing on-chip rise times and longer wire lengths [10]-[16]. Wide wires are frequently encountered in clock distribution networks and in data busses. These wires, often at the upper metal layers, are low resistance wires that can exhibit significant inductive effects [15], [16]. Furthermore performance requirements are accelerating the introduction of new materials such as low resistivity copper interconnect [17]. In the limiting case, high temperature superconductors may possibly become commercially available [18]. More accurate *RLC* transmission line models are therefore becoming necessary in the analysis of VLSI-based interconnect.

The *RC* model can be viewed as a limiting case of the *RLC* transmission line model where the inductance is considered to be negligible. This case has been thoroughly investigated and is well represented in the literature [19]-[24]. The other limiting case is an *LC* transmission line where the resistance is negligible. This case approximates the low loss lines encountered in Multi-Chip Modules (MCM) and Printed Circuit Boards (PCB). Although it is highly improbable that the resistance of on-chip interconnects will become negligible in the near term, an *LC* analysis provides an upper limit for analyzing inductance effects in VLSI circuits. The behavior of an *RLC* transmission line can therefore be bounded by analyzing the behavior of the *RC* and the *LC* cases.

The focus of this paper is the investigation of dynamic and short-circuit power in CMOS gates driving *LC* transmission lines. The dynamic and short-circuit power consumption of a CMOS gate driving an *LC* transmission line is presented in section II. The analysis in section II is performed for the case where the transition time of the signal at the input of the CMOS gate driving a transmission line is smaller than twice the time of flight of the waves propagating across the transmission line. The short-circuit to dynamic power ratio for a lossless transmission line load is examined in section III and compared to the same ratio when the load is a simple capacitor or an *RC* line. Finally, some conclusions are offered in section IV.

II. Dynamic and short-circuit power

The dynamic power consumption can be derived from analyzing the basic behavior of a transmission line interacting with a CMOS gate. This topic is discussed in subsection A. It is shown that the dynamic power consumption of a CMOS gate driving a transmission line is the same as the dynamic power

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consumption of a gate driving a capacitor equal to the total capacitance of the transmission line. In subsection B, the short-circuit power consumption of a CMOS gate driving a lossless transmission line is investigated for the regime where $t_r<2T_0$, where t_r is the rise time of the input signal of the CMOS gate and T_0 is the time of flight of the signals across the transmission line.

A. Dynamic power

A MOS transistor driving a lossless transmission line launches an initial voltage wave with a value $V_1=I_{sat}\ Z_0$ where I_{sat} is the saturation current of the CMOS gate and Z_0 is the characteristic impedance of the line. This initial voltage signal propagates towards the load and reaches the load at time T_0. Assuming the load is open or is a small capacitor, a voltage wave propagates back towards the transistor with a magnitude V_1 and a current wave $-I_{sat}$. This wave returns to the MOS transistor at time $2T_0$. At that moment the current of the two waves cancels and the voltage adds to $2V_1$. For this period of time (from 0 to $2T_0$), a current of V_1/Z_0 is drawn from the power supply. At $t=2T_0$, a new voltage wave is initiated with a value $V_2=I(V_{DD}-2V_1-V_2)Z_0$, where $I(V_{DD}-2V_1-V_2)$ is the current of the transistor with $V_{out}=2V_1+V_2$. The cycle is repeated and a current V_2/Z_0 is drawn from the supply for the period of time from $2T_0$ *to* $4T_0$. This cycle repeats until the voltage at the output of the transistor reaches V_{DD}. The last voltage wave is assumed to be V_n, where n is the number of traversals of the line required to reach steady state. The number of iterations can in general be infinite or only one in the perfectly matched case (where the geometric width of the driving transistors is adjusted so that the output impedance of the CMOS gate is equal to the characteristic impedance of the transmission line). The output current as a function of time of a PMOS transistor pulling up the output voltage is shown in Fig. 1.

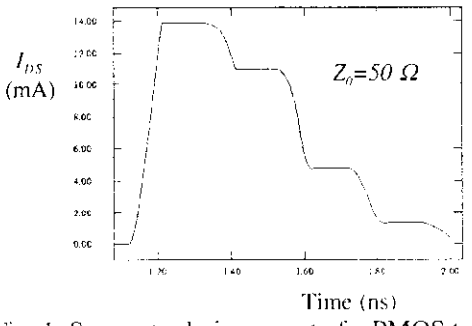

Fig. 1. Source to drain current of a PMOS transistor driving a lossless transmission line.

Summing these voltages, the following condition is satisfied,

$$V_1 + V_2 + \ldots + V_n = \frac{V_{DD}}{2}, \tag{1}$$

where the final voltage is V_{DD} once the transient response reaches the steady state value. From this analysis, the energy taken from the power supply for a low to high transition is given by

$$E_{dyn}/Cycle = V_{DD} \cdot \frac{2T_0}{Z_0} \cdot (V_1 + V_2 + \ldots + V_n). \tag{2}$$

Using (1) and noting that T_0/Z_0 is equal to C_t, the total capacitance of the line, (2) evaluates to

$$E_{dyn}/Cycle = C_t \cdot V_{DD}^2. \tag{3}$$

This energy is stored in the capacitance of the line and is passed to the ground in the following high to low transition as the line is discharged. Thus, (3) represents the energy per cycle of the output of the CMOS gate. The dynamic power is therefore

$$P_{dyn} = C_t \cdot V_{DD}^2 f, \tag{4}$$

where f is the frequency of the signal at the output of the CMOS gate. This formula is the same as the dynamic power for a capacitor which equals the total capacitance of the line.

B. Short-circuit power

The other component of switching transient power in CMOS circuits is the short-circuit power that occurs when both the NMOS and the PMOS transistors conduct current at the same time. This power is consumed during the rise (fall) time of the input signal when the input signal is between $V_{DD}+V_{Tp}$ and V_{Tn} (where V_{Tn} is the threshold voltage of the N-channel device and V_{Tp} is the threshold voltage of the P-channel device and is negative for an enhancement mode device). The case considered here is when the rise time is less than twice the propagation delay across the line ($t_r<2T_0$). In this case, the reflections do not affect the short-circuit power because the signal returns to the driver after the input signal has reached its final value. Under this condition, the transmission line appears as a resistance with a value Z_0. The equivalent circuit of a CMOS inverter driving a lossless transmission line for the period of time 0 to $2T_0$ is shown in Fig. 2, where C_0 is the intrinsic drain capacitance of the CMOS inverter. The differential equation describing the KCL for the output node is

$$(I_n - I_p) = C_0 \cdot \frac{d(V_{DD} - V_{out})}{dt} + \frac{(V_{DD} - V_{out})}{Z_0}. \tag{5}$$

where I_n and I_p are the currents of the NMOS transistor and the PMOS transistor, respectively. Note that the resistance Z_0 representing the transmission line is connected between V_{DD} and V_{out} because the line is assumed to be charged to V_{DD} and that $d(V_{DD}-V_{out})/dt=-d(V_{out})/dt$. The NMOS transistor is assumed to be in the saturation region during the rise time of the input

signal. This assumption is even more accurate in deep submicrometer technologies because of the early saturation phenomenon [25]. On the other hand, the PMOS transistor starts in the linear region and then enters the saturation region. Note that the short-circuit current is the current through the PMOS transistor during a rising input. The signal at the input of the CMOS driver is

$$V_{in} = kt = \frac{V_{DD}}{t_r} t, \tag{6}$$

before the input reaches V_{DD} (*i.e.*, $t < V_{DD}/k$).

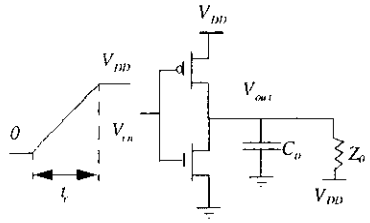

Fig. 2. Equivalent circuit of a CMOS driver driving a lossless transmission line for $0<t<2T_0$.

Based on the alpha power law, when the PMOS transistor is in saturation the short-circuit current is

$$I_{SC} = P_{Cp} \cdot \frac{W_p}{L_p} \cdot (V_{DD} - kt - |V_{Tp}|)^{\alpha p}. \tag{7}$$

where P_C is a constant that characterizes the drive current of the transistor in saturation, W and L are the geometric width and length, respectively, of the transistor, and α is a constant between one (strong velocity saturation) and two (weak velocity saturation) [25]. p indicates the PMOS transistor and n indicates the NMOS transistor. When the PMOS transistor operates in the linear region, the solution of (5) appears intractable because V_{DS} is a function of V_{out}. Therefore, the current from the output capacitor C_0 is assumed to be small compared to the current from the transmission line. This assumption is accurate in deep submicrometer technologies, because the transistors have small parasitic capacitances and high current levels. The magnitude of the drive current is relevant because smaller transistors are needed to match the transmission line, implying a smaller C_0. Also Z_0 is typically in the range of 30 to 60 ohms, which results in large currents compared to the parasitic capacitance C_0. Under this assumption and using the alpha power law model, the output voltage is

$$V_{out} = V_{DD} - \frac{Z_0 \cdot P_{Cn} \cdot \frac{W_n}{L_n} \cdot (kt - V_{tn})^{\alpha n}}{1 + \frac{P_{Cp}}{P_{Cn}} \cdot \frac{W_p}{L_p} \cdot \left(V_{DD} - kt - |V_{Tp}|\right)^{\frac{\alpha p}{2}} \cdot Z_0}, \tag{8}$$

for the time $0 < t < t_r$ where $t_r < 2T_0$. Noting that V_{DD}-V_{out} is V_{SD} of the PMOS transistor, the short-circuit current of a CMOS inverter driving an LC transmission line is

$$I_{SC} = \frac{Z_0 \cdot P_{Cn} \cdot \frac{W_n}{L_n} \cdot (kt - V_{Tn})^{\alpha n}}{\frac{P_{Cp}}{P_{Cn}} \cdot \frac{L_p}{W_p} \cdot \left(V_{DD} - kt - |V_{Tp}|\right)^{\frac{\alpha p}{2}} + Z_0}. \tag{9}$$

A CMOS gate driving a transmission line can be most efficiently characterized by the matching factor λ, where

$$\lambda = \frac{2 S_p W_p Z_0}{V_{DD}}. \tag{10}$$

When $\lambda = 1$, the transistor is optimally matched to the transmission line. If λ is less than one, the transmission line is underdriven and the response suffers from a slow output rise time. If λ is greater than one, the transmission line is overdriven and the response suffers from overshoots and undershoots that can cause reliability problems. If the overshoots and undershoots are large enough, logical errors can occur. Voltages higher than the supply voltage and lower than ground create large electric fields that can deteriorate the oxide and create hot electron effects. Also, out of rail voltages can forward bias the junctions between the drain and source and the substrate, the n-well, or the p-well. When these junctions are forward biased, current flows directly into the wells or the substrate. This behavior is undesirable because it wastes current, dissipating extra power, and can induce other reliability problems within the substrate. Thus, the range defined by $0.3 < \lambda < 1.6$ is arbitrarily chosen to represent the range of interest characterizing practical matching conditions. The analytical solutions of (7) and (9) are compared to AS/X [26] simulations in Fig. 3 assuming $t_r = 100$ *ps* and using λ as a parameter. The analytical solution shows good agreement with the circuit simulations for a wide range of λ.

The short-circuit energy per transition can be calculated from

$$E_{SC}/Transition = Area_{SC} \cdot V_{DD}, \tag{11}$$

where $Area_{SC}$ (in coulombs) is the area under the short-circuit current curve. This area can be approximated by a triangle [21] whose base is given by $(V_{DD}$-$V_{Tn}+V_{Tp})t_r/V_{DD}$ and height is given by I_{peak} (the maximum point on the short-circuit current curve). Thus, the short-circuit energy per transition is

$$E_{SC}/Transition = \frac{I_{peak}}{2}(V_{DD} - V_{tn} - |V_{tp}|)t_r K_c, \tag{12}$$

where K_c is a correction factor. Note in Fig. 3 that the analytical solution deviates from the simulated results in a consistent way at the point of intersection of the saturated curve and the linear curve. This deviation is due to the non-monotonic nature of the alpha power law model used to characterize the devices.

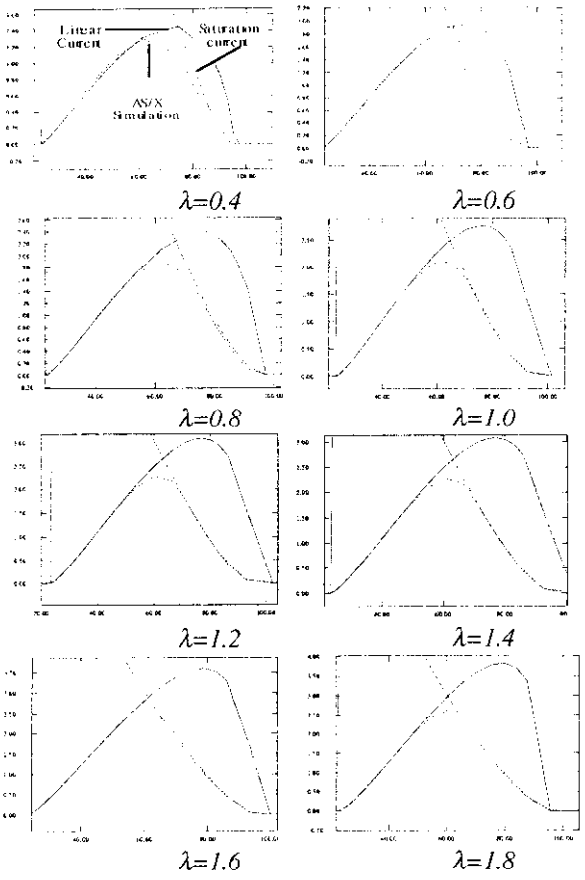

Fig. 3. Analytical solution for short-circuit current I_{SC} (mA) in (7) and (9) compared to AS/X simulations [26] for λ=0.4, 0.6, 1.0, 1.2, 1.4, 1.6, and 1.8.

Due to this consistent error at the saturation/linear region breakpoint, a constant correction factor K_c is used and calibrated at $\lambda=1$. I_{peak} can be calculated by equating (7) and (9). Alternatively, I_{peak} can be calculated as

$$I_{peak} = K(\lambda)W_p, \tag{13}$$

where $K(\lambda)$ is determined from varying λ and calculating I_{peak}/W_p. $K(\lambda)$ is plotted in Fig. 4.

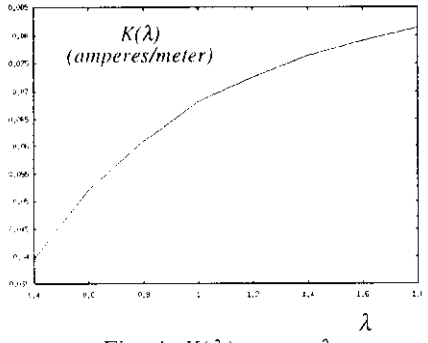

Fig. 4. $K(\lambda)$ verses λ.

$K(\lambda)$ quantifies in I_{peak} the effect of the output waveform shape on the short-circuit current. Note that $K(\lambda)$ saturates to an asymptotic value. This behavior can be explained by observing how the shape of the output signal varies with λ in Fig. 5. Note that the shape of the output voltage waveform depends heavily on λ for small λ and this dependence saturates as λ increases. The short-circuit current depends upon the output voltage because the drain to source voltage across the PMOS transistor is dependent on V_{out}. The gate to source voltage of the PMOS transistor depends only on the input signal of the transistor (since the source is connected to the power supply). Thus, the biasing of the PMOS transistor depends only on λ. The current of the PMOS transistor depends on the bias voltage and the geometric width. The AS/X circuit simulator is used to quantify the accuracy of these analytic equations, such as the comparison of (12) with AS/X [26] in Table 1. The analytical solution shows good agreement (less than 1% error for $\lambda > 1$) with the circuit simulations for a wide range of λ and exhibits a maximum error of 11% for small λ.

Table 1: AS/X simulations compared to analytical solution for E_{SC}/transition (in joules).

λ	AS/X Simulation x10^{-15}	Analytical x10^{-15}	% Error
0.4	131.20	116.00	11.00
0.6	161.45	152.50	5.50
0.8	182.77	178.95	2.09
1.0	199.60	199.60	0.00
1.2	212.55	212.30	0.12
1.4	224.55	223.20	0.60
1.6	231.93	231.37	0.24
1.8	239.68	238.20	0.62

III. Short-circuit to dynamic power ratio

Assuming a symmetric CMOS gate, the short-circuit power is

$$P_{SC} = I_{peak}(V_{DD} - V_{Tn} - |V_{Tp}|)t_r f. \tag{14}$$

As described previously, the dynamic power is

$$P_{dyn} = \frac{T_0}{Z_0} \cdot V_{DD}^2 f. \tag{15}$$

Dividing (14) by (15), the magnitude of the dynamic power can be compared to the magnitude of the short-circuit power. The resulting ratio is

$$\frac{P_{SC}}{P_{dyn}} = K(\lambda)\lambda \cdot \frac{(V_{DD} - V_{Tn} - |V_{Tp}|)}{V_{DD}} \frac{t_r}{T_0} \cdot \frac{K_c}{2S_p}. \tag{16}$$

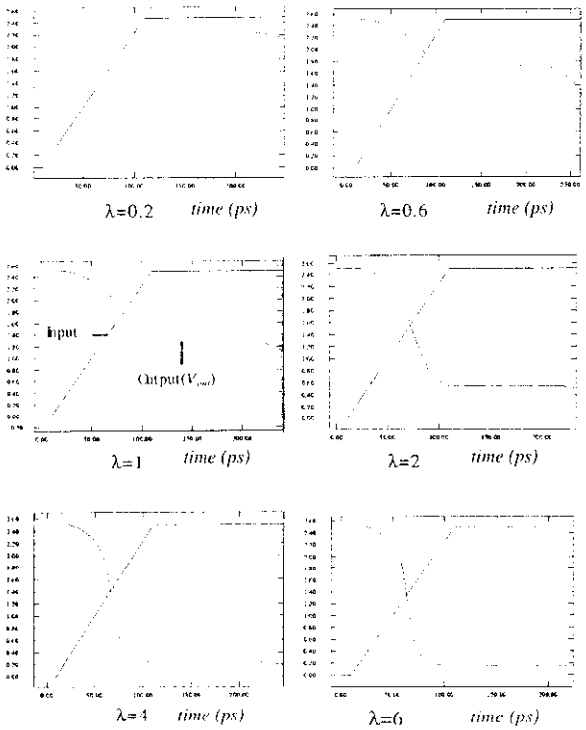

Fig. 5. Dependence of the output voltage on λ for λ = 0.2, 0.6, 1.0, 2.0, 4.0, and 6.0.

The ratio between the short circuit power and the dynamic power depends upon the matching condition λ of the transmission line impedance to the output impedance of the CMOS gate and the ratio between the rise time of the input signal to the time of flight of the waves across the transmission line (t_r/T_0). The dependence on the supply voltage is fairly weak. The dependence exists only if the supply voltage and the threshold voltages scale differently. The dependence of the short-circuit to dynamic power ratio on λ is shown in Fig. 6. As the matching condition moves from underdriven to matched to overdriven, the short-circuit to dynamic power ratio increases. This ratio is less than 7% for the matched (λ=1) and underdriven cases (λ<1). This low ratio is due to the small voltage step in the output voltage while the input signal is still changing, as can be seen from Fig. 5. In the matched case, the input signal transitions approximately twice as fast as the output signal since the input signal transitions from *0* to V_{DD} at the same time as the output signal transitions from *0* to $V_{DD}/2$. This characteristic explains the low short-circuit to dynamic power ratio in a matched or underdriven circuit. Therefore, it is preferable to not overdrive the line (*i.e.*, make $\lambda > 1$) in order to decrease the short-circuit power. The classical design criteria for driving a capacitive load is to maintain equal input and output transition times which gives rise to a short-circuit power of approximately *20%* of the dynamic power [3]. For *RC* loads, the P_{SC}/P_{Dyn} ratio is even greater because the voltage drop across the load resistance makes the source to drain voltage large once the transistor begins to switch.

As the rise time of the input signal t_r increases, the short-circuit power increases, since there is more time for the short-circuit current to flow. The rise time t_r does not affect the dynamic power and thus increasing t_r increases the ratio of the short-circuit power to the dynamic power. Dynamic power increases with increasing T_0 because the total capacitance of the line is T_0/Z_0. Thus, as T_0 increases, the capacitance of the line increases linearly which increases the dynamic power linearly. The short-circuit power is not affected by T_0 as long as T_0 is greater than half the input rise time, making the ratio of the short-circuit power to the dynamic power decrease as T_0 is increased.

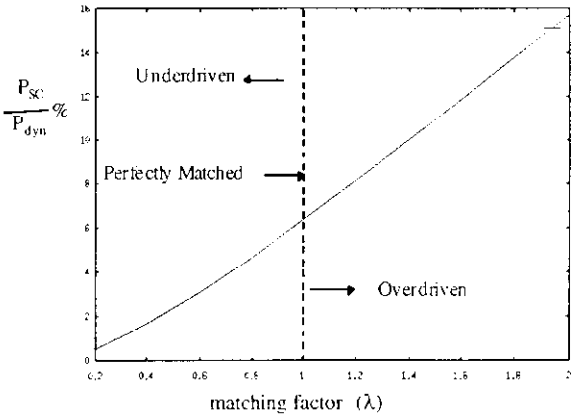

Fig. 6. Dependence of the short circuit to dynamic power ratio on λ.

IV. Conclusions

The dynamic and short-circuit power consumed by a CMOS gate driving a lossless transmission line is investigated. It is shown that the dynamic power of a CMOS gate driving a lossless transmission line is the same as that of a CMOS gate driving a capacitor equal to the total capacitance of the line. A closed form solution for the short-circuit power is presented that agrees with circuit simulations within 11% error for a wide range of the matching factor λ. An expression for the short-circuit to dynamic power ratio is presented that shows that the short-circuit power is below 7% of the dynamic power for λ less than or equal to one. The short-circuit power for the case of *LC* loads is much less than that of the case of *RC* loads. In the case of *RLC* loads, the short-circuit power is in the middle, greater than the case of *LC* loads but less than the case of *RC* loads.

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