Noise Estimation Due To Signal Activity For Capacitively Coupled CMOS Logic Gates

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Abstract

The effect of interconnect coupling capacitance on neighboring CMOS logic gates driving coupled interconnections strongly depends upon the signal activity. A transient analysis of two capacitively coupled CMOS logic gates is presented in this paper for different combinations of signal activity. The uncertainty of the effective load capacitance and propagation delay due to the signal activity is addressed. Analytical expressions characterizing the output voltage and propagation delay are also presented for different signal activity conditions. The propagation delay based on these analytical expressions is within 3% as compared to SPICE, while the estimated delay neglecting the difference between the load capacitances can exceed 45%. The logic gates should be properly sized to balance the load capacitances in order to minimize any uncertainty in the signal delay. The peak noise voltage on a quiet interconnection determined from the analytical expressions is within 4% of SPICE.

1 Introduction

On-chip coupling noise in VLSI circuits, until recently considered a second order effect, has become an important issue in deep submicrometer VLSI circuits [1], [2]. With decreasing feature sizes and the average length of on-chip interconnections increasing, the interconnect capacitance has become comparable to or larger than the gate capacitance [3].

Interconnections in VLSI circuit are conductors on dielectric insulation layers. The mutual electric field flux between neighboring interconnect lines results in a coupling capacitance [4]. The coupling (or fringing) capacitance increases if the spacing between the interconnect lines is reduced and/or the aspect ratio of the interconnect thickness-to-width increases. The coupling capacitance may become comparable to the line-to-ground interconnect capacitance. Therefore, coupling has emerged as one of the primary issues in evaluating the signal integrity of VLSI circuits [5], [6].

The importance of interconnect coupling capacitances depends upon the behavior of the CMOS logic gates. If the logic gates driving the coupled interconnections are in transition, the coupling capacitance can affect the propagation delay and the waveform shape of the output voltage signal. If one of these logic gates is in transition and the other logic gate is quiet, the coupling capacitance can not only change the propagation delay of the active logic gate, but can also induce a voltage change on the quiet line. The voltage change may cause extra current to flow through the CMOS logic gate driving the quiet interconnect line, resulting in additional power dissipation. Furthermore, a change in voltage may cause overshoots (the signal rises above the voltage supply) or undershoots (the signal falls below ground). The overshoots and undershoots may cause carrier injection or collection within the substrate [7]. If the voltage change is greater than the threshold voltage of the following logic gates, circuit malfunctions and excess power dissipation may occur.

In order to reduce both design cost and time, coupling effects should be estimated at the system level. The coupling noise voltage on a quiet interconnect line has been analyzed by Shoji using a simple linear RC circuit in [1]. The effects of the coupling capacitance have also been addressed by Sakurai using a resistive-capacitive interconnect model in [8], in which the CMOS logic gates are approximated by the effective output resistance and similar interconnect lines are assumed. An estimate of the peak coupling noise voltage based on a coupled transmission line model has been presented by the authors in [9]. The nonlinear behavior of the MOS transistors is neglected in these analyses [1], [8], [9]. The maximum effective load capacitance, *i.e.*, the intrinsic load capacitance plus two times the coupling capacitance ($C + 2C_c$), is typically used to estimate the worst case propagation delay of an active logic gate [1], [8].

In this paper, a transient analysis of two capacitively coupled logic gates is presented based on the signal activity. The interconnect-to-ground capacitance (or self capacitance) and the gate capacitance of the following logic stage are included in the intrinsic load capacitance (C_1 or C_2). An analysis of the in-phase transition, in which two coupled logic gates transition in the same direction, demonstrates that the effective load capacitances may deviate from the intrinsic load capacitances if the logic gates and intrinsic load capacitances are different. The same conclusion can also be observed for an out-of-phase transition, where the transition changes in the opposite direction, making the effective load capacitances deviate from $C_1 + 2C_c$ or $C_2 + 2C_c$.

If one logic gate is active and the other is quiet, the coupling capacitance may cause the effective load capacitance of the active logic gate to be less than $C_1 + C_c$ or $C_2 + C_c$ when the active logic gate transitions from high-to-low and the quiet state is at logic low (ground). However, if the quiet state is high (V_{dd}), the effective load capacitance of the active logic gate can exceed $C_1 + C_c$ or $C_2 + C_c$. If the active logic gate transitions from high-to-low and the quiet state is at logic low, the coupling noise voltage causes the quiet state to drop below ground (undershoots). Overshoots occur when the inverter transitions from low-to-high and the quiet state is at a logic high (V_{dd}). Overshoots or undershoots may cause current to flow through the substrate, possibly corrupting data in dynamic logic circuits [7]. This issue is also of significant concern in the logic elements within a bistable latch structure [10].

Analytical expressions characterizing the output voltages for each condition are presented here based on an assumption of a fast ramp input signal. Delay estimates based on the analytical expressions are within 3% as compared to SPICE, while the estimate based on C_1 (or C_2), $C_1 + 2C_c$ (or $C_2 + 2C_c$), and $C_1 + C_c$ (or $C_2 + C_c$) for in-phase, out-of-phase, and one active transition can reach 48%, 16%, and 12%, respectively, if the signal activity is not considered. The peak noise voltage based on the analytical prediction is within 4% of SPICE.

The dependence of the coupling capacitance on the signal activity is discussed in Section 2. Analytical expressions characterizing the effective load capacitance, output voltage, and propagation delay during an in-phase and out-of-phase transition are addressed in Sections 3 and 4, respectively, as well as a comparison between the analytical estimates and SPICE. An analytical expression characterizing the coupling noise voltage of a quiet logic gate is presented for both step and ramp input signals. The accuracy of these analytical expressions are compared to SPICE in Section 5. Strategies to re-

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duce the effects of coupling capacitance are discussed in Section 6, followed by some concluding remarks in Section 7.

2 Signal Activity

In VLSI circuits, interconnect lines are typically driven by CMOS logic gates. The logic gates driving these interconnect lines are capacitively coupled. A circuit diagram of two capacitively coupled CMOS inverters is shown in Fig. 1(a).

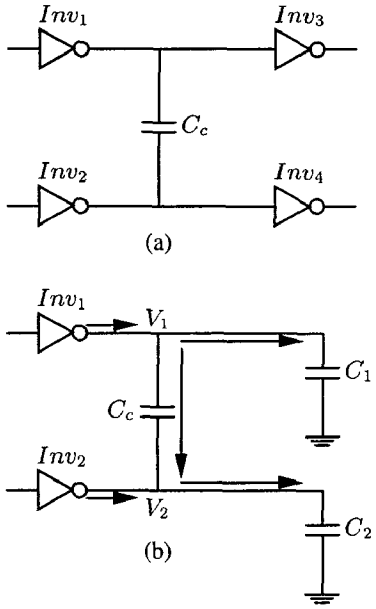

Figure 1: Circuit model of two capacitively coupled inverters. (a) A circuit diagram of two capacitively coupled CMOS inverters. (b) An equivalent circuit of the two coupled CMOS inverters.

In order to simplify this analysis, the interconnection is modeled as a capacitive load where C_1 includes both the interconnect capacitance of line 1 and the gate capacitance of Inv_3. C_2 includes both the interconnect capacitance of line 2 and the gate capacitance of Inv_4. The equivalent circuit and the current directions are shown in Fig 1(b). The output voltages of Inv_1 and Inv_2 are V_1 and V_2, respectively. The differential equations characterizing the behavior of this capacitively coupled system are

$$I_{DS1} = (C_1 + C_c)\frac{dV_1}{dt} - C_c\frac{dV_2}{dt}, \quad (1)$$

$$I_{DS2} = (C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt}. \quad (2)$$

The effects of the coupling capacitance on the transient response of these two coupled inverters also depend on the behavior of each inverter, *i.e.*, the signal activity. There are three possible conditions for each inverter, a high-to-low transition, a low-to-high transition, and a quiet state in which the output voltage of the inverter remains at either the voltage supply (V_{dd}) or ground. Both the high-to-low and low-to-high transitions are included in the dynamic transition. If the signals at the input of each inverter are purely random and uncorrelated, there are nine different combinations which can occur for a system composed of two capacitively coupled inverters. These combinations are listed in Table 1.

Assuming equal probability for each condition, the probability of an in-phase transition, in which both inverters have the same dynamic transitions, is 2/9. The probability of an out-of-phase transition, in which these two inverter have different dynamic transitions, is also 2/9. The probability of no dynamic transition is 1/9. The condition in which one inverter is quiet and the other is in transition has the highest probability, 4/9.

Table 1: Combinations of the signal activity for a system of two capacitively coupled inverters

V_{in1}	Inv_1	V_{in2}	Inv_2
0 to V_{dd}	High-to-low	0 to V_{dd}	high-to-low
		V_{dd} to 0	low-to-high
		V_{dd} or 0	quiet
V_{dd} to 0	Low-to-high	0 to V_{dd}	high-to-low
		V_{dd} to 0	low-to-high
		0 or V_{dd}	quiet
V_{dd} or 0	Quiet	0 to V_{dd}	high-to-low
		V_{dd} to 0	low-to-high
		0 or V_{dd}	quiet

In the following analysis, if both inverters are in transition, it is assumed that these inverters are triggered at the same time with the same input slew rate. During a logic transition, only the active transistors are considered in the development of the analytical expressions. The MOS transistors are characterized by the nth power law model in the saturation region and the effective output resistance in the linear region [11].

3 In-Phase Transition

The in-phase transition is an optimistic condition in terms of the effect of the coupling capacitance on the propagation delay of a CMOS inverter. With an in-phase transition, both inverters are assumed to transition in the same direction, for example, high-to-low at the output. The PMOS transistors are neglected based on an assumption of a fast ramp input signal [12].

$NMOS_1$ and $NMOS_2$ are the active transistors in each inverter for this transition and may have different geometric sizes. The shape of the input signals driving both inverters is characterized by a ramp waveform,

$$V_{in1} = V_{in2} = \frac{t}{\tau_r}V_{dd} \qquad 0 \le t \le \tau_r. \quad (3)$$

3.1 Waveform of the Output Voltage

An assumption of a fast ramp input signal supports the assumption that both inverters operate in the saturation region during a complete input transition. When the input voltage exceeds the threshold voltage V_{TN}, *i.e.*, $t \ge \tau_n = \frac{V_{TN}}{V_{dd}}\tau_r$, both of the NMOS transistors are ON and begin operating in the saturation region.

After the input transition is completed, the input voltage is fixed at V_{dd} and both of the NMOS transistors remain in the saturation region. The times at which $NMOS_1$ and $NMOS_2$ leave the saturation region are τ_{nsat1} and τ_{nsat2}, respectively. For the condition where these NMOS transistors are not equally sized, $NMOS_1$ and $NMOS_2$ may leave the saturation region at different times. If $NMOS_1$ leaves the saturation region first after a time τ_{nsat1}, $NMOS_1$ operates in the linear region and the drain-to-source current can be approximated by $\gamma_{n1}V_{DS}$, where γ_{n1} is the effective output conductance.

After τ_{nsat2}, both of these transistors operate in the linear region. Both of the NMOS transistors are modeled by the effective output conductances, γ_{n1} and γ_{n2}. A general solution of the output voltages is obtained by solving the linear differential equations, (1) and (2), with the initial conditions of V_1 and V_2.

Both β_1 and β_2 described by (6) and (7), respectively, include the effects of the coupling capacitance C_c and the intrinsic load capacitances, C_1 and C_2. If the ratio of B_{n1}/B_{n2} is the same as that of C_1/C_2, *i.e.*, these MOS transistors have the same ratio of

Table 2: Analytical expressions characterizing the output voltage for an in-phase transition

Operating region	Output voltage $V_1(t)$ and $V_2(t)$
$[\tau_n, \tau_r]$	$V_1 = V_{dd} - \beta_1 \frac{\tau_r}{(n_n+1)V_{dd}} (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n+1}$ (4) $V_2 = V_{dd} - \beta_2 \frac{\tau_r}{(n_n+1)V_{dd}} (\frac{t}{\tau_r} V_{dd} - V_{TN})^{n_n+1}$ (5) $\beta_1 = \frac{C_c B_{n2} + (C_2 + C_c) B_{n1}}{C_1 C_2 + C_c(C_1 + C_2)}$ (6) $\beta_2 = \frac{C_c B_{n1} + (C_1 + C_c) B_{n2}}{C_1 C_2 + C_c(C_1 + C_2)}$ (7)
$[\tau_r, \tau_{sat}^{min}]$	$V_1 = V_{dd} - \beta_1 (V_{dd} - V_{TN})^{n_n} (t - \frac{n_n V_{dd} + V_{TN}}{(n_n+1)V_{dd}} \tau_r)$ (8) $V_2 = V_{dd} - \beta_2 (V_{dd} - V_{TN})^{n_n} (t - \frac{n_n V_{dd} + V_{TN}}{(n_n+1)V_{dd}} \tau_r)$ (9) $\tau_{sat}^{min} = \min(\tau_{nsat1}, \tau_{nsat2})$ (10) $\tau_{sat}^{max} = \max(\tau_{nsat1}, \tau_{nsat2})$ (11)

output current drive to the corresponding intrinsic load capacitance, the coupling capacitance has no effect on the waveform of V_1 and V_2 (note that C_c is eliminated from the expressions for β_1 and β_2). In practical CMOS VLSI circuits, this condition cannot be satisfied due to the size difference among the MOS transistors, interconnect geometric parameters, and gate capacitances of the following logic stages. Therefore, the coupling capacitance affects the waveform shape of the output voltages, V_1 and V_2. It is therefore necessary to consider the interconnect capacitance when determining the proper size of the MOS transistors.

Assuming B_{n1} is equal to B_{n2}, *i.e.*, both NMOS transistors have the same geometric sizes (or, more precisely, output gain), the effective load capacitance of each inverter is

$$C_{n1_{\text{eff}}} = \frac{C_1 C_2 + C_c(C_1 + C_2)}{C_2 + 2C_c}, \tag{12}$$

$$C_{n2_{\text{eff}}} = \frac{C_1 C_2 + C_c(C_1 + C_2)}{C_1 + 2C_c}. \tag{13}$$

The solid lines shown in Fig. 2 depict the ratio of $C_{n1_{\text{eff}}}$ to C_1 and the dotted lines represent the ratio of $C_{n2_{\text{eff}}}$ to C_2. The horizontal axis represents the ratio of C_2 to C_1, which characterizes the difference between the intrinsic load capacitances. Ratios of the coupling capacitance, C_c to C_1, of 0.3, 0.5, and 0.7 are considered. Note that the deviation of the effective load capacitances from the intrinsic capacitances (C_1 and C_2) increases if the difference between the intrinsic load capacitances increases. The deviation also increases with increasing coupling capacitance for the same ratio of C_2/C_1.

Note in Fig. 2 that the effective load capacitance of one inverter increases above the corresponding intrinsic load capacitance while the effective load capacitance of the second inverter drops below the corresponding intrinsic load capacitance. The deviation of the effective load capacitances from the intrinsic load capacitances results in different propagation delays.

3.2 Propagation Delay Time

A comparison of the propagation delay based on these analytical expressions with SPICE is listed in Table 3. The delay is estimated based on the intrinsic load capacitances, C_1 and C_2, for the no coupling condition. Note that the error of the delay based on the intrinsic load capacitance can exceed 40% while the delay based on the analytical equations is within 1% as compared to SPICE.

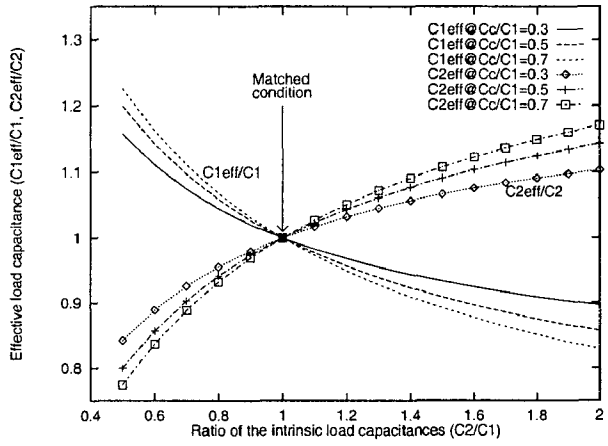

Figure 2: The ratio of the effective load capacitances, $C_{n1_{\text{eff}}}$ and $C_{n2_{\text{eff}}}$ to C_1 and C_2, respectively, for an in-phase transition assuming $B_{n1} = B_{n2}$.

4 Out-of-Phase Transition

The out-of-phase transition has the same probability as the in-phase transition. The out-of-phase transition is a pessimistic condition in terms of the effect of the coupling capacitance on the propagation delay of a CMOS inverter. It is assumed that Inv_1 transitions from high-to-low while Inv_2 transitions from low-to-high. NMOS_1 and PMOS_2 are the active transistors in each inverter. The initial states of V_1 and V_2 are V_{dd} and ground, respectively.

4.1 Waveform of the Output Voltage

In order to develop analytical expressions characterizing the output voltage, it is assumed that the absolute value of the threshold voltages of the NMOS and PMOS transistors are approximately equal. In the following analysis, all of the parameters describing the PMOS voltages are absolute values. When t is greater than τ_n, both NMOS_1 and PMOS_2 are ON and operate within the saturation region. Note in (14) and (15) that the coupling component $V_{p,1}$ in (14) causes V_1 to decrease slowly while the coupling component $V_{n,1}$ in (15) causes V_2 to increase slowly. The solutions of the out-

Table 3: Comparison of the in-phase transition with SPICE

	Size of Inv		Load Capacitance			SPICE		No Coupling				Analytic			
τ_r (ns)	W_{n1} (μm)	W_{n2} (μm)	C_1 (pF)	C_2 (pF)	C_c (pF)	τ_1 (ns)	τ_2 (ns)	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %
1.0	1.8	1.8	1.0	1.0	0.4	1.60	1.60	1.60	1.60	< 1.0	< 1.0	1.60	1.60	<1.0	< 1.0
1.0	1.8	1.8	0.8	1.0	0.3	1.29	1.25	1.30	0.65	< 1.0	48.0	1.29	1.24	<1.0	< 1.0
0.8	1.8	2.4	1.2	0.8	0.4	1.53	1.45	1.57	1.02	2.6	29.7	1.54	1.45	<1.0	< 1.0
1.0	2.4	1.8	1.2	0.8	0.4	1.43	1.35	1.45	0.78	1.7	42.0	1.42	1.34	<1.0	< 1.0
1.0	1.8	3.6	0.5	1.5	0.5	1.29	1.25	1.30	0.65	< 1.0	48.2	1.28	1.24	<1.0	< 1.0
1.0	1.8	3.6	1.0	1.0	0.8	1.27	1.00	1.60	0.62	25.6	38.2	1.28	1.00	<1.0	< 1.0

Table 4: Analytical expressions characterizing the output voltages for an out-of-phase transition

Operating region	Output voltage $V_1(t)$ and $V_2(t)$
$[\tau_n(\tau_p), \tau_r]$	$V_1 = V_{dd} - \frac{(C_2+C_c)V_{n,1} - C_cV_{p,1}}{C_1C_2 + C_c(C_1+C_2)}$ (14) $V_2 = \frac{(C_1+C_c)V_{p,1} - C_cV_{n,1}}{C_1C_2 + C_c(C_1+C_2)}$ (15) $V_{n,1} = B_{n1}\frac{\tau_r}{(n_n+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}$ (16) $V_{p,1} = B_{p2}\frac{\tau_r}{(n_p+1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p+1}$ (17)
$[\tau_r, \tau_{sat}^{min}]$	$V_1 = V_{dd} - \frac{(C_2+C_c)V_{n,2} - C_cV_{p,2}}{C_1C_2 + C_c(C_1+C_2)}$ (18) $V_2 = \frac{(C_1+C_c)V_{p,2} - C_cV_{n,2}}{C_1C_2 + C_c(C_1+C_2)}$ (19) $V_{n,2} = B_{n1}(V_{dd} - V_{TN})^{n_n}(t - \frac{n_nV_{dd}+V_{TN}}{(n_n+1)V_{dd}}\tau_r)$ (20) $V_{p,2} = B_{p2}(V_{dd} - V_{TP})^{n_p}(t - \frac{n_pV_{dd}+V_{TP}}{(n_p+1)V_{dd}}\tau_r)$ (21) $\tau_{sat}^{min} = \min(\tau_{nsat1}, \tau_{psat2})$ (22) $\tau_{sat}^{max} = \max(\tau_{nsat1}, \tau_{sat2})$ (23)

put voltages, V_1 and V_2, are listed in Table 4. These solutions are appropriate until one of the two transistors begins to operate in the linear region.

Assuming $V_{n,1}$ is equal to $V_{p,1}$, the effective load capacitances of $NMOS_1$ and $PMOS_2$ are

$$C_{n1_{\text{eff}}} = \frac{C_1C_2 + C_c(C_1+C_2)}{C_2}, \quad (24)$$

$$C_{p2_{\text{eff}}} = \frac{C_1C_2 + C_c(C_1+C_2)}{C_1}. \quad (25)$$

If C_1 is identical to C_2, $C_{n1_{\text{eff}}}$ and $C_{p2_{\text{eff}}}$ are equal to $C_1 + 2C_c$ or C_2+2C_c. The solid lines shown in Fig. 3 describe the ratio of $C_{n1_{\text{eff}}}$ to $C_1 + 2C_c$, and the dotted lines depict the ratio of $C_{n2_{\text{eff}}}$ to $C_2 + 2C_c$. The horizontal axis in Fig. 3 represents the ratio of C_2 to C_1, and ratios of C_c to C_1 of 0.3, 0.5, and 0.7 are considered for each condition. Note that the effective load capacitance of Inv_1 (Inv_2) may not be equal to $C_1 + 2C_c$ ($C_2 + 2C_c$) due to the difference between the load capacitances.

It is assumed in this discussion that the situation, $[(C_2 + C_c)V_{n,11} - C_cV_{p,1}] < 0$ or $[(C_1 + C_c)V_{p,1} - C_cV_{n,1}] < 0$, does not occur. This situation can occur if one transistor has a much higher output drive current than another, *i.e.*, $V_{n,1} \gg V_{p,1}$ or $V_{n,1} \ll V_{p,1}$, while C_c is comparable to C_1 or C_2. Under this condition, V_1 and V_2 may be greater than V_{dd} or less than ground, permitting overshoots or undershoots to occur.

When the input signal reaches V_{dd} at τ_r, both $NMOS_1$ and $PMOS_2$ continue to operate in the saturation region. For a non-ideal condition in which $NMOS_1$ and $PMOS_2$ are not sized equally, $NMOS_1$ and $PMOS_2$ may leave the saturation region at different times. The analysis after $\min(\tau_{nsat1}, \tau_{psat2})$ is the same as that of the in-phase transition.

4.2 Propagation Delay Time

A comparison of these analytical expressions with SPICE simulations is listed in Table 5. The delay is estimated based on the intrinsic load capacitance plus two times the coupling capacitance, *i.e.*, $C_1 + 2C_c$ and $C_2 + 2C_c$, respectively, for the no coupling condition. Note that the error of the delay based on $C_1 + 2C_c$ and $C_2 + 2C_c$ can reach 16% while the delay based on the analytical equation listed in Table 4 is within 3% as compared to SPICE.

5 One Inverter is Active and the Other is Quiet

The condition where one inverter is active and the other is quiet has the highest probability of occurrence. If one inverter is active and the other is quiet, the active transition can induce a voltage change on the quiet interconnect line through the coupling capacitance. The coupling noise voltage may therefore seriously affect

Table 5: Comparison of the out-of-phase transition with SPICE

	Size of Inv		Load Capacitance			SPICE		No Coupling				Analytic			
τ_r (ns)	W_{n1} (μm)	W_{n2} (μm)	C_1 (pF)	C_2 (pF)	C_c (pF)	τ_1 (ns)	τ_2 (ns)	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %
1.0	1.8	1.8	1.0	1.0	0.4	2.80	2.62	2.77	2.52	1.1	3.8	2.80	2.64	< 1.0	< 1.0
1.0	1.8	2.4	0.8	1.0	0.3	3.04	1.87	2.75	1.80	9.5	3.7	2.96	1.92	2.6	2.6
1.0	2.4	2.4	1.5	0.8	0.4	2.89	1.65	2.64	1.61	8.6	2.4	2.83	1.69	2.1	2.4
1.0	2.4	2.4	1.5	0.8	0.8	3.96	2.24	3.49	2.30	11.8	2.7	3.90	2.22	1.5	< 1.0
1.0	2.4	3.6	1.0	1.5	1.0	3.97	2.21	3.35	2.22	15.6	< 1.0	3.89	2.21	2.0	< 1.0

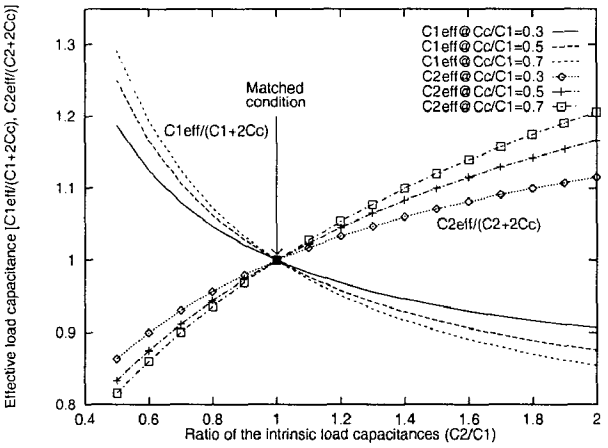

Figure 3: The ratio of the effective load capacitances, $C_{n1_{\text{eff}}}$ and $C_{n2_{\text{eff}}}$ to $C_1 + 2C_c$ and $C_2 + 2C_c$, respectively, for an out-of-phase transition assuming $B_{n1} = B_{p2}$.

the circuit behavior and power dissipation. In the following analysis, Inv_1 is assumed to transition from high-to-low while the input of Inv_2 is fixed at V_{dd}. Therefore, the initial voltage of V_1 and V_2 are V_{dd} and ground, respectively.

When the input voltage exceeds V_{TN}, NMOS_1 is ON and starts operating in the saturation region. NMOS_2 starts operating in the linear region due to the voltage change at the output. The differential equations, (1) and (2), therefore change to

$$(C_1 + C_c)\frac{dV_1}{dt} - C_c\frac{dV_2}{dt} = -B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n}, \quad (26)$$

$$(C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt} = -\gamma_{n2}V_2, \quad (27)$$

where $\tau_n \leq t \leq \tau_r$. There are no tractable solutions to these coupled differential equations. In order to derive a tractable solutions, it is therefore necessary to make certain simplifying assumptions.

5.1 Step Input Approximation

If the transition time of the input signal is assumed to be small as compared to the delay of the CMOS inverters and the output transition time, the input can be approximated as a step input. The output voltages are

$$V_1 = V_{dd} - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n}t + \frac{C_c}{C_1 + C_c}V_2, \quad (28)$$

$$V_2 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{n2}t}), \quad (29)$$

where

$$\alpha_{n2} = \frac{C_1 + C_c}{C_1C_2 + C_c(C_1 + C_2)}\gamma_{n2}. \quad (30)$$

The time τ_{nsat1} when NMOS_1 leaves the saturation region can be determined from (28) by using a Newton-Raphson iteration. After τ_{nsat1}, NMOS_1 operates in the linear region.

The propagation delay of Inv_1 can be approximated using (28) and a Newton-Raphson iteration. Since the current through NMOS_2 discharges the capacitor C_1, the propagation delay is less than the delay estimated based on a load of $C_1 + C_c$. After τ_{nsat1}, both of the NMOS transistors operate in the linear region. Note that V_2 decreases exponentially in the linear region. The peak noise occurs at τ_{nsat1},

$$V_2(peak) = -\frac{C_cB_{n1}(V_{dd} - V_{TN})^{n_n}}{(C_1 + C_c)\gamma_{n2}}(1 - e^{-\alpha_{n2}\tau_{nsat1}}). \quad (31)$$

5.2 Approximation of the Drain-to-Source Current

In order to derive tractable solutions, the drain-to-source current of NMOS_1 can be approximated using a second order polynomial expansion,

$$B_{n1}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} \approx A_0 + A_1\xi + A_2\xi^2, \quad (32)$$

where $\xi = \frac{t}{\tau_r} - \frac{V_{TN}}{V_{dd}}$ and A_0, A_1, and A_2 are determined by a polynomial expansion. The solutions of the differential equations represented by (26) and (27) are

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c}V_{1_a} + \frac{C_c}{C_1 + C_c}V_2, \quad (33)$$

$$V_2 = B_1\xi + B_2\xi^2 + (1 - B_0)e^{-\alpha_{n2}(t-\tau_n)}, \quad (34)$$

where

$$V_{1_a} = B_{n1}\frac{\tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n+1}, \quad (35)$$

and

$$B_0 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_0 + \frac{C_cC_t}{(C_1 + C_c)^2\gamma_{n2}^2\tau_r}A_1 - 2\frac{C_cC_t^2}{(C_1 + C_c)^3\gamma_{n2}^3\tau_r^2}A_2, \quad (36)$$

$$B_1 = 2\frac{C_cC_t}{(C_1 + C_c)^2\gamma_{n2}^2\tau_r}A_2 - \frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_1, \quad (37)$$

$$B_2 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_2, \quad (38)$$

where $C_t = C_1C_2 + C_c(C_1 + C_2)$ and $\tau_n \leq t \leq \tau_r$.

After the input transition is completed, NMOS_1 still operates in the saturation region. The output voltages are

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c}V_{1_a} - \frac{C_c}{C_1 + C_c}V_{1_b}, \quad (39)$$

$$V_2 = -V_{2_a} + (V_2(\tau_r) + V_{2_a})e^{-\alpha_{n2}(t-\tau_r)}, \quad (40)$$

Table 6: Comparison of Inv1 active and Inv2 quiet with SPICE

	Size of Inv		Load Capacitance			Initial	Delay of Inv1					Peak voltage of Inv2		
							SPICE	No Coupling		Analytic		SPICE	Analytic	
τ_r	W_{n1}	W_{n2}	C_1	C_2	C_c	state	τ_1	τ_1	δ_1	τ_1	δ_1	V_2	V_2	δ_2
(ns)	(μm)	(μm)	(pF)	(pF)	(pF)	of Inv2	(ns)	(ns)	%	(ns)	%	(V)	(V)	%
1.0	1.8	1.8	1.0	1.0	0.4	Low	2.11	2.18	3.3	2.11	<1.0	-0.328	-0.32	2.4
1.0	1.8	1.8	1.0	1.0	0.4	High	2.09	2.18	4.3	2.09	<1.0	4.58	4.61	<1.0
1.0	1.8	2.4	1.0	1.0	0.4	Low	2.12	2.18	2.8	2.12	<1.0	-0.258	-0.26	<1.0
1.0	1.8	2.4	1.0	1.0	0.4	High	2.10	2.18	3.8	2.11	<1.0	4.67	4.68	<1.0
1.0	1.8	1.8	1.0	1.0	0.8	Low	2.52	2.77	9.9	2.52	<1.0	-0.528	-0.51	3.4
1.0	1.8	1.8	1.0	1.0	0.8	High	2.47	2.77	12.1	2.48	<1.0	4.32	4.38	1.4
1.0	1.8	2.4	1.0	1.0	0.8	Low	2.57	2.77	7.8	2.57	<1.0	-0.414	-0.42	1.5
1.0	1.8	2.4	1.0	1.0	0.8	High	2.52	2.77	9.9	2.53	<1.0	4.46	4.49	<1.0

where

$$V_{1_a} = (V_{dd} - V_{TN})^{n_n}(t - \frac{n_n V_{dd} + V_{TN}}{(n_n + 1)V_{dd}}\tau_r), \quad (41)$$

$$V_{1_b} = \frac{C_c}{(C_1 + C_c)\gamma_{n2}} B_{n1}(V_{dd} - V_{TN})^{n_n}, \quad (42)$$

$$V_{2_a} = \frac{C_c}{(C_1 + C_c)\gamma_{n2}} B_{n1}(V_{dd} - V_{TN})^{n_n}. \quad (43)$$

$V_2(\tau_r)$ can be determined from (34). τ_{nsat1} and $t_{0.5}$ can also be determined from (39) using a Newton-Raphson iteration. V_2 exhibits an exponential decay when both transistors operate in the linear region. Therefore, the peak coupling noise can be approximated at τ_{nsat1}.

A comparison of the analytical expressions with SPICE simulations is listed in Table 6. The delay is estimated based on the intrinsic load capacitance plus the coupling capacitance, *i.e.*, $C_1 + C_c$ or $C_2 + C_c$, for the no coupling condition. Note that the error of the delay based on $C_1 + C_c$ or $C_2 + C_c$ can reach 16% while the delay based on the analytical equation is within 3% as compared to SPICE. The peak noise based on the analytical expression is within 4% as compared to SPICE.

6 Minimizing Coupling Effects

Coupling effects can be minimized or even eliminated if the circuit elements are appropriately sized for an in-phase transition, as discussed in Section 3.1. Any uncertainty can be eliminated when both of the inverters and load capacitances are the same, *i.e.*, $B_{n1} = B_{n2}$ and $C_1 = C_2$. To reduce the propagation delay of the coupled inverters, the probability of an out-of-phase transition should be minimized because of the large effective load capacitance. In order to minimize any delay uncertainty, all of these circuit elements should be designed as similar to each other as possible.

The coupling noise voltage is proportional to B_{n1}/γ_{n2} and C_c, as described in (31). If the effective output conductance of the quiet inverter is increased, the peak noise voltage can be reduced. This conclusion suggests that the size of the MOS transistors within the quiet inverter should be increased, contradicting the observation for the propagation delay. Therefore, a tradeoff exists between the peak noise and the propagation delay when choosing the appropriate size of the transistors for capacitively coupled inverters. The optimal size of these transistors is also related to the signal activity and other circuit constraints.

7 Conclusions

An analysis of capacitively coupled CMOS inverters is presented in this paper. The uncertainty of the effective load capacitance and the propagation delay is noted for both in-phase and out-of-phase transitions if the circuit elements are not sized the same. The coupling noise voltage on the interconnect line driven by the quiet inverter is also analyzed. Finally, some design strategies are suggested to reduce the noise and delay caused by the interconnect coupling capacitance.

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