Optimum Wire Sizing of RLC Interconnect With Repeaters

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ABSTRACT

Repeaters are often used to drive high impedance interconnects. These lines have become highly inductive which can affect signal behavior in long interconnects. The line inductance should, therefore, be considered in determining the optimum number and size of the repeaters driving a line. A tradeoff exists, however, between the transient power dissipation and the minimum propagation delay in sizing long interconnects driven by repeaters. Optimizing the line width to achieve the minimum power delay product, however, can satisfy current high speed, low power design objectives. A reduction in power of 65% and delay of 97% is achieved for an example repeater system.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]: Miscellaneous–RLC interconnects, power dissipation; B.8.m [**Performance and Reliability**]: Miscellaneous–repeater insertion, propagation delay

General Terms

Design, Performance

Keywords

RLC interconnect, repeater insertion, wire sizing, propagation delay, transient power dissipation, power delay product

1. INTRODUCTION

Interconnect design has become a dominant issue in high speed integrated circuits (ICs). With the decreased feature size of CMOS circuits, on-chip interconnect now dominates both circuit delay and power dissipation. Many algorithms have been proposed to determine the optimum wire size that minimizes a cost function such as delay [1].

The number of long interconnects doubles every three years [2], further increasing the importance of on-chip interconnect inductance. The behavior of inductive interconnect can no longer be neglected, particularly in long, low resistance interconnect lines [3]. As on-chip inductance becomes important, some wire optimization algorithms have been enhanced to consider RLC impedances [4]. Previous work has not considered the effect of interconnect sizing on the repeater insertion process for long inductive lines.

Uniform repeater insertion is an effective technique for driving long interconnects. Based on a distributed RC interconnect model, a repeater insertion technique to minimize signal propagation delay was introduced in [5]. A uniform repeater structure decreases the total delay as compared to a tapered buffer structure when driving long resistive interconnects while buffer tapering is more efficient for driving large capacitive loads [6]. For an RC line, repeater insertion outperforms wire sizing. It is shown in this paper that this behavior is not the case for an RLC line. The minimum signal propagation delay always decreases with the line width for RLC lines if an optimum repeater system is used.

With increasing demands for low power ICs, different strategies have been developed to minimize power in the repeater insertion optimization process. Power dissipation and area overhead have been considered in previous work. The line inductance, however, has yet to be considered in the optimization process of sizing a wire driven by a repeater system.

As shown in Fig. 1, the minimum propagation delay decreases while the power dissipation increases as the interconnect width is increased [7]. In this paper, the tradeoff between signal propagation delay and transient power dissipation in sizing long interconnect driven by a repeater system is discussed. The minimum power delay product is used as a criterion to size long interconnects. Both line inductance and short-circuit power are considered.

The paper is organized as follows. In section 2, the minimum signal propagation delay as a function of interconnect width is presented. In section 3, the dependence of the transient power dissipation on wire size is discussed. A power delay product criterion for sizing an interconnect driven by a repeater system is described in section 4. In section 5, different wire sizing criteria are applied to different systems. Some conclusions are provided in section 6.

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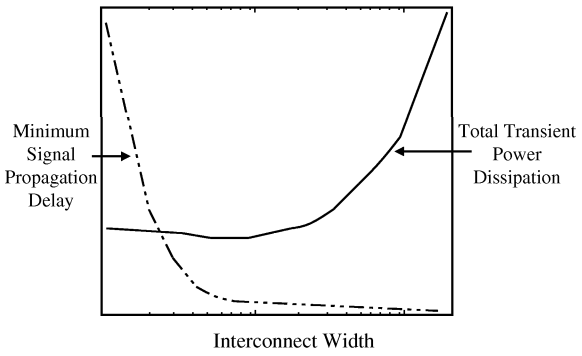

Figure 1: Minimum signal propagation delay and transient power dissipation as a function of line width for a repeater system

2. PROPAGATION DELAY

The objective of a uniform repeater insertion system is to minimize the time for a signal to propagate through a long interconnect. Uniform repeater insertion techniques divide the interconnect into equal sections and employ equal size repeaters to drive each section as shown in Fig. 2. Bakoglu and Meindl have developed closed form expressions for the optimum number and size of repeaters to achieve minimum signal propagation delay in an RC interconnect [5]. Adler and Friedman characterized a timing model for a CMOS inverter driving an RC load [8, 9]. They used this model to enhance the repeater insertion process in RC interconnects. Alpert considered the interconnect width as a design parameter [10]. He showed that, for RC lines, repeater insertion outperforms wire sizing.

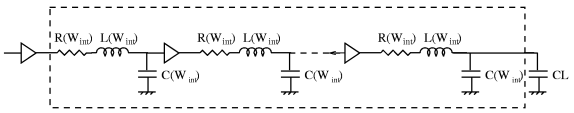

Figure 2: Uniform repeater system driving a distributed RLC interconnect

The delay can be greatly affected by the line inductance, particularly for low resistance materials and fast signal transitions. Ismail and Friedman extended previous research in repeater insertion by considering line inductance [11]. Ismail showed that on-chip inductance can minimize the speed, area, and power of the repeater insertion process as compared to an RC line model. Banerjee and Mehrotra developed a new analytic delay model and a novel methodology for inserting repeaters into distributed RLC interconnect which demonstrated the importance of including line inductance as technology advances [12, 13].

The interconnect resistance decreases with increasing line width, increasing $\frac{L}{R}$, the ratio between the line inductance and resistance, and decreasing the number of inserted repeaters to achieve a minimum propagation delay. For an RLC line, the minimum signal propagation delay deceases with wider wires until no repeaters should be used. Wire sizing outperforms repeater insertion in RLC lines.

For different line lengths l, the optimum number of repeaters $k_{opt-RLC}$ is shown in Fig. 3. It is shown in the figure that for an RLC line the optimum number of repeaters which minimizes the total signal propagation delay decreases with an increase in the line width for all line lengths. The number of repeaters reaches zero (or only one driver at the begining of the line) for an interconnect width = 3 μm and 4 μm for l = 5 mm and 10 mm, respectively. Above a width of 4 μm, the wire should be treated as one segment. A repeater system should not be used above a certain width for each line length.

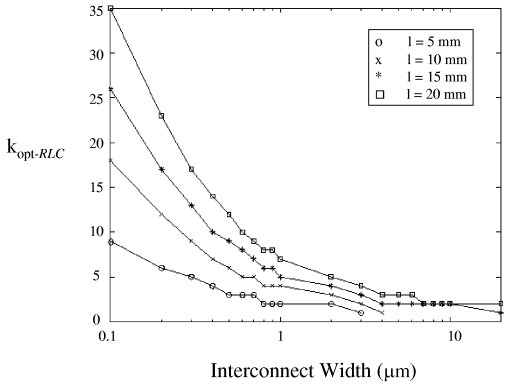

Figure 3: Optimum number of repeaters for minimum propagation delay for different line widths

The line capacitance per unit length increases with line width. As the number of inserted repeaters decreases with wider lines, a longer line section is driven by each repeater. An increase in the section length and width increases the capacitance driven by each repeater. To drive a high capacitive load, a larger repeater size is required to minimize the overall delay. As shown in Fig. 4, the optimum repeater size $h_{opt-RLC}$ is an increasing function of line width.

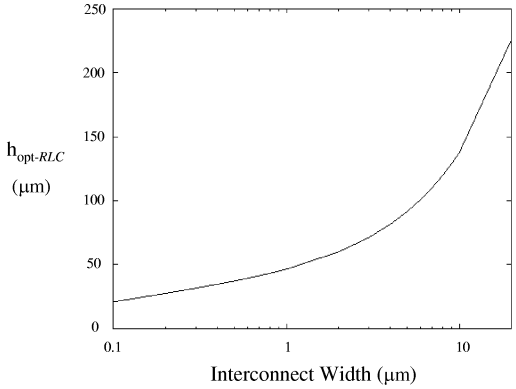

Figure 4: Optimum repeater size for minimum propagation delay for different line widths

The minimum signal propagation delay using an optimum repeater system decreases with increasing line width as the

total gate delay decreases. For an inductive interconnect line, the total signal propagation delay is

$$t_{pd-total} = k_{opt-RLC}\, t_{pd-section}, \quad (1)$$

where $t_{pd-section}$ is the signal delay of each RLC section [11]. The minimum delay [obtained from (1)] is shown in Fig. 5. An increase in the line inductive behavior and a reduction in the number of repeaters decreases the minimum signal propagation delay that can be achieved by a repeater system.

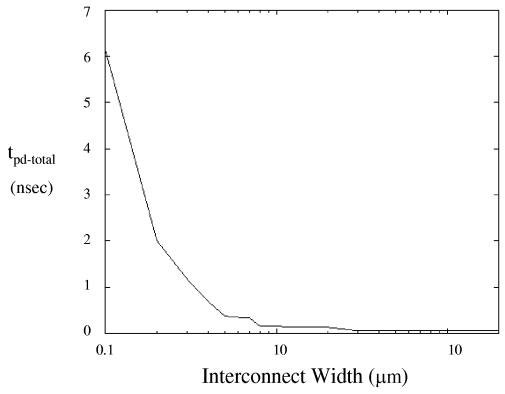

Figure 5: Minimum signal propagation delay as a function of interconnect width (l = 5 mm)

The signal delay for different line lengths is shown in Fig. 6. The lower limit in the propagation delay decreases with increasing line width until the number of repeaters is zero. For a system of repeaters, there is no optimum width at which the total propagation delay is minimum. Rather, the delay is a continuously decreasing function of the line width. This characteristic is an important trend when developing a wire sizing methodology for a repeater system.

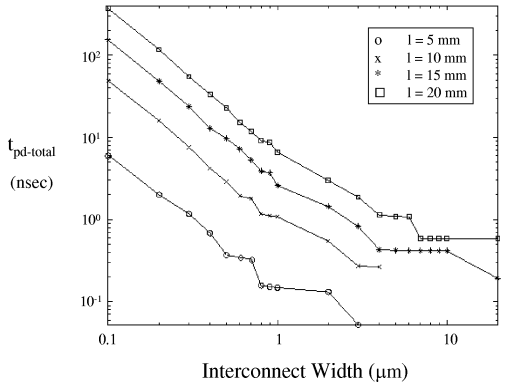

Figure 6: Minimum signal delay as a function of interconnect width for different line lengths

3. POWER DISSIPATION

The power characteristics of a repeater insertion system is discussed in this section. The work described in [14, 15] considers power and area as design constraints. The line inductance, however, has not been considered. In subsection 3.1, the factors that affect the short-circuit power while considering the line inductance of an interconnect driven by a repeater system is analyzed. The dependence of the dynamic power on wire size is described in subsection 3.2. The total transient power dissipation characteristics are summarized in subsection 3.3.

3.1 Short-circuit Power Dissipation

Short-circuit current flows when both transistors within an inverting repeater are simultaneously on. Thin lines dissipate less dynamic power and higher short-circuit power. For thin resistive lines, the number of repeaters can be large. The short-circuit power dissipation in all repeaters along a line is considered. Short-circuit power depends on both the input signal transition time and the load characteristics. A simple and accurate expression for short-circuit power dissipation of a repeater driving an RC load has been presented in [8],

$$P_{sc-section} = \frac{1}{2}\, I_{peak}\, t_{base}\, V_{dd}\, f, \quad (2)$$

where I_{peak} is the peak current that flows from V_{dd} to ground, t_{base} is the time period during which both transistors are on, V_{dd} is the supply voltage, and f is the switching frequency.

Tang used this expression to characterize the short-circuit power of an RLC load [16]. A closed form expression for the signal transition time at the far end of an RLC line has been described in [17]. Increasing the line width has two competing effects on the short-circuit power. As described in [17, 18], the short-circuit power decreases when a line is underdamped. For wide interconnect, the short-circuit power increases as the line capacitance becomes dominant. Furthermore, increasing the length of the section by reducing the number of repeaters increases the short-circuit power of each section because of a higher section impedance.

The total short-circuit power of a repeater system is

$$P_{sc-total} = k_{opt-RLC}\, P_{sc-section}. \quad (3)$$

Equation (3) is used in subsection 3.3 to characterize the total power dissipation in terms of the interconnect width.

3.2 Dynamic Power Dissipation

The dynamic power is the power required to charge and discharge the various device and interconnect capacitances. The total dynamic power is the summation of the CV^2f power from the line capacitance and the repeaters.

$$P_{dyn-total} = P_{dyn-line} + P_{dyn-repeaters}, \quad (4)$$

where

$$P_{dyn-repeaters} = k_{opt-RLC}\, h_{opt-RLC}\, C_0\, {V_{dd}}^2\, f, \quad (5)$$

where C_0 is the input gate capacitance of a minimum size repeater.

$P_{dyn-repeaters}$ depends on both the number and size of each repeater. While the number of repeaters decreases, the repeater size increases.

The dynamic power dissipated by a line increases with greater line capacitance (as the line width is increased). The dynamic power of the repeaters, however, decreases since fewer repeaters are used with wider lines. As shown in Fig. 7, the total dynamic power is a minimum for thin interconnect. The effect of sizing the interconnect on the total transient power dissipation is discussed in subsection 3.3.

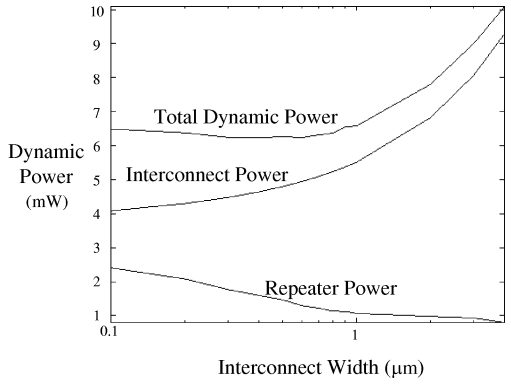

Figure 7: Dynamic power dissipation as a function of interconnect width for l = 20 mm

3.3 Total Power Dissipation

In order to develop an appropriate criterion for determining the optimal interconnect width between repeaters, the total transient power dissipation of a system needs to be characterized. The total transient power can be described as

$$P_{total}(W_{int}) = V_{dd} f [k_{opt-RLC}(W_{int}) (\frac{1}{2} I_{peak}(W_{int})\, t_{base}(W_{int}) + h_{opt-RLC}(W_{int}) V_{dd}\, C_0) + V_{dd}\, C_{int}(W_{int})], \quad (6)$$

where W_{int} is the interconnect width. All of the terms in (6) are functions of the line width except V_{dd}, C_0, and f. As described in subsections 3.1 and 3.2, both transient power components of repeaters decrease with increasing line width, thereby decreasing the total power until the line capacitance becomes dominant.

For an *RLC* interconnect, few repeaters are necessary to drive a line while achieving the minimum propagation delay [11]. For an inductive interconnect, the interconnect capacitance is larger than the input capacitance of the repeaters. Increasing the width reduces the power dissipation of the repeaters and increases the power dissipation of the line. The reduction in power dissipated by the repeaters overcomes the increase in the interconnect power until the line capacitance dominates the line impedance. After exceeding a certain width, the total power increases with increasing line width.

The total power dissipation as a function of line width for different interconnect lengths is shown in Fig. 8. As the line width increases from the minimum width (*i.e.,* 0.1 μm in this case), the total power dissipation is reduced. A minimum transient power dissipation therefore occurs with thin interconnect (see Fig. 8). The minimum transient power dissipation is obtained from

$$\frac{\partial P_{total}}{\partial W_{int}} = 0. \quad (7)$$

$\frac{\partial P_{total}}{\partial W_{int}}$ is a nonlinear function of W_{int}. Numerical methods are used to obtain values of W_{int} for specific interconnect and repeater parameters.

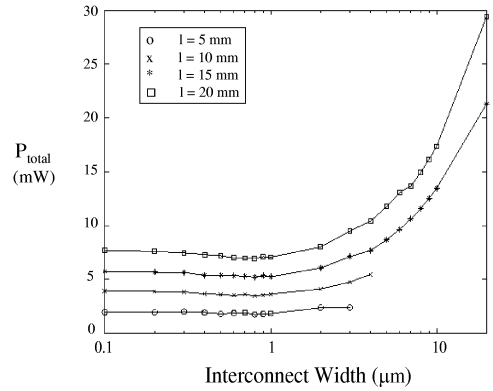

Figure 8: Total transient power dissipation as a function of interconnect width

For a range of reasonable interconnect width, the total transient power increases. As the line length increases, the total power dissipation rapidly increases with increasing line width as the interconnect capacitance becomes dominant. In section 4, the tradeoff between signal delay and power dissipation is considered in the development of a criterion for interconnect sizing.

4. POWER DELAY PRODUCT DESIGN CRITERION

From the discussions in sections 2 and 3, the minimum signal propagation delay of an *RLC* interconnect driven by a repeater system decreases with increasing line width. Alternatively, the total transient power has a global minimum at narrow widths. Over the entire range of line width, the total transient power increases with increasing line width. At a line width smaller than the line width for minimum power, the power and delay both increase. An upper limit on the line width is reached where the minimum propagation delay of a repeater system is attained. Beyond that limit, a single segment sizing criterion should be used to optimize the width according to a cost function (*i.e.,* delay [1] or power [17]). Between these two limits, a tradeoff exists between power dissipation and signal propagation delay. A single expression for the power-delay product as a function of the interconnect width is

$$PDP(W_{int}) = P_{total}(W_{int})^{w_p}\, t_{pd-total}(W_{int})^{w_d}, \quad (8)$$

where w_p and w_d, are the weights of the cost functions. A local minimum for the power delay product exists for each line length. The minimum power delay product is obtained by numerically solving the nonlinear equation,

$$\frac{\partial PDP}{\partial W_{int}} = 0. \quad (9)$$

In the following section, different criteria are applied to different systems to size the interconnect within a repeater system.

5. APPLICATION OF INTERCONNECT DESIGN METHODOLOGY

Optimization criteria have been applied to different repeater systems. The results are summarized in this section. In subsection 5.1, a constrained system is considered. Application to an unconstrained system along with analytical results are provided in subsection 5.2.

5.1 Constrained Systems

For a constrained system, there is a delay target (minimum speed or maximum delay) and/or a limit on the power dissipation. The minimum signal propagation delay determines a lower limit on the line width while the maximum power dissipation determines the upper limit.

If the minimum limit on the line width obtained from (1) is greater than the maximum width obtained from (6), both limits cannot be simultaneously satisfied and one of the design constraints needs to be relaxed. If the minimum limit is lower than the maximum limit, both constraints can be satisfied.

5.2 Unconstrained Systems

For an *RLC* line, there are three criteria to size interconnect in an unconstrained system. The first criterion is for minimum power while sacrificing speed. The optimum solution for this criterion is obtained from (7).

The second criterion is for minimum delay. As no optimum interconnect width exists for minimum propagation delay, the practical limit is either the maximum repeater size or no repeaters, whichever produces a tighter constraint. The criterion in this case is the maximum repeater size or line width. The optimum number of repeaters for a target line width is determined from [11]. Otherwise, no repeaters should be used and the design problem reduces to choosing the width of a single section of interconnect.

The third criterion is to satisfy both the power dissipation and speed. The weights w_p and w_d determine which design objective is more highly valued.

The three criteria are applied to a 0.24 μm CMOS technology to determine the optimum solution for different line lengths. No limit on the maximum buffer size is assumed. In order to characterize the line inductance in terms of the geometric dimensions, an interconnect line shielded by two ground lines is assumed. For a repeater system with the following characteristics, $C_0 = 1\ fF$, and $w_p = w_d = 1$, the optimum solution for each criterion is listed in Table 1.

The optimum line width using each design criterion is listed in the first row of each line length. The optimum number and size of the repeaters for each line width is listed in the second and third row of each line length. The per cent increase in the minimum propagation delay based on the optimum power and power delay product as compared to no repeaters is also listed. The per cent increase in the total transient power dissipation is provided.

For an $l = 5$ mm line, the optimum interconnect width for both minimum power delay product and no repeaters is the same, producing a 14.5% increase in power as compared to the optimum width for minimum power and a reduction of 68% as compared to the optimum width for minimum signal propagation delay.

For short interconnects, few repeaters are needed to produce the minimum propagation delay. For longer interconnect, an increase in the line capacitance rapidly increases the power dissipation, while the minimum propagation delay decreases more slowly.

For $l = 15$ mm, the optimum solution for the minimum power delay product increases the delay by 1.26 rather than 20 times for the solution for minimum power. The power increases by 45% rather than 3.1 times for the no repeater solution. Optimizing the interconnect to produce the minimum power delay product produces a smaller increase in both the power and delay as compared to separately optimizing either the power or delay. A reduction in the minimum propagation delay of 89% and in the power dissipation of 65% is achieved if the optimum width for the minimum power delay product is used rather than the optimum width for either minimum power or no repeaters.

6. CONCLUSIONS

Repeater insertion outperforms wire sizing in *RC* lines. However, for *RLC* lines the minimum signal propagation delay always decreases with increasing wire width if an optimum repeater system is used. In *RLC* lines, wire sizing outperforms repeater insertion as the minimum signal propagation delay with no repeaters is less than the minimum signal propagation delay using any number of repeaters. The minimum signal propagation delay always decreases with wider lines until the number of repeaters equals zero. In *RLC* lines, there is no optimum interconnect width for minimum signal propagation delay.

The total transient power dissipation of a repeater system driving an *RLC* line is minimum at small line widths. Below the width for minimum power, both the signal delay and the power dissipation increase. Increasing the line width above the width for minimum power reduces the number of repeaters and the minimum signal propagation delay while increasing the total transient power dissipation. A tradeoff between the transient power dissipation and the signal propagation delay, therefore, exists in sizing the interconnect width.

Optimizing the interconnect for minimum power delay product produces a much smaller increase in both the power and delay as compared to separately optimizing for either the power or delay. As the interconnects becomes longer, the difference between the optimum width for minimum power and the optimum width for minimum delay increases, further enhancing the effectiveness of the proposed criterion. A reduction in power of 65% and minimum delay of 97% is achieved for an example repeater system driving a long interconnect.

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Table 1: Uniform repeater system for different optimization criteria

l = 5 mm		Minimum Power	No Repeaters	Minimum Power Delay Product
W_{int} (μm)		0.8	2.1	2.1
Number of Repeaters		1	0	0
Repeater Size (μm)		43.3	61.2	61.2
Minimum Delay (nsec)	Total	0.157	0.051	0.051
	Increase	208%	0%	0%
Power (μW)	Total	1730	1980	1980
	Increase	0%	14.5%	14.5%
l = 15 mm		Minimum Power	No Repeaters	Minimum Power Delay Product
W_{int} (μm)		0.8	20	3.9
Number of Repeaters		5	0	1
Repeater Size (μm)		43.2	225.6	80.7
Minimum Delay (nsec)	Total	3.87	0.19	0.43
	Increase	1936%	0%	126.3%
Power (μW)	Total	5200	21,310	7580
	Increase	0%	310%	45.7%

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