Shielding Effect of On-Chip Interconnect Inductance

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ABSTRACT

Interconnect inductance introduces a shielding effect which decreases the effective capacitance seen by the driver of a circuit, reducing the gate delay. The effective capacitance of an RLC load driven by a CMOS inverter is analytically modeled. The interconnect inductance decreases the gate delay and increases the time required for the signal to propagate across an interconnect, reducing the overall signal propagation delay to drive an RLC load. Ignoring the line inductance overestimates the circuit delay, inefficiently oversizing the circuit driver. Considering line inductance in the design process saves gate area, thereby reducing the dynamic power dissipation. A reduction in power of 17% and area of 29% is achieved for an example circuit.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]: Miscellaneous–on-chip inductance, propagation delay; B.8.m [**Performance and Reliability**]: Miscellaneous–propagation delay

General Terms

Design, Performance

Keywords

on-chip inductance, shielding effect, gate delay, propagation delay, interconnect modeling

1. INTRODUCTION

With the decrease in feature size of CMOS circuits, on-chip interconnect dominates both circuit delay and power dissipation. Interconnect resistance increases the importance of modeling the interconnect as a distributed load. The driver gate should also be included in the delay model. Using a reduced order model of the driving point impedance [1]-[3], the concept of an effective capacitance has been introduced in [4, 5] to determine the gate delay. An iterative approach is proposed to determine the delay of a gate driving an RC tree. It has been shown that the effective capacitance of a distributed load is less than the total load capacitance, effectively reducing the gate delay. An enhanced method has been developed to replace the iterative approach [6]. As shown in [7]-[9], an effective capacitance improves the accuracy of the delay model.

The inductive behavior of interconnect can no longer be neglected, particularly in long, low resistance interconnect [10, 11]. The inductive interconnect increases the on-chip noise as well as the computational complexity of the design process. Furthermore, on-chip inductance affects certain design techniques such as repeater insertion [12]. The concept of an effective capacitance based on a high order model for the driving point admittance [13] can be used to determine the gate delay of an RLC load. It is shown in this paper that the on-chip inductance can also decrease the signal propagation delay.

In this paper, a new concept, the shielding effect of an inductive load, is introduced. The line inductance decreases the gate delay and increases the interconnect delay. The total circuit delay may decrease with higher inductance as shown in Fig. 1. The minimum delay occurs when the load is matched with the driver.

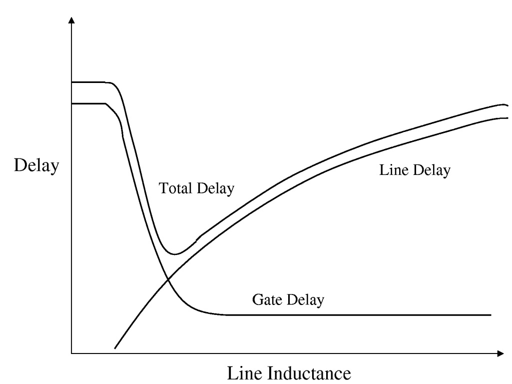

Figure 1: Propagation delay as a function of the line inductance

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From a noise perspective, the line inductance should be suppressed. As presented in this paper, however, the line inductance can save power and area. Furthermore, if the line is matched with the driver, ringing does not appear in the signal waveform.

The paper is organized as follows. In section 2, the effective capacitance of an RLC load as compared to an RC load is presented. The effect of inductive shielding on the total propagation delay is discussed in section 3. Some simulation results are presented in section 4. In section 5, some conclusions are provided.

2. EFFECTIVE CAPACITANCE OF RLC INTERCONNECT

Reduced order models are used to increase the computation efficiency of the timing analysis process. A lumped model for an RLC load which uses the first two moments of the transfer function is shown in Fig. 2a. The lumped model suffers from significant inaccuracy. Furthermore, the shielding effect of the load inductance is not considered. The circuit representation of a three moment reduced order model (π_{21} model) is shown in Fig. 2b [2, 3].

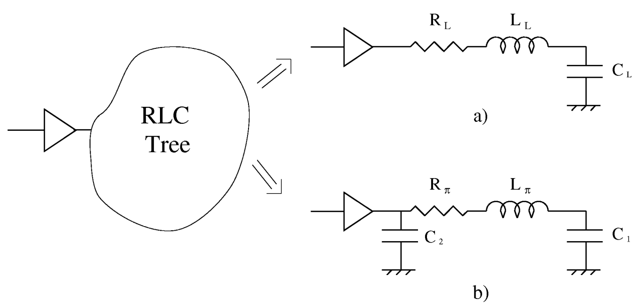

Figure 2: Reduced order model for a general RLC tree a) Lumped model b) π_{21} model

An efficient technique is presented in [14] to determine the values of R_π, L_π, C_1, and C_2 for a general RLC load. If the interconnect inductance is not considered, the RLC π_{21} model reduces to a π_{21} RC model with the same values of R_π, C_1, and C_2 [15, 16].

Intuitively, the effective capacitance is the equivalent capacitance which replaces the reduced order π_{21} model while producing the same delay at the load (as shown in Fig. 3). The effective capacitance of an RLC load is

$$C_{eff-RLC} = C_2 + C_{x-RLC}, \tag{1}$$

where C_{x-RLC} is characterized in Appendix A. C_{x-RLC} is less than C_1, reducing the total capacitance seen by the driver for the π_{21} model as compared to a lumped model. C_{x-RC} for an RC model is determined for an RC load in [5]. C_{x-RLC} is less than C_{x-RC} for an inductive load. C_{x-RLC} decreases with increasing load inductance as the inductive shielding effect increases. The gate delay is linearly proportional to the effective capacitance seen at the driving point. Since the effective capacitance decreases for larger inductances, the gate delay decreases. The interconnect inductance shields part of the load capacitance, reducing the gate delay.

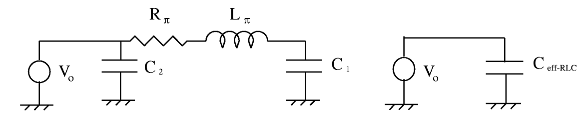

Figure 3: Effective capacitance of RLC π_{21} model

For a total load capacitance and resistance of 400 fF and 100 Ω, respectively, the impedance parameters of the π_{21} model are $R_\pi = 48\ \Omega$, $C_2 = 67$ fF, and $C_1 = 333$ fF [15]. The ratio between the effective capacitance of the RLC and RC π_{21} models for different load inductances is shown in Fig. 4. The effective capacitance decreases as the load inductance increases. The waveform illustrated in Fig. 4 does not have a monotone shape due to the existence of the line inductance.

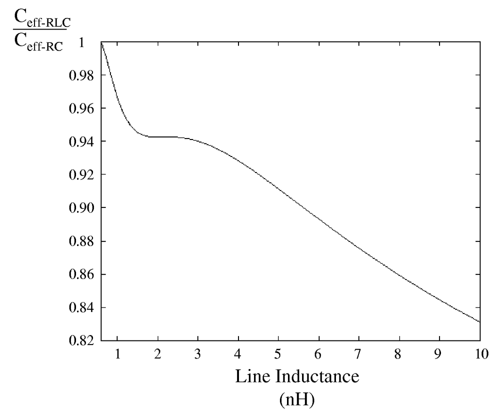

Figure 4: Ratio between the effective capacitance of an RLC and RC load

The shielding effect of the interconnect inductance increases the importance of including the line inductance in the delay analysis. Ignoring the inductance overestimates the circuit delay, requiring an oversized buffer to drive the load. The effect of the interconnect inductance on the total signal propagation delay is discussed in section 3.

3. EFFECT OF LINE INDUCTANCE ON THE DELAY MODEL

The effective capacitance can be used to characterize the gate delay. The signal propagation delay depends on the active gate and passive interconnect components of the signal path. The gate delay is the time required to charge the capacitance seen by the driver through the equivalent resistance of the driver. The interconnect delay is the time required for the signal to propagate through the line. These two components cannot be separated as the driver and load represent a single system. The interconnect inductance reduces both the capacitance seen by the driver (as described in section 2) and the equivalent output resistance of the driver, reducing the overall gate delay.

For an ideal source driving a distributed RLC line, however, the signal delay is primarily due to the line delay. Lline inductance increases the signal propagation delay. For an ideal source driving an RLC line, the line delay can be modeled as [12]

$$t_{pd-RLC} = \frac{e^{-2.9\zeta^{1.35}}}{\omega_n} + 0.74 R_{line}(C_L + 0.5C_{line}), \quad (2)$$

$$\zeta = \frac{R_{line}\omega_n}{2}(0.5C_{line} + C_L), \quad (3)$$

$$\omega_n = \frac{1}{\sqrt{L_{line}(C_{line} + C_L)}}, \quad (4)$$

where C_L is the load capacitance driven by the line and R_{int}, C_{int}, and L_{int} are the total line resistance, capacitance, and inductance, respectively.

The line delay increases with the line inductance as shown in Appendix B. As the line inductance increases, two competing effects change the total delay of the signal. The delay due to the active transistor decreases while the delay due to the passive interconnect increases. A closed form solution characterizing the signal propagation delay of an inverter driving a reduced order π_{21} model of a distributed RLC line is presented in Appendix C. A comparison between this model and two related models is provided in section 4.

To exemplify the effect of the line inductance on the propagation delay, a CMOS inverter driving a long (inductive) interconnect with $R_{line} = 50\ \Omega$ and $C_{line} = 400$ fF is considered. The total delay for different driver sizes based on a 0.24 μm CMOS technology is shown in Fig. 5. Different values of the line inductance with $C_L = 50$ fF are considered.

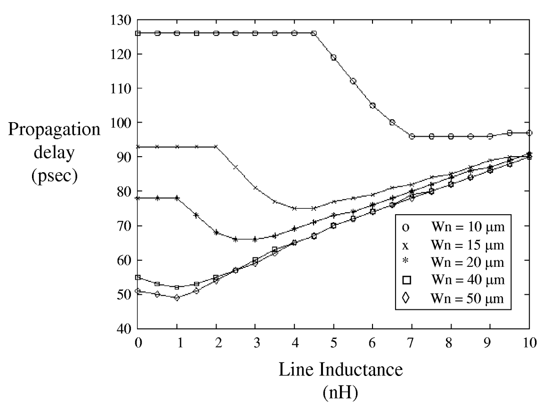

Figure 5: Total delay for different values of line inductance and driver size of a distributed RLC interconnect as estimated by the Cadence simulator

The propagation delay decreases with increasing line inductance until a minimum delay is reached. The total delay decreases with higher line inductance over a wide range of driver size (the NMOS transistor size W_n ranges from 10 μm to 50 μm). For small drivers (*i.e.,* $W_n < 5\,\mu$m), the line inductance has no effect on the propagation delay as the delay is dominated by the driver output resistance (and the line does not behave inductively). For large drivers (*i.e.,* $W_n > 50\,\mu$m), the line inductance increases the delay. The output resistance of these drivers is small and the interconnect delay dominates the total delay. Large drivers are not preferred as the decrease in signal delay is not significant, while the required area and dissipated power are large. Furthermore, the input gate capacitance increases with larger drivers, increasing the delay of the previous logic stage. Buffer tapering can be used for large drivers, but the power dissipation increases with the added inverters (cascaded tapered inverters [17]) employed to reduce the delay.

Curve fitting is employed to determine the optimum value of the line inductance to achieve the minimum propagation delay. The minimum delay is determined over a wide range of line inductance (from 0.1 to 10 nH), load capacitance (from 10 to 250 fF), inverter size (from 5 to 50 μm), line capacitance (from 100 fF to 1 pF), and line resistance (from 25 to 100 Ω) . The minimum delay occurs when the ratio between the equivalent output resistance of the driver R_{tr} equals the magnitude of the lossy characteristic impedance of the line $|Z_{line}|$ or $Z_T = 1$,

$$Z_T = \frac{R_{tr}}{|Z_{line}|}, \quad (5)$$

$$R_{tr} = \frac{V_{dd}}{k_n(V_{dd} - V_{tn})^{\alpha}} + \frac{V_{dd}}{k_n[2(V_{dd} - V_{tn})V_{dd} - \frac{V_{dd}^2}{2}]}, \quad (6)$$

$$|Z_{line}| = \sqrt{\frac{\sqrt{R_{line}^2 + (\omega L_{line})^2}}{\omega C_{line}}}, \quad (7)$$

$$\omega = \frac{2\pi}{t_r}, \quad (8)$$

where V_{dd} is the supply voltage, k_n is the transconductance of the NMOS transistor of the driving inverter, V_{tn} is the threshold voltage of an NMOS transistor, $\alpha = 1.3$ and models the velocity saturation in a short-channel transistor, and t_r is the signal transition time at the output of the driving inverter.

The total propagation delay increases if the line inductance is less than the matched condition. Ignoring the line inductance overestimates the delay and the size of the driver. The line inductance is considered in section 4 in the design of an inverter driving a section of RLC interconnect. The savings in both power and area if the line inductance is considered is noted.

4. SIMULATION RESULTS

Three different models are used to illustrate the importance of an accurate model to represent both the driver and the interconnect. In Table 1, a comparison between the model provided in [12], a lumped RLC model, and the π_{21} model (which is described in Appendix C) is listed.

The line inductance reduces the total signal propagation delay as discussed in the previous sections. Including the inductance in the interconnect model is important in the design of an appropriate driver. Excluding the inductance overestimates the delay of the circuit and underestimates the current sourced by the driver. Including the line inductance can reduce the driver size, saving area and power.

A 0.24 μm CMOS technology is used to demonstrate the effect of including line inductance in the design of a line driver. An interconnect line with $R_{line} = 10\ \Omega/mm$, C_{line} = 105 fF/mm, and $L_{line} = 650$ pH/mm is assumed to determine the reduction in the size of the line driver if inductance

Table 1: Propagation delay using different models for different line inductances

$W_n = 20\ \mu$m, $R_{line} = 50\ \Omega$															
L_{line}	$C_{line} = 400$ fF							$C_{line} = 1$ pF							
nH	Cadence	Ismail [12]		Lumped		π_{21}		Cadence	Ismail [12]		Lumped		π_{21}		
	(psec)	psec	Err	psec	Err	psec	Err	(psec)	psec	Err	psec	Err	psec	Err	
0.0	77	35.2	-54.2	59.5	-22.7	68.2	-11.3	148	86.3	-41.6	97.8	-33.8	130.1	-12	
1.0	74	35.7	-51.7	62.2	-15.8	70	-5.4	147	86.4	-41.2	93.3	-36.5	129.6	-11.7	
2.0	67	38.1	-43	66.6	-0.5	64.7	-3.4	153	87.0	-43	86.5	-43.4	131.5	-14	
3.0	68	41.4	-39	97.8	43.8	63.3	-6.8	145	88.7	-38.7	81.1	-44	134.2	-7.3	
4.0	70	45	-35.6	101.8	45.5	72.6	3.8	132	91.1	-30.9	76.6	-41.9	122.5	-7.1	
5.0	73	48.6	-33.4	105.2	44.1	80.3	10	118	94	-20.2	96.8	-17.8	117.1	-0.7	
Maximum		-54.27		-45.95		-11.35			-43		-45.64		-14		
Average		41.51		30.75		6.11			36.23		38.69		8.91		

Table 2: Reduction in area and power dissipation when considering line inductance for different dielectric and line materials

Dielectric Material	Resistivity	Target Delay (psec)	W_n (μm)		Per cent reduction in power dissipation	Per cent reduction in area
			RC	RLC		
SiO_2	Aluminum	100	19	16.5	5%	13%
	Copper	100	17.8	15.2	6%	15%
Low-K	Aluminum	60	23	19	9%	17%
	Copper	60	21	15	17%	29%

is considered. A symmetric CMOS inverter is used to drive a line loaded by a capacitive load of 50 fF to achieve a target delay. The target delay and the driver size that achieves this delay are listed in Table 2. A reduction in power dissipation of 5% and gate area of 13% is achieved if the line inductance is considered. As technology advances, different dielectric and line materials will be used to reduce the interconnect delay. Using low-k dielectric materials and copper interconnect will reduce both the line capacitance and resistance, increasing the effect of inductance on the signal behavior. A 17% reduction in power dissipation and 29% reduction in gate area are achieved for an example circuit.

5. CONCLUSIONS

The shielding effect of interconnect inductance is introduced. The effective capacitance of an RLC load decreases with increasing line inductance, reducing the gate delay of a driver. Furthermore, the line inductance reduces the equivalent output resistance of a driver, reducing the total propagation delay. A parameter Z_T, the ratio of the output driver resistance and the magnitude of the line lossy characteristic impedance, is introduced to characterize the signal propagation delay of a CMOS inverter driving an RLC interconnect. The minimum propagation delay is achieved when $Z_T = 1$ where the driver is matched with the lossy characteristic impedance of the line.

The line inductance affects the design process. A smaller driver can be used to drive an interconnect line if the line inductance is considered, more accurately achieving the target delay than if the line inductance is ignored. The per cent savings in both area and power dissipation is expected to increase as technology advances. A reduction of 17% in power dissipation and 29% in gate area is achieved for an example circuit.

APPENDIX

A. EFFECTIVE CAPACITANCE OF AN RLC LOAD

In order to compare the effective capacitance of RC and RLC delay models, the signal transition time at the output of a driving inverter V_o is assumed equal for both interconnect models. The waveform used in [5] is assumed to compare the effective capacitance of an RLC model with the capacitance obtained in [5].

$$V_o(t) = \begin{cases} V_{dd} - ct^2 & \text{for } 0 \leq t \leq t_x, \\ a + b(t - t_x) & \text{for } t_x \leq t \leq t_D, \end{cases} \tag{A.1}$$

where $b = -0.8\frac{V_{dd}}{t_r}$ and t_x, t_D, a, and c are constants that characterize the waveform of V_o. t_r is the transition time of V_o which is obtained iteratively after determining the effective capacitance. The waveform of a signal propagating along an RLC line may be distorted by the inductance; however, the effect of this distortion on the effective capacitance is not significant. The effective capacitance of the π_{21} model is the capacitance which draws a current equal to the average current from both C_1 and C_2 in the π_{21} model [4]. The average currents, I_{c1-av} and I_{c2-av}, discharge (for an output high-to-low transition) the capacitances C_1 and C_2, respectively, as shown in Fig. 6.

Laplace transforms are used to obtain an expression for I_{c1-av}. The average I_{c1-av} during a high-to-low transition

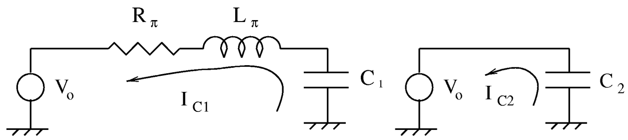

Figure 6: Discharge currents for the RLC π_{21} model

is

$$I_{c1-av} = \frac{I_{c1-av-I}t_x + I_{c1-av-II}(t_D - t_x)}{t_D}, \tag{A.2}$$

$$\begin{aligned} I_{c1-av-I} &= \frac{-1}{t_x L_\pi}(A\frac{{t_x}^2}{2} + Bt_x + D \\ &+ Ee^{-\alpha_1 t_x} + Fe^{-\alpha_2 t_x}) + C_1\frac{V_{dd}}{t_x}, \end{aligned} \tag{A.3}$$

$$\begin{aligned} I_{c1-av-II} &= \frac{-1}{(t_D - t_x)L_\pi}((A_1(t_D - t_x) + B_1 \\ &+ D_1 e^{-\alpha_1(t_D - t_x)} + E_1 e^{(-\alpha_2(t_D - t_x))}) \\ &+ C_1\frac{V_{C1t_x}}{(t_D - t_x)}, \end{aligned} \tag{A.4}$$

$$\begin{aligned} V_{C1t_x} &= \frac{1}{C_1 L_\pi}(A\frac{t_x^2}{2} + Bt_x + D \\ &+ Ee^{-\alpha_1 t_x} + Fe^{-\alpha_2 t_x}), \end{aligned} \tag{A.5}$$

$$A = -2cL_\pi C_1, \tag{A.6}$$

$$B = -2cR_\pi L_\pi C_1^2, \tag{A.7}$$

$$D = -(E + F) + V_{dd}L_\pi C_1, \tag{A.8}$$

$$E = \frac{E_0}{\alpha_1^3(\alpha_1 - \alpha_2)}, \tag{A.9}$$

$$F = \frac{F_0}{\alpha_2^3(\alpha_2 - \alpha_1)}, \tag{A.10}$$

$$\begin{aligned} E_0 &= -2c + \alpha_1^2 V_{dd} + \alpha_1^4 V_{dd} L_\pi C_1 \\ &- \alpha_1^3(R_\pi C_1 V_{dd}), \end{aligned} \tag{A.11}$$

$$\begin{aligned} F_0 &= -2c + \alpha_2^2 V_{dd} + \alpha_2^4 V_{dd} L_\pi C_1 \\ &- \alpha_2^3(R_\pi C_1 V_{dd}), \end{aligned} \tag{A.12}$$

$$\alpha_1 = \frac{\frac{R_\pi}{L_\pi} + \sqrt{(\frac{R_\pi}{L_\pi})^2 - \frac{4.0}{L_\pi C_1}}}{2}, \tag{A.13}$$

$$\alpha_2 = \frac{\frac{R_\pi}{L_\pi} - \sqrt{(\frac{R_\pi}{L_\pi})^2 - \frac{4.0}{L_\pi C_1}}}{2}, \tag{A.14}$$

$$A_1 = L_\pi C_1 b, \tag{A.15}$$

$$B_1 = L_\pi C_1 V_{C1t_x} - D_1 - E_1, \tag{A.16}$$

$$D_1 = \frac{D_2}{\alpha_1^2(\alpha_2 - \alpha_1)}, \tag{A.17}$$

$$\begin{aligned} E_1 &= \frac{E_2}{\alpha_2^2(\alpha_1 - \alpha_2)}, \\ &- \alpha_2 F e^{-\alpha_2 t_x}), \end{aligned} \tag{A.18}$$

$$\begin{aligned} D_2 &= b - \alpha_1 a + \alpha_1^2(kL_\pi C_1 + R_\pi C_1 V_{C1t_x}) \\ &- \alpha_1^3 L_\pi C_1 V_{C1t_x}, \end{aligned} \tag{A.19}$$

$$\begin{aligned} E_2 &= b - \alpha_2 a + \alpha_2^2(kL_\pi C_1 + R_\pi C_1 V_{C1t_x}) \\ &- \alpha_2^3 L_\pi C_1 V_{C1t_x}, \end{aligned} \tag{A.20}$$

$$k = \frac{1}{C_1 L_\pi}(At_x + B - \alpha_1 E e^{-\alpha_1 t_x} \tag{A.21}$$

$$- \alpha_2 F e^{-\alpha_2 t_x}). \tag{A.22}$$

Equalizing the average current driving an effective capacitance $I_{Ceff-av}$ with the summation of I_{C1-av} and I_{C2-av}, the effective capacitance $C_{eff-RLC}$ can be expressed as

$$C_{eff-RLC} = C_2 + C_{x-RLC}, \tag{A.23}$$

where

$$C_{x-RLC} = \frac{t_D}{2ct_x(t_D - \frac{t_x}{2})} I_{c1_{av}}. \tag{A.24}$$

B. DEPENDENCE BETWEEN LINE INDUCTANCE AND PROPAGATION DELAY

The delay of a signal propagating through an interconnect line increases as the line inductance increases. The line inductance impedes the propagation of the signal through the line. This behavior can be shown analytically by differentiating the delay expression in [12] with respect to the line inductance. The sign of the differentiation determines whether the delay increases or decreases with inductance. A negative solution means that the delay decreases with an increase in the line inductance.

The delay expression in [12] is differentiated with respect to the line inductance, permitting the range of line damping factor ζ where the sign of the differentiation changes to be obtained. The delay decreases with the line inductance over the range at which the differentiation is negative. This condition is satisfied by the differentiation if

$$\zeta > \frac{2.8e-3}{{L_{line}}^{2.86}} . \tag{B.1}$$

The differentiation is negative when (B.1) is satisfied. The line propagation delay is an increasing function of the line inductance as (B.1) cannot be satisfied and the differentiation is always positive in practical circuits.

C. PROPAGATION DELAY OF CMOS INVERTER DRIVING Π_{21} RLC LOAD

In order to determine a closed form solution of the propagation delay assuming a π_{21} model, an expression for the signal across C_2 during a high-to-low transition is

$$\begin{aligned} V_c(t) &= \frac{1}{C_1 C_2 L_\pi}(A_2 e^{a_1(t-\tau_{nsat})} + B_2 e^{b_1(t-\tau_{nsat})} \\ &+ D_2 e^{d_1(t-\tau_{nsat})}), \end{aligned} \tag{C.1}$$

$$A_2 = \frac{\theta + C_2 V_{c2}(a_1 C_1 + \gamma_n)(R_\pi + a_1 L_\pi)}{(a_1 - b_1)(a_1 - d_1)}, \tag{C.2}$$

$$B_2 = \frac{\theta + C_2 V_{c2}(b_1 C_1 + \gamma_n)(R_\pi + b_1 L_\pi))}{(b_1 - a_1)(b_1 - d_1)}, \tag{C.3}$$

$$D_2 = \frac{\theta + C_2 V_{c2}(d_1 C_1 + \gamma_n)(R_\pi + d_1 L_\pi)}{(d_1 - a_1)(d_1 - b_1)}, \tag{C.4}$$

$$\theta = C_1 V_{o2} + C_2 V_{c2}, \tag{C.5}$$

where V_{o2} and V_{c2} are the voltage across C_1 and C_2, respectively, when the PMOS transistor of the driving inverter turns off.

$$\gamma_n = \alpha B_n (V_{dd} - V_{tn})^{(n_n - m_n)}, \tag{C.6}$$

where α, B_n, V_{tn}, n_n, and m_n are the n^{th} power law transistor parameters [18] and V_{dd} is the supply voltage. a_1, b_1, and d_1 are the roots of the polynomial,

$$x^3 + e_2 x^2 + e_1 x + e_0 = 0, \tag{C.7}$$

where

$$e_0 = \frac{C_1 C_2 R_\pi + \gamma_n C_2 L_\pi}{C_1 C_2 L_\pi}, \tag{C.8}$$

$$e_1 = \frac{C_2 + C_1 + C_2 R_\pi \gamma_n}{C_1 C_2 L_\pi}, \tag{C.9}$$

$$e_2 = \frac{\gamma_n}{C_1 C_2 L_\pi}. \tag{C.10}$$

The propagation delay can be determined by numerically solving the nonlinear equation (C.11).

$$V_c(t_{50\%}) - \frac{V_{dd}}{2} = 0. \tag{C.11}$$

The propagation delay is

$$t_{pd} = t_{50\%} - \frac{t_{r-In}}{2}, \tag{C.12}$$

where t_{r-In} is the transition time of the input signal of the driving gate.

6. REFERENCES

[1] L. T. Pillage and R. A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 9, No. 4, pp. 352-366, April 1990.

[2] P. R. O'Brien and T. L. Savarino, "Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation," *Proceedings of the IEEE International Conference on Computer-Aided Design*, pp. 512-515, November 1989.

[3] P. R. O'Brien and T. L. Savarino, "Efficient On-Chip Delay Estimation for Leaky Models of Multiple-Source Nets," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 9.6.1-9.6.4, May 1990.

[4] C. L. Ratzaff, S. Pullela, and L. Pillage, "Modeling the *RC*-Interconnect Effects in a Hierarchical Timing Analyzer," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 15.6.1-15.6.4, May 1992.

[5] J. Qian, S. Pullela, and L. Pillage, "Modeling the 'Effective Capacitance' for the *RC* Interconnect of CMOS Gates," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 12, pp. 1526-1535, December 1994.

[6] A. B. Kahng and S. Muddu, "New Efficient Algorithms for Computing Effective Capacitance," *Proceedings of the ACM International Symposium on Physical Design*, pp. 147-151, April 1998.

[7] F. Dartu, N. Menezes, J. Qian, and L. T. Pillage, "A Gate-Delay Model for High-Speed *RLC* Circuits," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 576-580, June 1994.

[8] C. V. Kashyap, C. J. Alpert, and A. Devgan, "An Effective Capacitance Based Delay Metric for *RC* Interconnect," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 229-234, November 2000.

[9] C. J. Alpert, A. Devgan, and S. T. Quay, "Buffer Insertion With Accurate Gate and Interconnect Delay Computation," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 479-584, June 1999.

[10] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figure of Merit to Characterize the Importance of On-Chip Inductance," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 7, No. 4, pp. 442-449, December 1999.

[11] B. Krautr, S. Mehrotra, and V. Chandramouli, "Including Inductive Effects in Interconnect Timing Analysis," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 445-452, May 1999.

[12] Y. I. Ismail and E. G. Friedman, "Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 8, No. 2, pp. 195-206, April 2000.

[13] R. Arunachalam, F. Dartu, and L. T. Pileggi, "CMOS Gate Delay Models for General *RLC* Loading," *Proceedings of the IEEE International Conference on Computer Design*, pp. 224-229, October 1997.

[14] X. Yang, C-K. Chang, W. H. Ku, and R. J. Carragher, "Hurwitz Stable Reduced Order Modeling for *RLC* Interconnect Trees," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 222-228, November 2000.

[15] A. B. Kahng and S. Muddu, "Efficient Gate Delay Modeling for Large Interconnect Loads," *Proceedings of the IEEE Multi-Chip Module Conference*, pp. 202-207, February 1996.

[16] L. Yin and L. He, "An Efficient Analytical Model of Coupled On-Chip *RLC* Interconnects," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 385-390, January 2001.

[17] B. S. Cherkauer and E. G. Friedman, "A Unified Design Methodology for CMOS Tapered Buffers," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. VLSI-3, No. 1, pp. 99-111, March 1995.

[18] T. Sakurai and A. R. Newton, "A Simple MOSFET Model for Circuit Analysis," *IEEE Transactions on Electron Devices*, Vol. 38, No. 4, pp. 887-894, April 1991.