Sensitivity Evaluation of Global Resonant H-Tree Clock Distribution Networks

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ABSTRACT
A sensitivity analysis of resonant H-tree clock distribution networks is presented in this paper for a TSMC 0.18 μm CMOS technology. The analysis focuses on the effect of the driving buffer output resistance, on-chip inductor and capacitor size, and signal and shielding transmission line width and spacing on the output voltage swing and power consumption. A two level resonant H-tree network exhibits low sensitivity to these variations.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Advanced technologies, VLSI (very large scale integration).*

General Terms
Design.

Keywords
Resonance, clock distribution networks, on-chip inductors and capacitors, H-tree sector, sensitivity.

1. INTRODUCTION
In modern VLSI circuits fabricated in nanometer processes, significant variations are exhibited. Imperfections in the manufacturing process and environmental effects can degrade overall system performance [1, 2]. Interconnect process variations can affect, for example, timing analysis, buffer insertion, high density SRAMs, and clock distribution networks [3-5].

To lower the power dissipation in clock distribution networks, new concepts have been proposed [6-9]. These novel clock distribution networks aim to lower the power while improving clock signal skew and jitter. Such networks, however, must be highly tolerant to process and environmental variations in order to produce feasible solutions.

Clock generation and distribution networks based on *LC* oscillators in the form of transmission line systems have been considered. In salphasic clock distribution networks [6], a sinusoidal standing wave is established within a transmission line. Coupled standing oscillators of this type are used in [7] to distribute a high frequency clock signal. A similar approach uses traveling waves in coupled transmission line loops [8] driven by distributed cross coupled inverters. In [9-11], a resonant global clock distribution network is described. The sensitivity due to process variations in resonant H-tree clock distribution networks [11] is evaluated in this paper.

This paper is organized into the following sections. Resonant clock networks are described in section 2. In section 3, the sensitivity of clock distribution networks to certain design parameters is examined. Some conclusions are offered in section 4.

2. BACKGROUND
The concept of exploiting resonant transmission lines was first introduced by Chi in 1994 [6]. A global resonant clock distribution network was later introduced in 2003 by Chan *et al.* [9]. In [11], an accurate model of a two level resonant H-tree sector is presented and a design methodology is described for determining the on-chip spiral inductors, capacitors, and driving buffer resistance that produces the minimum power consumption. The on-chip spiral inductors and capacitors are attached to a traditional H-tree structure, as depicted in Figure 1. The on-chip spiral inductors are connected at four points in the tree, while the decoupling capacitors are attached to the opposite side of the spiral inductors.

The capacitance of the clock distribution network resonates with the inductance, while the on-chip capacitors establish a mid-rail DC voltage around which the grid oscillates. This approach lowers the power consumption, since the energy resonates between the electric and magnetic fields rather than dissipated as heat. Consequently, the number of gain stages is reduced, resulting in further reductions in power consumption, skew, and jitter. The resonant sector (such as the network shown in Figure 1) can be used as a building block to construct a much larger global clock distribution network.

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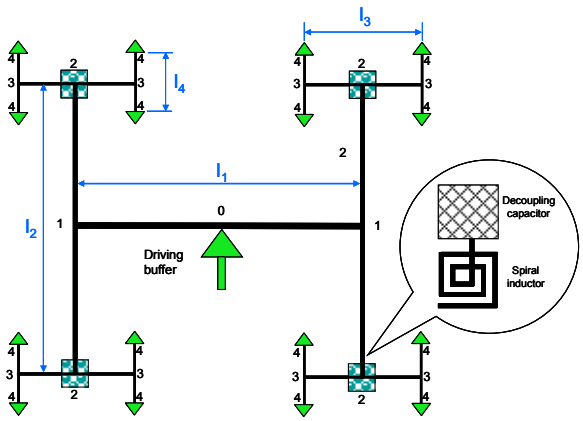

Figure 1. H-tree sector with on-chip inductors and capacitors

The design methodology described in [11] considers the physical geometry of the structure and the technology, and is formulated as

$$\text{H-Tree Sector} = f\left(w_i, l_i, h_i, f_o, C_l\right) \ \forall i, \qquad (1)$$

where w_i, l_i, and h_i are the width, length, and thickness of each section of the H-tree sector, respectively, f_o is the clock frequency, and C_l is the capacitive load at each leaf node. The index i varies between one and four, representing each section of the H-tree sector (see Figure 1). Process and environmental variations may affect the geometric parameters w_i, l_i, and h_i. These variations may alter the output design function described by (1), deviating from the optimal solution. To produce feasible solutions such as the network shown in Figure 1, the network should be highly tolerant to process variations, a topic discussed in the next section.

3. SENSITIVITY OF H-TREE SECTOR

The effect of process variations on the performance of the resonant H-tree sector is explored in this section. In particular, six types of circuit variations are considered: the driving buffer output resistance, on-chip inductor and capacitor size, and signal and shielding transmission line width and spacing. These variations are examined with respect to two performance figures of merit: the clock signal voltage swing at the leaf nodes and the power consumption.

The physical structure of the H-tree is described in section 3.1. A model of the on-chip spiral inductor is discussed in section 3.2, and finally, a sensitivity analysis is presented for the structure described in subsection 3.3.

3.1 Physical Structure of H-tree Sector

The layout geometry and configuration of a symmetric balanced resonant H-tree sector is schematically illustrated in Figure 2. Assuming a 5 GHz clock signal, the investigation is performed on a resonant H-tree based on a CMOS 0.18 µm TSMC technology.

The H-tree sector including the on-chip inductors and capacitors occupies two metal layers, metal 5 and metal 6, for a total area of 2500 × 2500 µm^2. The horizontal transmission line and capacitors are placed on metal 6, while the vertical transmission lines and spiral inductors are located on metal 5. This strategy reduces the coupling between the lines. In order to further reduce coupling noise, each signal line is shielded by two parallel ground lines. The separation distance s between the ground and signal lines is constant and equals 4 µm, while the signal and ground line lengths and widths are the same in each section, *i.e.*, $w_{GND} = w_s = w_i$, where i varies between one and four. The metal line heights have the same constant value of h = 0.5 µm.

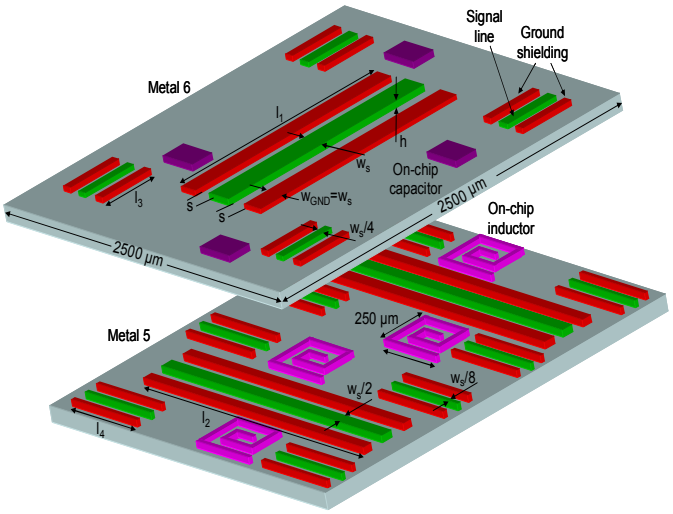

Figure 2. Structure of resonant H-tree sector

The capacitors are connected to the ground lines, while the other ends of the spiral inductors are connected to a signal line, namely, to l_4 (the connection is not shown on Figure 2). Finally, note that the width of the signal lines are reduced by two at each branching point in order to reduce reflections caused by differences between the characteristic impedances at the branch points. The interconnect widths and lengths, indicated on Figure 2 and used in this example, are listed in Table 1.

Table 1. Resonant H-tree Parameters

l_1, w_1 [µm]	l_2, w_2 [µm]	l_3, w_3 [µm]	l_4, w_4 [µm]
1600, 16	1600, 8	800, 4	800, 2

The resistance, inductance, and capacitance per unit length of the transmission lines are extracted using HENRY™ and METAL™ from the OEA software suite [12]. For the technology and geometry described above (see Figure 2), the extracted interconnect parameters are listed in Table 2. Inverters are located at the leaf nodes of the H-tree sector, driving a load of 20 fF.

Table 2. Extracted transmission line parameters

i	R_i [mΩ/µm]	L_i [pH/µm]	C_i [fF/µm]
1	3.1875	1.194	0.2765
2	6.375	1.427	0.296
3	12.75	1.535	0.1259
4	25.5	1.7845	0.14

In order to determine the minimum power consumption, the design methodology described in [11] is applied in this example.

The spiral inductance is chosen as L_s = 2 nH, the driving buffer output resistance is $R_g \approx 25\ \Omega$, and the corresponding on-chip capacitor is C_d = 15 pF.

The 5 GHz output waveform at the leaf nodes described in the time domain is shown in Figure 3. Note that a square clock waveform is distributed to the leaf node, achieving a full rail-to-rail voltage swing, and exhibiting a power consumption of 15 mW (including the buffers at the leaves).

3.2 Model of H-tree Spiral Inductor

On-chip spiral inductors play an important role in the design of silicon-based RF integrated circuits (ICs). On-chip spiral inductors can be integrated into the fabrication process of a standard CMOS technology.

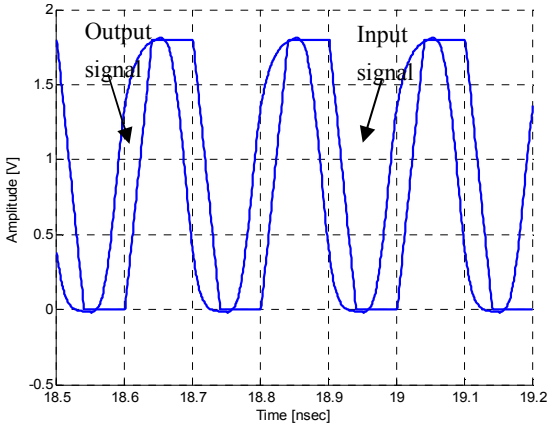

Figure 3. Output waveform at the leaf nodes

Unfortunately, particularly in processes with a heavily doped silicon substrate, substrate losses resulting from eddy current effects can be significant [13, 14]. It is therefore important to accurately model the resistive losses of the on-chip spiral inductors.

The most commonly used compact spiral inductor model is the so-called "nine element" π-model. To simplify the analysis, however, a simpler model as shown in Figure 5 is used.

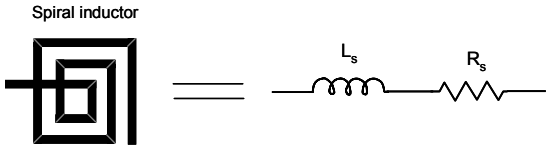

Figure 5. Simplified model of an on-chip spiral inductor

In this model, only the inductance and resistance are considered. The parasitic resistance of a spiral inductor greatly affects the behavior of the resonant clock sector [11], and should be included in the design process. To determine the value of the on-chip spiral inductors and the effective series resistance (ESR), customized extraction software, Asitic, is used [15].

In this example, spiral inductors, occupying an area of 250 x 250 μm^2, are optimized for maximum Q. The ESR for a range of inductor values at certain frequencies is shown in Figure 4. Note that as the frequency increases, the ESR increases. At low frequencies, the ESR exhibits a linear dependency with frequency, while at higher frequencies the relationship behaves quadratically. The values of ESR extracted at 5 GHz are used in the sensitivity analysis presented in subsection 3.3.

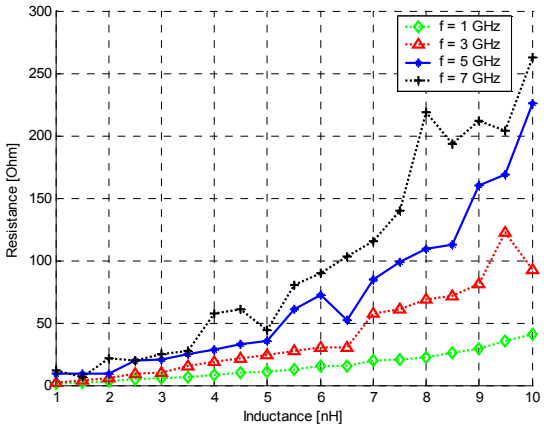

Figure 4. Effective series resistance of spiral inductors

3.3 Sensitivity Analysis

The buffer driving the H-tree sector is modeled as a voltage source with an output resistance. This effective output resistance is modeled as the output resistance in the saturation region, since the NMOS or PMOS transistor of the driver operates in the saturation region during large portions of the switching time. This simple model, however, does not consider the transitions between the linear and saturation regions, nor when both transistors are on and conducting current.

To evaluate the affect of this variation on the resonant H-tree performance, the output resistance is varied over a range of ±25% of the optimal value (25 Ω), as shown in Figure 5. The voltage swing at the leaves and variations in the power dissipation are considered as two performance metrics. The voltage swing is measured with respect to the clock output swing in Figure 3 (1.8 volts) while the variations in power consumption are measured with respect to the optimal power consumption of 15 mW.

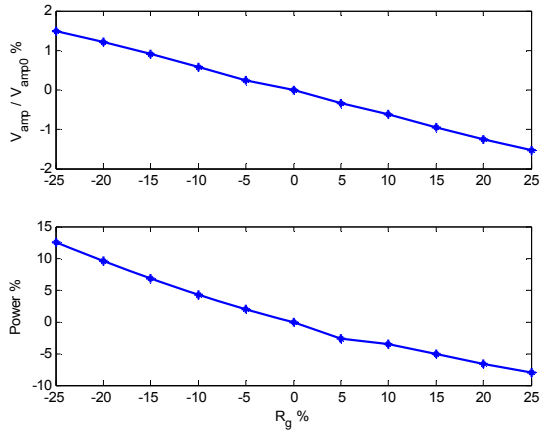

Figure 5. Voltage swing and power consumption as a function of variations in the output resistance

When the output resistance increases, the power consumption decreases. This behavior occurs since the power consumption is inversely proportional to the output resistance of the driving

buffer [11]. Note that the variation of the voltage swing is ±1.25%, even at the extrema of the variations in the output resistance. The model can therefore be used to represent the driving buffer.

To examine the effects of variations in the on-chip inductors and capacitors, consider Figures 6 and 7. Variations in the spiral inductor, assuming a uniform distribution, are shown in Figure 6. Process variations or sharp temperature gradients may alter the spiral wire width, changing the inductance and therefore the parasitic ESR. The change in the inductance may occur since the inductance depends on the specific geometry of the spiral.

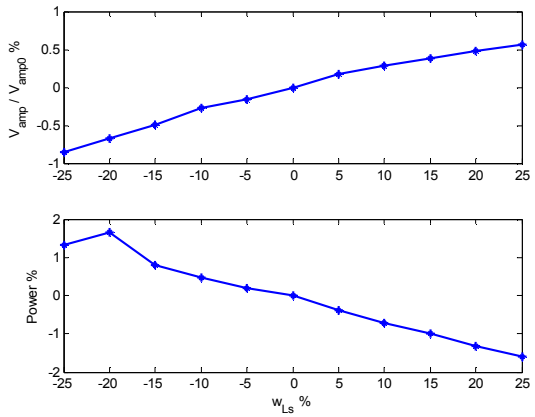

Figure 6. Voltage swing and power consumption as a function of variations in the on-chip inductor width

The inductance and ESR, extracted using Asitic [15], are a function of the variation in spiral width, as shown in Figure 6. For a ±25% change in the wire width, the output voltage swing varies less than ±1%, while the power consumption varies less than ±2%. This behavior indicates that the resonant H-tree is highly tolerant to significant variations in the on-chip spiral inductor and suffers only a minor degradation in performance. Note that the inductance increases as the spiral inductor wire width increases, saving additional energy, as shown in Figure 6.

In modern semiconductor fabrication processes, the on-chip capacitor can vary by up to ±20%. To examine this variation on the behavior of the resonant H-tree, consider Figure 7. The on-chip capacitors are swept over ±25% of the optimal value (15 pF). As observed from Figure 7, the performance of the resonant H-tree is almost insensitive to these changes since the voltage swing varies by less than ±0.15% while the power consumption varies by less than +0.15%. This behavior occurs since the transfer function of the entire network is a weak function of the on-chip capacitors [11]. The main purpose of the on-chip capacitors is to establish a DC voltage around which the clock signal oscillates.

To explore the effect of transmission line variations on the behavior of the H-tree sector, three simulation scenarios are considered. The width of the signal and shielding line, and spacing between the signal and shielding lines are varied. Geometric interconnect variations are important since the physical structure strongly determines the resistance, inductance, and capacitance per unit length. As described by (1), these parameters affect the performance of the resonant H-tree. In the following evaluation, it is assumed that the variations are uniformly distributed along the lines.

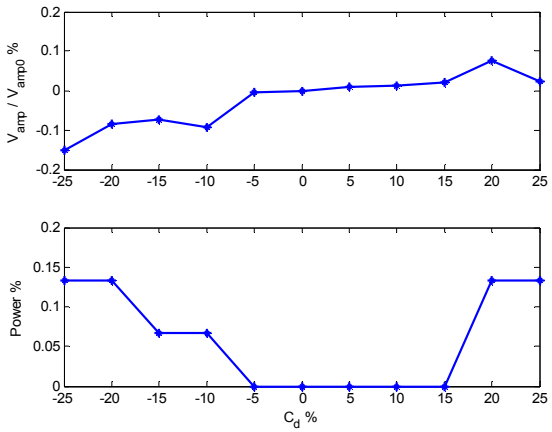

Figure 7. Voltage swing and power consumption as a function of variations of the on-chip capacitor

The impact of the variations of the interconnect width (see Figure 2) on the H-tree performance is illustrated in Figure 8. The H-tree interconnect width is varied by ±10%, exhibiting a voltage swing and power variations of 0 to -0.25% and -0.9% to +0.5%, respectively. Note that the resonant H-tree performance is not significantly affected which implies that in the design of a resonant H-tree sector, the interconnect width is less significant than other parameters. Note also that since the wire resistance is inversely proportional to the wire cross-sectional area, an increase in the interconnect width decreases the resistance, resulting in lower wire losses, thereby decreasing the power dissipation (see Figure 8).

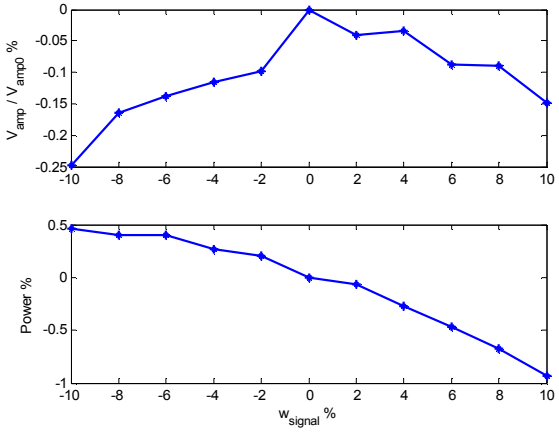

Figure 8. Voltage swing and power consumption as a function of variations in the signal line width

The impact of the variations of the interconnect width on the shield lines is shown in Figure 9. Similar to the signal line variations, the H-tree exhibits a voltage swing and power variations of about 0.1% and -0.6% to +0.8%, respectively. Hence, the performance of the resonant H-tree network is preserved under these variations.

From a power consumption perspective, note that as the shield line width increases, the power dissipation decreases. This behavior occurs since the total capacitance of the structure is proportional to the distance between the signal and the shield

lines, resulting in lower power consumption. The increase in the equivalent capacitance permits more charge to be stored.

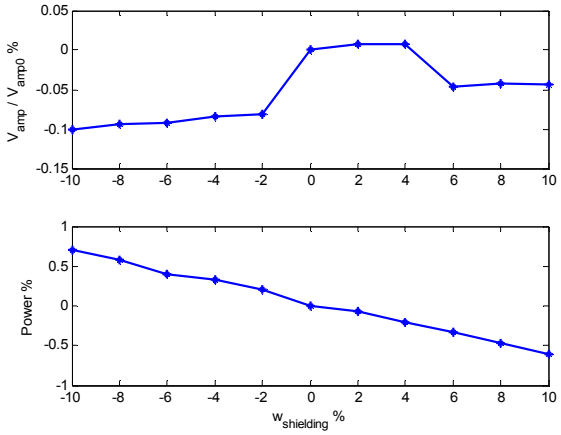

Figure 9. Voltage swing and power consumption as a function of variations in the shield line width

The space between the shield line and the signal line determines the strength of the coupling capacitance, the mutual inductance, and the noise coupled to the signal line (see Figure 10). With spacing variations, the H-tree network exhibits a voltage swing and power variations of about -0.1% to +0.03% and -0.08% to +0.2 %, respectively.

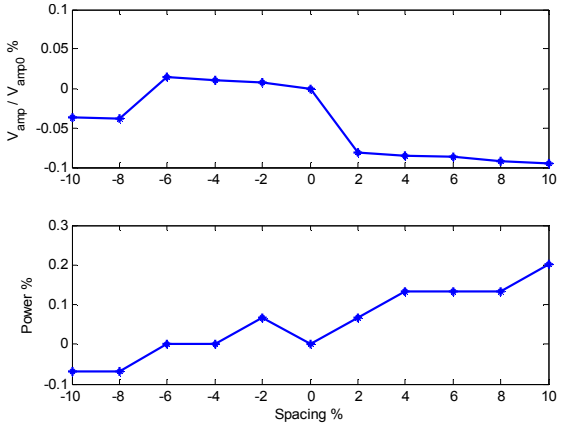

Figure 10. Voltage swing and power consumption as a function of spacing variations between the signal and shield lines

The spacing between the signal and shield lines does not significantly affect the performance of the resonant clock network. The shielding around the H-tree interconnects can therefore be used to target low noise rather than increase the speed of the resonant H-tree network. Note also that as the spacing between the signal and shield lines increases, the capacitance of the structure decreases, resulting in increased power consumption, as depicted in Figure 10. The different design criteria and variation characteristics presented in this subsection are summarized in Table 3.

As predicted by theory and verified by OEA extraction tools, HENRY™ and METAL™, and SpectreS simulations, the following trends are observed. As the width of the signal or shield lines increases, the resistance and inductance decreases while the capacitance increases. As the separation distance between the signal and shield lines increases, the resistance remains constant while the inductance increases and the capacitance decreases.

Table 3. Sensitivity of resonant H-tree structure

Category	Variation range	Voltage swing variations	Power consumption variations
R_g	±25%	-1.5 to 1.5%	-8 to 13%
W_{Ls}	±25%	-0.8 to 0.6%	-1.5 to 1.9%
C_d	±25%	-0.15 to 0.1%	0 to 0.14%
W_{signal}	±10%	-0.25 to 0%	-0.9 to 0.5%
$W_{shielding}$	±10%	-0.1 to 0%	-0.6 to 0.7%
Spacing	±10%	-0.1 to 0.03%	-0.08 to 0.2%

In order to explore the effect of multiple simultaneous variations on the performance of the resonant H-tree, three simulation cases are considered, as shown in Figure 11. The buffer output resistance, on-chip spiral inductors, and capacitors are varied simultaneously with signal (case 1), shield line width (case 2), or spacing (case 3).

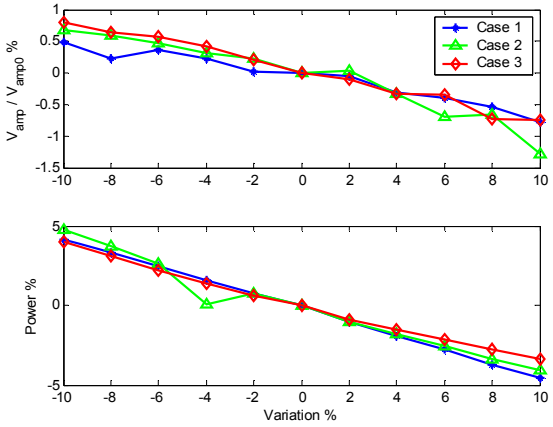

Figure 11. Three cases of voltage swing and power consumption as a function of four simultaneous variations

The H-tree network exhibits the maximum voltage swing and power variations of about ±1.3% and ±5%, respectively (see Figure 11) for all three cases. As expected, the dominant source of deviation (as seen in Figure 5) from the optimal behavior of the resonant H-tree sector is variations in the driving buffer output resistance. The other variation parameters have a much smaller effect on the H-tree performance. The values confirm that a resonant H-tree network is robust and relatively tolerant to process variations.

4. CONCLUSIONS

Resonant H-tree clock distribution networks may be a suitable alternative to traditional clock distribution networks. As shown in [11], a significant decrease in power consumption can be achieved as compared to standard H-tree networks. This paper explores the sensitivity of a resonant H-tree sector to six different design criteria: variations in buffer output resistance, on-chip inductor and capacitor size, and signal and shield line width and spacing. Simulations demonstrate that the resonant H-tree sector exhibits acceptable robustness and relatively low sensitivity to process and

environmental variations for a 5 GHz operating frequency. The maximum voltage swing and power consumption observed in simulations are +1.5% and +13%, respectively. These variations occur when the driving buffer output resistance varies by 25%. For the remaining parameters, the resonant H-tree sector exhibits insignificant variations as compared to the optimal performance with no variations. Simultaneous process variations demonstrate that resonant clock networks are highly tolerant and robust.

5. REFERENCES

[1] S. Borkar *et al.*, "Parameter Variations and Impacts on Circuits and Microarchitecture," *Proceedings of the IEEE/ACM Conference on Design Automation*, pp. 338-342, June 2003.

[2] D. Velenis, R. Sundaresha, and E. G. Friedman, "Buffer Sizing for Delay Uncertainty Induced by Process Variations," *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems*, pp. 415-418, December 2004.

[3] W. Dai and H. Ji, "Timing Analysis Taking into Account Interconnect Process Variations," *Proceedings of the IEEE International Workshop on Statistical Methodology*, pp. 51-53, June 2001.

[4] A. Teene, *et al.*, "Impact of Interconnect Process Variations on Memory Performance and Design," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 694-699, March 2005

[5] K. A. Bowman, S. G. Duvall, and J. D. Meindl, "Impact of Die-to-Die and Within-Die Parameter Fluctuations on the Maximum Clock Frequency Distribution," *IEEE Journal of Solid-State Circuits*, Vol. 37, No. 2, pp. 183-190, February 2002.

[6] V. L. Chi, "Salphasic Distribution of Clock Signals for Synchronous Systems," *IEEE Transaction on Computers*, Vol. 43, No. 5, pp. 597-602, May 1994.

[7] F. O. Mahony, C. P. Yue, M. A. Horowitz, and S. S. Wong, "A 10-GHz Global Clock Distribution Using Coupled Standing-Wave Oscillators," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 11, pp. 1813-1820, November 2003.

[8] J. Wood, T. C. Edwards, and S. Lipa, "Rotary Traveling-Wave Oscillator Arrays: A New Clock Technology," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 11, pp. 1654-1665, November 2001.

[9] S. C. Chan, K. L. Shepard, and P. J. Restle, "Design of Resonant Global Clock Distributions," *Proceedings of the IEEE International Conference on Computer Design*, pp. 248-253, October 2003.

[10] S. C. Chan, K. L. Shepard, and P. J. Restle, "Uniform-phase, Uniform-amplitude, Resonant-Load Global Clock Distributions," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 1, pp. 102-109, January 2005.

[11] J. Rosenfeld and E. G. Friedman, "Design Methodology for Global Resonant H-Tree Clock Distribution Networks," *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2006

[12] http://www.oea.com

[13] L. Sun, J. Wen, J. Yan, and J. Hu, "Modeling and Parameters Extraction of Spiral Inductors for Silicon-Based RFICs," *Proceedings of the IEEE International Conference on Solid-State and Integrated Circuits Technology*, Vol. 1, No. 1, pp. 224-227, October 2004

[14] M. Niknejad and R. G. Meyer, "Analysis Design and Optimization of Spiral Inductors and Transformers for Si RF ICs," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 10, pp. 1470-1481, October 1998

[15] http://rfic.eecs.berkley.edu/~niknejad/asitic.html