Design Challenges in High Performance Three-Dimensional Circuits

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Abstract

The initial focus of the presentation will be on reviewing the fundamental trends specific to 3-D circuits and systems, including the many opportunities and challenges of this exciting new technology. A short review of the MIT Lincoln Laboratories 3-D manufacturing technology will follow. A summary of some primary issues in the physical design of 3-D systems will be reviewed. This discussion will be followed by a review of current research in the area of on-chip 3-D computer network topologies; specifically, 3-D networks-on-chip. A discussion of the so-called Rochester Cube will then be presented in the context of its relative impact and importance. Circuit design issues will be discussed and experimental results will be reviewed. The presentation will conclude with a review of some near-term and long term research problems in 3-D systems.

Categories & Subject Descriptors: B.7 INTEGRATED CIRCUITS, B.7.1 Types and Design Styles, Advanced technologies, Algorithms implemented in hardware, Microprocessors and microcomputers, VLSI (very large scale integration)

General Terms: Performance, Design, Reliability

Bio

Eby G. Friedman received the B.S. degree from Lafayette College in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering. From 1979 to 1991, he was with Hughes Aircraft Company. He has been with the Department of Electrical and Computer Engineering at the University of Rochester since 1991, where he is a Distinguished Professor, and the Director of the High Performance VLSI/IC Design and Analysis Laboratory. He is also a Visiting Professor at the Technion - Israel Institute of Technology. His current research and teaching interests are in high performance synchronous digital and mixed-signal microelectronic circuit design. He is the author of more than 325 papers and book chapters, several patents, and the author or editor of ten books in the fields of high speed and low power CMOS design techniques, high speed interconnect, and the theory and application of synchronous clock and power distribution networks. He previously was the Editor-in-Chief of the *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, and a recipient of the University of Rochester Graduate Teaching Award, and a College of Engineering Teaching Excellence Award. Dr. Friedman is a Senior Fulbright Fellow and an IEEE Fellow.

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