Simultaneous Shield and Repeater Insertion

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ABSTRACT

Resource based optimization for high performance integrated circuits is presented. The methodology is applied to simultaneous shield and repeater insertion, resulting in minimum coupling noise under power, delay, and area constraints. Design expressions exhibiting parabolic noise behavior are compared with SPICE simulations. Due to the parabolic coupled noise behavior, the minimum noise is established. Good agreement between the analytic results and SPICE simulations is shown.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]: Miscellaneous—*Interconnects, resources*

General Terms

Design

Keywords

Interconnects, area, delay, noise, power

1. INTRODUCTION

Further increases in integrated circuit (IC) scaling requires more efficient devices, circuits, and systems in terms of power, delay, noise, and area. Efficient optimization processes are therefore required. To achieve this capability, many different design techniques are used. In many cases, only one technique is implemented; however, two or more techniques applied simultaneously may provide higher performance. A methodology that considers multiple design objectives while satisfying system requirements typically utilizes lower resources. Optimization processes and related design techniques applied to high performance ICs are the topic of this paper.

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A standard optimization process is based on a *cost* function. There are two steps involved in this process, building a function and determining the optimal value of the function. The *cost* function is typically a sum of coefficients multiplied by the resources or a product of resources with power coefficients, such as

$$cost = \alpha_1 \cdot power + \alpha_2 \cdot delay + \alpha_3 \cdot noise + \alpha_4 \cdot area, \quad (1)$$

$$cost = power^{\beta_1} \cdot delay^{\beta_2} \cdot noise^{\beta_3} \cdot area^{\beta_4}, \quad (2)$$

where α and β characterize the importance of a particular resource. In [1], the function with $\beta_1 = \beta_2 = 1$ and $\beta_3 = \beta_4 = 0$, referred to as a power-delay product, is used to optimize a system of tapered buffers. While normalization is required for the resources in (1), (2) is more complicated. The primary disadvantage of a standard optimization process is the requirement to select the values of α and β prior to the optimization process.

IC development can be functionally separated into two major layers, the design layer and the support layer. The design layer includes the architecture, circuit, and interconnect. The power supply system, clock distribution network, and substrate are related to the support layer. In the literature, a number of local optimization techniques have been published for each separate group of layers. For interconnect, low swing interconnects [2], cascaded buffers [3], repeater insertion [4], shielding [5], differential signaling [6], active regeneration [7], intentional skewing [8], bus swizzling [9], and tapered interconnects [10] are well known design techniques. Each technique trades off power, delay, noise, and area differently. Delay, bandwidth, and power for *RC* and *RLC* interconnects have been investigated in [11]; however, only one design technique, repeater insertion, is used. By combining some of these techniques, more efficient results may be achieved. In [12], two methods, shield and repeater insertion, have been combined to reduce noise within a standard optimization process.

In this paper, a general resource based optimization process is presented. Any design constraint may be characterized as a resource. Some constraints, such as power and area, are more commonly treated as a resource. Other design objectives, such as delay or noise, are less commonly referred to as a resource. A practical application is composed of a combination of optimization processes and multiple design techniques. A methodology that considers these issues in an integrated fashion is the focus of this paper. Two different techniques that provide immunity to coupled noise, shield and repeater insertion, have been combined based on resource optimization to exemplify this process. Each of the techniques exhibits different power, delay, noise, and area resource characteristics.

The paper is organized as follows. Limitations to the standard optimization process that motivates resource based optimization processes are described in Section 2. This process is simultane-

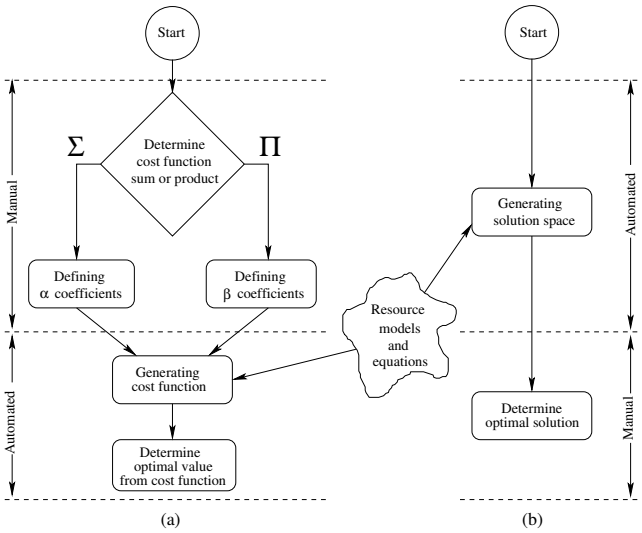

Figure 1: Optimization flow diagram, (a) standard and (b) resource based optimization process.

ously applied to shield and repeater insertion in Section 3. A practical design case is presented in Section 4. In this section, the parabolic noise behavior is also described. Finally, the paper is concluded in Section 5.

2. RESOURCE BASED OPTIMIZATION

Limitations in standard optimization processes are described in subsection 2.1. The theory and limitations of resource based optimization processes are presented in subsection 2.2 and 2.3, respectively. Different design techniques are introduced in subsection 2.4.

2.1 Limitations in standard optimization processes

A general flow for a standard optimization process is shown in Fig. 1(a). The primary disadvantage of this flow is the need for user involvement before the optimization process is initiated. The *cost* function and coefficients must be allocated for each resource. For the same system, two users may choose different coefficients and thereby produce different results. Additionally, some resources have changing importance. These aspects constrain the standard optimization process.

2.2 Resource based optimization processes

To overcome these limitations, a different resource based optimization process is proposed. The user involvement occurs at the end of this process. In Fig. 1(b), a flow diagram of this resource based optimization process is presented. Any system can be represented by n variables and $n+1$ resources,

$$\left.\begin{array}{rcl} res_1 &=& f_1(a_1,a_2,a_3,\ldots,a_n) \\ res_2 &=& f_2(a_1,a_2,a_3,\ldots,a_n) \\ &\vdots& \\ res_n &=& f_n(a_1,a_2,a_3,\ldots,a_n) \\ res_{n+1} &=& f_{n+1}(a_1,a_2,a_3,\ldots,a_n) \end{array}\right\}, \quad (3)$$

where $res_1, res_2, \ldots, res_{n+1}$ are the resources, such as power, delay, noise, and area, and $a_1, a_2, \ldots, a_n$ are variables, such as the line width, shield width, and length. Inverting the first n equations in (3),

$$\left.\begin{array}{rcl} a_1 &=& g_1(res_1,res_2,\ldots,res_n) \\ a_2 &=& g_2(res_1,res_2,\ldots,res_n) \\ &\vdots& \\ a_n &=& g_n(res_1,res_2,\ldots,res_n) \\ res_{n+1} &=& f_{n+1}(a_1,a_2,a_3,\ldots,a_n) \end{array}\right\}. \quad (4)$$

To exemplify this process, if n equations in (3) are invertible, (4) describes the same system. The first n equations in (4) are substituted into the last equation in (4), resulting in

$$\begin{aligned} res_{n+1} = f_1[\ & g_1(res_1,res_2,\ldots,res_n), \\ & g_2(res_1,res_2,\ldots,res_n), \\ & \ldots, \\ & g_n(res_1,res_2,\ldots,res_n)]. \end{aligned} \quad (5)$$

Representing the system by (5), the interaction is among the resources and not among the design variables. The function described in (5) represents a solution space. The behavior of each resource among the other resources is referred to here as a tradeoff surface.

2.3 Limitations in resource base optimization processes

Resource based optimization also exhibits limitations. These limitations can be categorized as

- Model inaccuracies
- Function inversability

In a standard optimization process, inaccuracy in the models produces quantization error. In resource based optimization, however, this error is cumulative. Due to these additive errors, the models used in this optimization process must be sufficiently accurate. Otherwise, only the fidelity of the final function may be useful.

Function inversability is a different limitation in resource based optimization processes. For $y = f(x)$ where x can not be directly extracted, certain techniques are required to provide inversability. Some of these techniques are truncation, Taylor expansion, and approximation, which can lead to greater model inaccuracy.

2.4 Local Optimization Techniques

Several techniques have been proposed in the literature to overcome interconnect noise, such as shielding, repeater insertion, differential signaling, active regeneration, intentional skewing, and bus swizzling. Each of these techniques protect the interconnect from coupled noise in a different way and require different resources. The following section focuses on two commonly used techniques, shield and repeater insertion.

3. SHIELD AND REPEATER INSERTION

Placing a shield beside and inserting repeaters along a victim line are chosen to exemplify the resource based optimization process. The width of the shield line, and the number and size of the repeaters are chosen to express noise on the victim line as a function of power, area, and delay resources. Repeater insertion, shielding, and the basic resource expressions are summarized in the following section. As compared to [12] where a *cost* function is used, this work is based on resource optimization. In [12], the noise is modeled based on the Devgan metric [13], while in this paper the shielded noise model is based on [14].

3.1 Repeater Insertion

Repeater insertion is a well known design technique to reduce the delay required to propagate a signal along a line [4]. The objective is to divide the interconnect into smaller sections, reducing the quadratic delay dependency on length to a linear dependency, thereby reducing the overall delay [15]. If the number of repeaters is too small, the delay due to the interconnect will dominant. If the number of repeaters is too large, the repeater delay dominates. The optimal number of repeaters that minimizes the overall delay has been presented in [4], [11], and [15].

An additional advantage of repeater insertion is reducing the coupled noise from adjacent interconnects. It is impractical, however, to insert excessive repeaters due to delay, power and area constraints.

3.2 Shielding

Shielding inserts an additional line between a victim line and an aggressor line. A shield line is connected to the power/ground network, filtering the noise from the aggressor away from the victim line. The technique is highly effective, although significant area is required.

3.3 Resources

Four primary resources for simultaneous shield and repeater insertion are considered: power, delay, noise, and area. In this paper, the resource models are based on a 0.18 μm CMOS technology.

3.3.1 Power

Two primary power dissipation sources are considered. The first source, dynamic power, is used to charge and discharge the interconnect and transistor capacitances. The second source, short-circuit power, also occurs when the transistors switch. During the switching time, the current from the power to ground network passes through the NMOS and PMOS transistors. This power component is typically in the range of 5% to 10% of the overall transient power. The total transient power is the summation of the dynamic and short-circuit power,

$$power = power_{dyn} + power_{sc} = f_1(h,k), \tag{6}$$

where k and h are, respectively, the number of inserted repeaters along the victim line and the ratio between the final and minimum transistor widths.

3.3.2 Delay

Minimizing the overall interconnect delay in a repeater system has been investigated in [4]. In [15], a more accurate delay expression is presented based on the saturation velocity characteristic,

$$delay = f_2(h,k). \tag{7}$$

3.3.3 Noise

Noise modeling in shielded interconnect has been investigated in [5], [14]. From the shield model used in [14], the noise as a function of the shield line width can be expressed as

$$noise_{sh} = f_{sh}(w_{sh}), \tag{8}$$

where w_{sh} is the width of the shield line. Repeater insertion divides the overall length of the line into smaller sections. Assuming a uniform distribution of the noise along the victim line, the total noise of the line is

$$noise_{rep} = \frac{1}{k}, \tag{9}$$

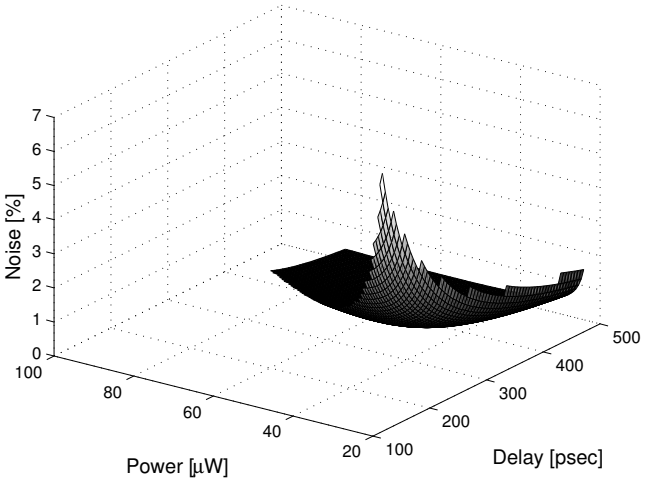

Figure 2: Noise as a function of power and delay in a system with shields and repeaters.

dividing the noise by the number of inserted repeaters. The total effect of inserting a shield line and repeaters is expressed as a product,

$$noise = noise_{sh} \cdot noise_{rep} = f_{sh}(w_{sh})\frac{1}{k} = f_3(w_{sh},k). \tag{10}$$

3.3.4 Area

The width ratio between the PMOS and NMOS transistors is taken to be three. The PMOS transistor is designed in a stack structure to reduce the overall width. The area of the shield and repeater is

$$area = f_4(w_{sh},h). \tag{11}$$

3.4 Coupling Noise with Resource Based Optimization

The resource models are expressed in (6), (7), (10), and (11). The power, delay, and area equations are inverted and substituted into the noise expression,

$$noise = f_5(area, power, delay), \tag{12}$$

where the noise is a function of resources such as the area, power, and delay. The complete form of the analytic expression is presented in [16]. Note that the noise is not a function of the number or size of the repeaters or the width of the shield line.

4. SIMULATION RESULTS

A case study with inserted repeaters and a shielded victim line is considered. The area, power, delay, and noise are evaluated for this system. Several physical parameters are chosen to reflect practical design characteristics. Specifically, $s = 0.5$ μm, $length = 1$ mm, $v_{dd} = 1.8$ volts, $v_{ss} = 0$ volts, $v_t = 0.5$ volts, $l_t = 0.18$ μm, and $w_{line} = 2$ μm, representing the spacing between the victim and aggressor lines, length of the structure, power, ground, and threshold voltages, transistor length, and width of the victim line, respectively. By increasing the area, the noise is reduced since wider shield lines and additional repeaters are possible. The noise monotonically decreases as a function of area; therefore, the area is set to a value of 4.15 nm^2, a practical design value.

A graph presenting *noise* as a function of *power* and *delay* is illustrated in Fig. 2. Note the relationship among power, delay, and

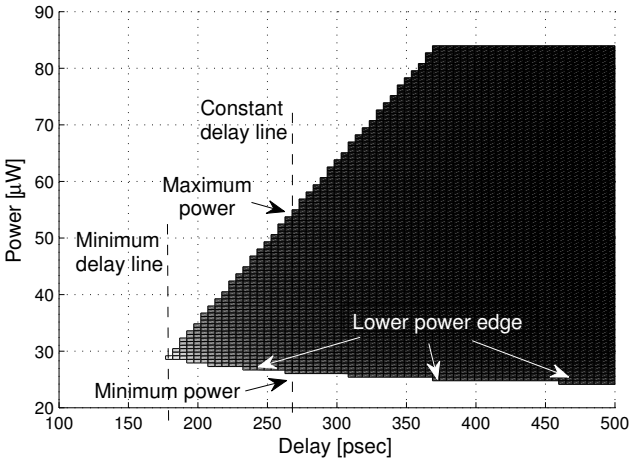

Figure 3: Top view of Fig. 2. The lighter color represents a larger amount of noise.

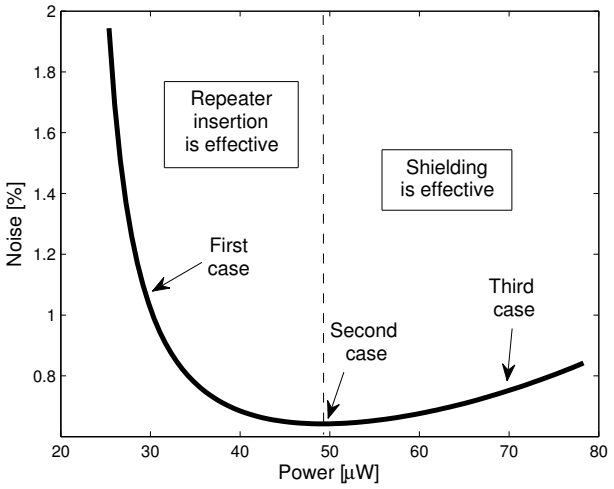

Figure 4: Noise as a function of power at the maximum allowed delay (350 psec) and area (4.15 nm^2).

noise, generating a tradeoff surface, permitting different tradeoffs to be made. The top view of the graph illustrated in Fig. 2 is shown in Fig. 3, where the lighter region indicates a higher noise. For this design case, a 180 psec delay is the minimum delay, as depicted in Fig. 3. This delay is not the same as determined in [4], [11] and [15], since power, noise, and area are also considered. The lower edge of the power curve, illustrated in Fig. 3, saturates to a minimum power level. This curve does not reach zero due to the minimum power required to charge and discharge the line capacitance.

Noise as a function of power at the maximum allowed delay and area is illustrated in Fig. 4. The graph consists of two different regions. The noise is reduced by increasing the power and the noise increases at a higher power. This parabolic noise behavior can be exploited to determine the minimum noise for this circuit. To motivate these results, three cases, depicted in Fig. 4, have been evaluated. The first case, at a power of 29 μW, produces a 1.1% noise (normalized to V_{dd}). The noise voltage in this case is 21 mV. The noise for the second case located at a power of 49 μW is 0.65% (or 11.5 mV). The final case at a power of 70 μW produces 0.8% (or

Table 1: Three design cases shown in Fig. 4 evaluated in SPICE

Case number	k (number of repeaters)	$h\cdot$ 0.5 (width of the repeaters)	w_{sh} (width of the shield line)
First	2	0.8 μm	0.8 μm
Second	6	1.2 μm	0.5 μm
Third	8	1.5 μm	0.1 μm

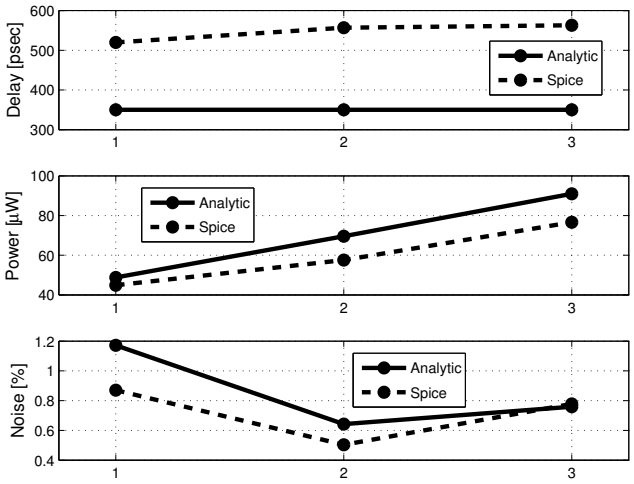

Figure 5: Delay, power, and noise for three different design cases. Analytic and SPICE results are compared.

14 mV) noise. The 20 mV noise difference between the first and second case exemplifies the tradeoff. The noise difference between the second and third case is smaller, but significant. The area and delay are maintained at maximum values. With an increase in the power, the number and width of the repeaters increase at a different rate, maintaining a constant delay. Simultaneously, the width of the shield lines decreases, providing more space for larger repeaters while maintaining the area constant. The larger number of repeaters reduces the noise; however, the reduction in the shield width increases the noise. Adding repeaters at lower power levels reduces the noise more than adding repeaters at higher power levels. Therefore, at lower power, the reduction in noise due to the repeaters is greater. Hence, at lower power levels, the most efficient noise reduction technique is repeaters, while at higher power levels, the most efficient noise reduction technique is shield lines, as illustrated in Fig. 4. Both of these techniques reduce the noise, exhibiting a parabolic noise behavior, allowing the minimum noise design to be determined. In this case, the minimum noise is 49 μW total power and contributes only 0.65% (or 11.5 mV) noise.

This concept is evaluated on a system composed of a victim interconnect with several repeaters and a shield line. Three design cases, listed in Table I, are considered. The power, delay, and noise are determined from SPICE simulations. The analytic model and SPICE results are compared in Fig. 5 and Table II for three design cases, listed in Table I and depicted in Fig 4. In Table II, the change in delay, power, and noise is determined relative to the minimum noise design case (second case). In the analytic model, the delay is maintained constant; however, small changes in the delay are noted from SPICE. The error between the analytic model and SPICE among the three design cases is due to inaccuracies in the delay model. The power resulting from the analytic model and SPICE

Table 2: Analytic and SPICE results for the three design cases from Table I and Fig. 4

		k	h	w_{sh}	Delay [psec]	Change in Delay [%]	Power [μW]	Change in Power [%]	Noise [mV]	Change in Noise [%]
Analytic	First case	2.04	1.63	0.83	350	0.0	28.9	41.1	21.1	82.5
	Second case	5.91	2.33	0.48	350		49.0		11.6	
	Third case	8.04	3.04	0.13	350	0.0	69.6	42.1	13.7	18.2
SPICE	First case	2	1.63	0.83	520	6.6	44.9	22.0	15.7	73.0
	Second case	6	2.33	0.48	557		57.6		9.1	
	Third case	8	3.04	0.13	563	1.1	76.6	33.1	14.0	54.5

is similar. The noise evaluated from SPICE also exhibits good agreement with the analytic model. The SPICE results demonstrate the same parabolic noise behavior when simultaneously applying shield and repeater insertion. The noise is lower in the second design case than the first and third design cases, confirming the parabolic noise behavior. The minimum noise is achieved with simultaneous shield and repeater insertion, while satisfying power, area, and delay constraints.

5. CONCLUSIONS

Resource based optimization is described and compared in this paper to standard optimization processes. The resource based optimization process is evaluated for a system that simultaneously considers shield and repeater insertion. The methodology is used to investigate area, power, delay, and noise tradeoffs. Coupled noise as a function of power with maximum allowed delay and area is evaluated, demonstrating a parabolic behavior. This approach permits the minimum noise design to be determined. The analytic model exhibits good agreement with SPICE. Over 50% reduction in coupled noise is demonstrated as compared to three design cases by applying this resource based optimization process.

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