Methodology to Achieve Higher Tolerance to Delay Variations in Synchronous Circuits

Emre Salman and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627 USA
[salman,friedman]@ece.rochester.edu

ABSTRACT

A methodology is proposed for designing robust circuits exhibiting higher tolerance to process and environmental variations. This higher tolerance is achieved by exploiting the interdependence between the setup and hold times, reducing the delay uncertainty caused by variations. An algorithm is proposed to determine the interdependent setup-hold pair of a register. A data path designed with the proposed setup-hold pair improves the overall tolerance to variations. The methodology is evaluated for several technologies to determine the overall reduction in delay uncertainty.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]:

General Terms

Algorithms, design

1. INTRODUCTION

Process and environmental variations are a primary concern for deeply scaled CMOS technologies [1]. The accurate control of the channel length, gate oxide thickness, and channel doping concentration significantly challenges the miniaturization process, producing on-chip process variations [2]. Similarly, fluctuations in temperature and power supply voltage are primary sources of environmental variations [3].

Process and environmental variations affect the timing characteristics of a circuit by producing additional delay uncertainty [4]. The delay of a long critical path can increase due to variations, decreasing the maximum operating frequency [2]. These variations can also cause a circuit failure by decreasing the delay of a short path, resulting in a race condition [4].

Two primary approaches exist to alleviate the effect of variations. The first category involves those techniques that improve the manufacturing process while the second category targets design methodologies that produce a robust circuit tolerant to variations [2]. The first category is difficult to achieve since the device and interconnect geometries are smaller with each technology. A design methodology is proposed in this paper that produces a more robust circuit by exploiting the interdependence between the setup and hold times.

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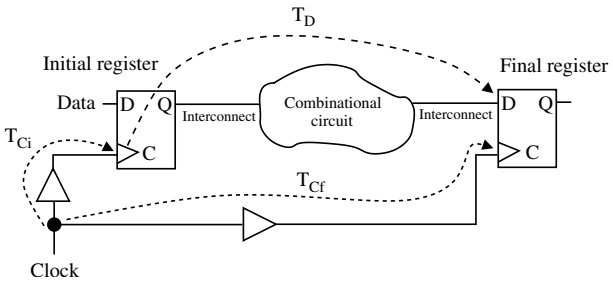


Figure 1: Simple synchronous circuit consisting of a combinational logic and two registers.

Specifically, the significance of interdependence in reducing *delay uncertainty* is demonstrated herein as opposed to previous works where the primary focus is on exploiting this interdependence in static timing analysis [5–7] and the efficient characterization of the interdependence [8]. The evolution of interdependence with process technology is also investigated in this paper to investigate the effect of scaling on these interdependent timing constraints.

The rest of the paper is organized as follows. Background material is provided in Section 2. The problem is formulated in Section 3. A methodology to reduce delay uncertainty and compensate for variations is described in Section 4. A case study is presented in Section 5 to evaluate the significance of setup-hold interdependence. Finally, the paper is concluded in Section 6.

2. BACKGROUND

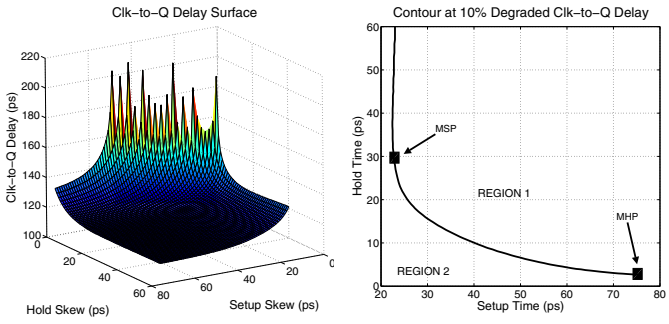
The timing characteristics of synchronous circuits are reviewed in Section 2.1. Interdependent setup-hold times are described in Section 2.2.

2.1 Timing Characteristics of Synchronous Circuits

A simple synchronous digital circuit consisting of two sequentially-adjacent registers with a combinational circuit between these registers is shown in Fig. 1. Two inequalities should be satisfied for this circuit to function properly. Referring to Fig. 1, the first inequality is

$$T_{Cf} + T_{CP} \geq T_{Ci} + T_D + T_S, \tag{1}$$

where T_{Ci} and T_{Cf} are the delay for the clock signals to arrive, respectively, at the *initial* and *final* registers. Note that T_{Ci} and T_{Cf} are also referred to, respectively, as the delay of the clock launch path and clock capture path. T_{CP} is the clock period, T_D is the data path delay consisting of the clock-to-Q delay of the initial register, logic delay of the combinational circuit, and the interconnect delay. T_S is the setup time of the final register. Note that (1) determines the maximum speed of the circuit, making this inequality important for the critical paths within a circuit.



(a) (b)

Figure 2: Interdependent setup-hold time characterization: (a) CLK-to-Q delay surface as a function of independently varying setup skew and hold skew, (b) The contour at 10% degraded CLK-to-Q delay.

The second inequality that needs to be satisfied is

$$T_{Ci} + T_D \geq T_{Cf} + T_H, \tag{2}$$

where T_H is the hold time of the final register. This inequality guarantees that no race condition exists, *i.e.*, the data is not latched within the final register during the same clock edge. Note that (2) is relatively more important for those timing paths where the data path delay is sufficiently small, such as a shift register or counter.

2.2 Interdependent Setup-Hold Times

Existing approaches to characterize the timing constraints of a register, *i.e.*, setup and hold times in (1) and (2), assume these timing constraints are independent [9]. This independent characterization produces overly pessimistic results since the setup-hold times are, in reality, interdependent [5]. An example of an interdependent setup-hold contour curve obtained from a clock-to-Q delay surface at a constant delay is illustrated in Fig. 2 [6]. In Fig. 2(a), the CLK-to-Q delay is obtained as a function of independently varying setup skew and hold skews. Those setup and hold skews corresponding to a specific per cent degradation in CLK-to-Q delay are extracted from this surface, representing a contour curve. Each (setup, hold) pair on this contour curve shown in Fig. 2(b) is a valid pair for the register. Multiple timing constraints therefore exist rather than a single setup and hold time. As indicated in Fig. 2(b), a small setup time can be obtained at the expense of a large hold time. Similarly, a small hold time can be obtained at the expense of a large setup time. For example, *minimum setup pair* (*MSP*) and *minimum hold pair* (*MHP*) refer, respectively, to a pair on the contour with the minimum setup time and minimum hold time. Also note that any pair in region 1 is also valid with additional pessimism, whereas any pair in region 2 is invalid, as the pairs in this region are optimistic.

A methodology to interdependently characterize setup-hold times and exploit this interdependence in static timing analysis has been described [5]. The computational efficiency of interdependent setup-hold time characterization has been improved through state transition equations [8]. Interdependent setup-hold times have also been exploited in statistical static timing analysis processes [7].

Interdependent setup-hold times not only reduce pessimism in timing analysis, but also provide an opportunity to improve the tolerance of a circuit to process and environmental variations. The significance of interdependence is demonstrated in this paper for deeply scaled technologies. A methodology is proposed to reduce the delay uncertainty caused by process and environmental variations.

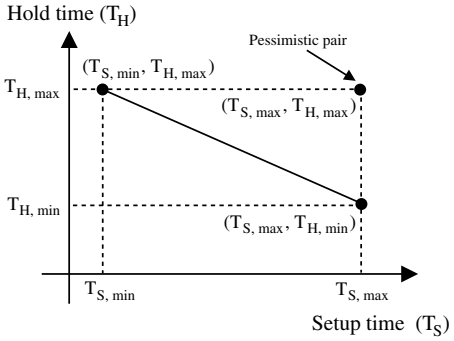


Figure 3: Linear approximation of the contour curve using two pairs: ($T_{S,min}$, $T_{H,max}$) and ($T_{S,max}$, $T_{H,min}$).

3. PROBLEM FORMULATION

The contour curve illustrated in Fig. 2(b) can be approximated as a linear line using two critical pairs: *MSP* and *MHP*. Note that this approximation is valid since any point above the curve, *i.e.*, in region 1, is a valid pair with some pessimism. An approximation of the contour using two critical pairs is illustrated in Fig. 3 where the pairs *MSP* and *MHP* are represented, respectively, as ($T_{S,min}$, $T_{H,max}$) and ($T_{S,max}$, $T_{H,min}$).

According to (1) and (2), at a specific clock period, the delay of the data path T_D is dependent upon both the setup and hold times. Referring to Fig. 1, the delay of the data path should satisfy

$$T_{Cf} + T_H - T_{Ci} \leq T_D, \tag{3}$$

$$T_D \leq T_{Cf} + T_{CP} - (T_{Ci} + T_S), \tag{4}$$

where (3) and (4) determine, respectively, the lower and upper bounds of the data path delay.

The allowable range of T_D is minimized if the pessimistic pair ($T_{S,max}$, $T_{H,max}$) is used, causing the circuit to be overdesigned. Which specific (setup, hold) pair should be chosen to design the circuit is unclear even if the interdependence is known since multiple valid pairs are available. For example, if the pair ($T_{S,min}$, $T_{H,max}$) is used, the lower bound constraint of the data path delay is difficult to satisfy since the hold time is large. Hence, the data path delay should be increased by inserting additional stages, dissipating unnecessary power. Alternatively, if the pair ($T_{S,max}$, $T_{H,min}$) is used, the upper bound constraint on the data path delay is difficult to satisfy since the setup time is large. Consequently, the data path delay should be lowered by inserting an additional register to satisfy the target frequency, also causing unnecessary power consumption. Furthermore, both pairs ($T_{S,min}$, $T_{H,max}$) and ($T_{S,max}$, $T_{H,min}$) exhibit low tolerance to process and environmental variations since the range of valid setup times $T_{S,max} - T_{S,min}$ and hold times $T_{H,max} - T_{H,min}$ is not exploited.

It is therefore important to determine the appropriate (setup time, hold time) pair during the design process that lowers power consumption, satisfies the required delay, and increases the robustness of the circuit to achieve a higher tolerance to process and environmental variations. A methodology is described in this paper to determine the appropriate (setup, hold) pair during the design process that improves the tolerance of a circuit to variations while increasing the maximum operating frequency. The interdependence is also evaluated for several advanced technologies, demonstrating the increasing significance of this interdependence in deeply scaled technologies.

Note that interdependence has previously been exploited in static timing analysis [5–7]. A disadvantage of considering only the analysis phase is the inability to accurately evaluate the significance of

interdependence. Specifically, the results presented in [5] and [6] strongly depend upon the specific circuit and the target clock frequency. For example, while interdependence can significantly reduce timing violations in one circuit, interdependence may not be as efficient in another circuit with the same technology, producing inconsistent results. A more comprehensive methodology is proposed in this paper that considers this interdependence during the *design* phase. The ability of this interdependence to tolerate variations is investigated, providing a more complete understanding of the significance of interdependence, specifically in deeply scaled technologies.

4. REDUCING DELAY UNCERTAINTY

An efficient technique to obtain the interdependent setup-hold time characteristics is explained in Section 4.1. A procedure to reduce delay uncertainty and compensate for variations is described in Section 4.2. The amount of compensation achieved by the proposed methodology is determined in Section 4.3.

4.1 Obtaining Linear T_S vs. T_H Relationship

The first step to reduce delay uncertainty is to obtain the linear T_S vs. T_H relationship for a register. Two critical pairs, *MSP* and *MHP*, should be identified to define this line, as illustrated in Fig. 3. Generation of the CLK-to-Q delay surface to obtain these critical pairs is inefficient since a large number of simulations is required. An alternative procedure is proposed to obtain *MSP* and *MHP* without generating the CLK-to-Q delay surface. Referring to Fig. 3, the four points defining *MSP* and *MHP*, *i.e.*, $T_{S,min}$, $T_{H,max}$, $T_{H,min}$, and $T_{S,max}$, are obtained as follows:

$T_{S,min}$: The CLK-to-Q delay of a register is determined as a function of setup skew at a sufficiently high hold skew. The setup skew corresponding to a 10% degradation in delay represents $T_{S,min}$.

$T_{H,max}$: The CLK-to-Q delay of a register is determined as a function of hold skew at $setup\ skew = T_{S,min}$. The hold skew corresponding to a 10% degradation in delay represents $T_{H,max}$.

$T_{H,min}$: The CLK-to-Q delay of a register is determined as a function of hold skew at a sufficiently high setup skew. The hold skew corresponding to a 10% degradation in delay represents $T_{H,min}$.

$T_{S,max}$: The CLK-to-Q delay of a register is determined as a function of setup skew at $hold\ skew = T_{H,min}$. The setup skew corresponding to a 10% degradation in delay represents $T_{S,max}$.

Note that the critical pairs are obtained with significantly fewer simulations using this technique as compared to generating the complete CLK-to-Q delay surface. The linear relationship can be represented by the critical pairs as $T_H = f(T_S)$ or, equivalently, $T_S = f^{-1}(T_H)$. Note that $T_{S,r} = T_{S,max} - T_{S,min}$ represents the range of valid setup times while $T_{H,r} = T_{H,max} - T_{H,min}$ represents the range of valid hold times. The inverse proportionality and this range of valid setup/hold times can be exploited to reduce delay uncertainty, as described in the following subsection.

4.2 Procedure to Reduce Delay Uncertainty

For a critical path, an increase in the delay of a data path ΔT_D due to variations causes the frequency to be decreased to satisfy (4). This increase in the data path delay produces additional slack in (3), *i.e.*, hold skew. This additional slack in the hold skew can be exploited to increase the hold time in (3) by ΔT_{Hold} where $\Delta T_{Hold} = \Delta T_D$. An increase in the hold time enables a decrease in the setup time by $\Delta T_S = f^{-1}(\Delta T_H)$ due to the interdependence, as illustrated in Fig 3. The effect of the variation, *i.e.*, the decrease in frequency, can therefore be compensated by exploiting a lower setup time.

Similarly, for a timing path sensitive to a race condition, referred to as a *short path*, a decrease in the delay of the data path by ΔT_D can cause a hold time violation. Since the delay of the data path is reduced, any additional slack in (4), *i.e.*, setup skew, can be exploited by increasing the setup time by ΔT_S where $\Delta T_S = \Delta T_D$. An increase in the setup time supports a decrease in the hold time by $\Delta T_H = f(\Delta T_S)$, potentially resolving the violation. The delay uncertainty due to a variation is therefore reduced by exploiting interdependent setup-hold times. This procedure is summarized in the flowchart depicted in Fig. 4.

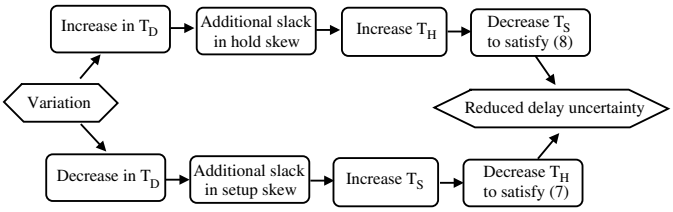


Figure 4: Flow diagram to reduce delay uncertainty by exploiting interdependent setup-hold times.

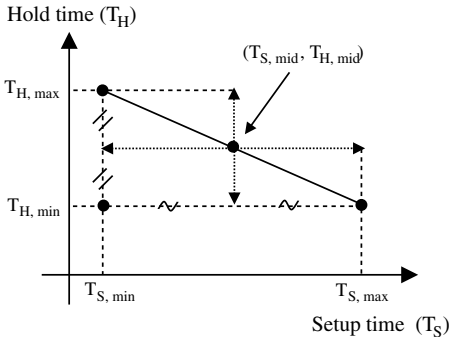


Figure 5: A data path designed at the pair $(T_{S,mid}, T_{H,mid})$ achieves the highest tolerance to variations.

Note that the variation in the delay of the clock launch path ΔT_{Ci} and clock capture path ΔT_{Cf} is assumed in this approach to be equal. For those cases where this assumption is not accurate, the variation in the delay of the clock path may either enhance or degrade the delay uncertainty depending upon the sign of $\Delta T_{Cf} - \Delta T_{Ci}$, as described in the following section.

4.3 Amount of Compensation

The compensation in delay variation (or the reduction in delay uncertainty) is dependent upon three primary factors: (a) the range of the valid setup times $T_{S,r}$ and hold times $T_{H,r}$, (b) the specific (setup, hold) pair used in (3) and (4) to determine the data path delay, and (c) the effect of the variations on the clock launch and capture paths, *i.e.*, the clock distribution network.

If a register has a greater range of valid setup times and hold times, this register is more effective in reducing delay uncertainty. Note however that this type of register may exhibit other tradeoffs such as higher power consumption and CLK-to-Q delay.

As described in Section 3, the specific (setup, hold) pair used to determine the data path delay can lower the power consumption while satisfying the target frequency and achieving a higher tolerance to variations. The middle point of the setup-hold line ($T_{S,mid}$, $T_{H,mid}$) results in a highest tolerance since the setup and hold times exhibit the maximum flexibility to variations, as illustrated in Fig. 5.

Choosing all of the data paths to satisfy the pair ($T_{S,mid}$, $T_{H,mid}$) may cause, however, overdesign of some specific paths. For example, for a critical path, $T_{S,mid} - T_{S,min}$ may be greater than the worst case variation in the data path delay. In this case, a smaller setup time than $T_{S,mid}$ can be chosen for the data path. Similarly,

CHOOSE-PAIR
1. Obtain $T_{S,min}$, $T_{S,max}$, $T_{H,min}$, and $T_{H,max}$ as in Section 4.1
2. Obtain worst case variations in data path delay $T_{D,max}$ and $T_{D,min}$
3. **if** data path is a critical path **then**
4. $T_S = T_{S,min} + (T_{D,max} - T_{D,nom})$
5. **if** $T_S \leq T_{S,max}$ **then**
6. find $T_H = f(T_S)$ using interdependence
7. **else**
8. $T_S = T_{S,max}$
9. $T_H = f(T_{S,max}) = T_{H,min}$
10. **else if** data path is sensitive to a race condition (short path) **then**
11. $T_H = T_{H,min} + (T_{D,nom} - T_{D,min})$
12. **if** $T_H \leq T_{H,max}$ **then**
13. find $T_S = f^{-1}(T_H)$ using interdependence
14. **else**
15. $T_H = T_{H,max}$
16. $T_S = f^{-1}(T_{H,max}) = T_{S,min}$
17. **else**
18. $T_S = (T_{S,min} + T_{S,max})/2$
19. $T_H = f(T_S) = (T_{H,min} + T_{H,max})/2$
20. **end**

Figure 6: Pseudo-code to determine the appropriate (setup, hold) pair that prevents the overdesign of a circuit while achieving a higher tolerance to variations.

for a short path, $T_{H,mid} - T_{H,min}$ may be greater than the worst case variation, suggesting a hold time smaller than $T_{H,mid}$ is possible.

An algorithm is proposed to prevent this overdesign where the selection of the (setup, hold) pair depends upon the type of data path. This technique prevents an overly conservative design while achieving a higher tolerance to variations. Pseudo-code of the proposed algorithm CHOOSE-PAIR is shown in Fig. 6.

The critical points $T_{S,min}$, $T_{S,max}$, $T_{H,min}$, and $T_{H,max}$ are obtained in the first line, as described in Section 4.1. The worst case variation in the delay of the data path is determined in the second line. In lines 3-10, a (setup, hold) pair is determined for a worst case path where the upper bound of the data path delay, *i.e.*, (4), is critical. The minimum valid setup time $T_{S,min}$ is increased by the worst case variation $T_{D,max} - T_{D,nom}$ in the delay of the data path. If the resulting setup time T_S is valid, *i.e.*, $T_S \leq T_{S,max}$, T_S is chosen as the setup time. The corresponding hold time is determined by $T_H = f(T_S)$. If, however, T_S is outside the valid range, $T_{S,r}$ is insufficient to tolerate the variation. In this case, $T_{S,max}$ is chosen as the setup time, providing the maximum tolerance for the critical path.

Alternatively, if the data path is a short path where the lower bound of the data path delay, *i.e.*, (4), is critical, T_H is initially determined in line 11 as the summation of the minimum hold time $T_{H,min}$ and worst case variation $T_{D,nom} - T_{D,min}$. If this hold time is valid, *i.e.*, $T_H \leq T_{H,max}$, T_H is chosen as the hold time. The corresponding setup time is determined by $T_S = f^{-1}(T_H)$. If the hold time is not within this valid range, $T_{H,max}$ is chosen as the hold time since $T_{H,max}$ provides the maximum tolerance for a short path.

For all of the remaining data paths where either (3) or (4) is not critical or if the amount of variation cannot be determined *a priori*, $T_{S,mid}$ and $T_{H,mid}$ are chosen, respectively, as the setup and hold times. At this point, the setup and hold times exhibit the greatest tolerance to delay variations.

The amount of variation tolerated by this methodology is also dependent upon the variation in the delay of the clock launch path ΔT_{Ci} and clock capture path ΔT_{Cf}. Specifically, if $\Delta T_{Ci} = \Delta T_{Cf}$, *i.e.*, constant clock skew, these variations compensate, maintaining the validity of the proposed algorithm. In this case, the variation in the delay of the clock paths does not affect the tolerance. If

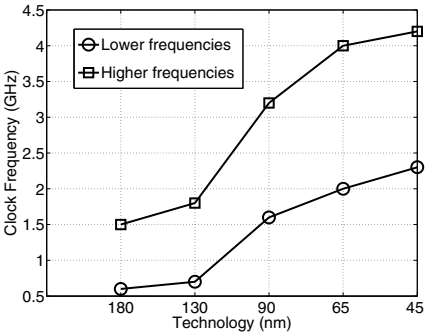


Figure 7: Target clock frequency for each technology node. Higher frequencies represent the upper bound of the frequency while the lower frequencies represent the lower bound of the frequency.

however $\Delta T_{Ci} > \Delta T_{Cf}$, less variation can be tolerated by a critical path since the delay of the clock launch path is increased, delaying the data signal from leaving the register. For a short path, however, additional variation can be tolerated.

Alternatively, if $\Delta T_{Cf} > \Delta T_{Ci}$, additional variation can be tolerated for a critical path since the clock launch path is relatively faster than the clock capture path. For a short path, however, less variation can be tolerated. The effect of the variation on the clock path delays can be considered in the proposed algorithm by replacing line 4 with $T_S = T_{S,min} + (T_{D,max} - T_{D,nom}) + (T_{Ci} - T_{Cf})$ and line 11 with $T_H = T_{H,min} + (T_{D,nom} - T_{D,min}) + (T_{Cf} - T_{Ci})$.

5. CASE STUDY

The efficacy of setup-hold time interdependence to compensate power supply variations is evaluated in this section. Four CMOS technology generations are considered: 180 nm, 90 nm, 65 nm, and 45 nm. An industrial model is used for the 180 nm, 90 nm, and 65 nm CMOS technologies. For the 45 nm CMOS technology, a predictive model is used [10]. Two clock frequencies are considered for each technology based on the data published in [11], as illustrated in Fig. 7. Higher frequencies represent the upper bound on the frequency while the lower frequencies represent the lower bound on the frequency.

The interdependent setup-hold time characteristics for each technology is described in Section 5.1. The dependence of these characteristics on process technology is also discussed. The variation in the delay caused by the power noise is quantified as a function of technology in Section 5.2. Finally, the efficacy of setup-hold time interdependence in tolerating this delay variation is evaluated in Section 5.3.

5.1 Interdependent T_S vs T_H Relationship

A master-slave type, rising edge triggered register is used to illustrate the T_S vs. T_H relationship for each technology node. The register has been simulated to obtain the critical setup-hold pairs, as described in Section 4.1, where the signal transition times are assumed to be 10% of the clock period. The T_S vs. T_H relationship for each technology is illustrated in Fig. 8. Each line can be represented as

$$\text{180 nm: } T_H = -0.386T_S + 72.839 \text{ for } 41 \leq T_S \leq 180, \quad (5)$$

$$\text{90 nm: } T_H = -0.494T_S + 65.32 \text{ for } 33 \leq T_S \leq 125, \quad (6)$$

$$\text{65 nm: } T_H = -0.269T_S + 33.255 \text{ for } 25.8 \leq T_S \leq 110, \quad (7)$$

$$\text{45 nm: } T_H = -0.123T_S + 16.202 \text{ for } 15.4 \leq T_S \leq 98, \quad (8)$$

where each range is in picoseconds. The range of valid setup times

Table 1: Power supply voltage, clock-to-Q delay, and critical points $T_{S,min}$, $T_{H,max}$, $T_{S,max}$, $T_{H,min}$, $T_{S,r}$, and $T_{H,r}$ for each technology.

CMOS Technology	V_{DD} (V)	Clock-to-Q delay (ps)	$T_{S,min}$ (ps)	$T_{H,max}$ (ps)	$T_{S,max}$ (ps)	$T_{H,min}$ (ps)	$T_{S,r}$ (ps)	$T_{H,r}$ (ps)
180 nm	1.8	172	41	57	180	3.3	139	53.7
90 nm	1.2	86.4	33	49	125	3.5	92	45.5
65 nm	1.1	57	25.8	26.3	110	3.6	84.2	22.7
45 nm	1.0	29.8	15.4	14.3	98	4.1	82.6	10.2

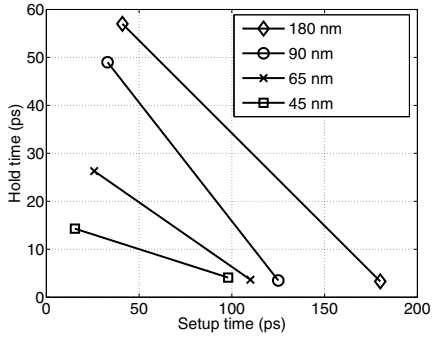


Figure 8: Interdependent setup-hold time characteristics for four technologies.

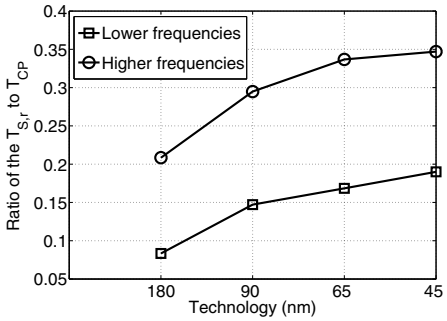


Figure 9: Ratio of the range of valid setup times $T_{S,r}$ to the clock period T_{CP}.

$T_{S,r} = T_{S,max} - T_{S,min}$ and range of valid hold times $T_{H,r} = T_{H,max} - T_{H,min}$ scale with technology, as shown in Fig. 8. These critical points, CLK-to-Q delay of the register, and power supply voltage are listed in Table 1 for each CMOS technology.

Note the behavior of $T_{S,r} = T_{S,max} - T_{S,min}$ (range of valid setup times) as a function of technology. The ratio of the range of valid setup times to the clock period ($T_{S,r}/T_{CP}$) increases as the technology advances, as illustrated in Fig. 9. Specifically, for the 45 nm CMOS technology, the range of valid setup times is approximately 20% of the clock period at lower frequencies. At higher frequencies, this ratio increases to 35%. The interdependence of the setup-hold times is therefore more able to tolerate variations in deep submicrometer technologies, where the difference between the maximum and minimum setup time is a significant fraction of the clock period.

5.2 Delay Variation due to Power Noise

The effect of power supply variations, *i.e.*, power noise, on delay is evaluated in this section. These variations are compared with the range of valid setup times $T_{S,r}$ and hold times $T_{H,r}$, thereby determining the ability to exploit this interdependence to reduce delay uncertainty. The clock period corresponding to each technology is determined from Fig. 7. A critical path is designed for each technology to evaluate the efficacy of exploiting the interdependence relationship in compensating for a drop in the power supply voltage. Identical inverters are used in the combinational circuit. A specific number of inverters is inserted between the initial and final register until the delay of the data path satisfies (4).

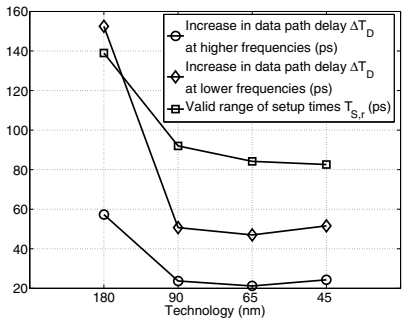


Figure 10: Comparison of the increase in the delay of a critical data path with $T_{S,r}$ to evaluate the efficacy of exploiting the interdependence relationship.

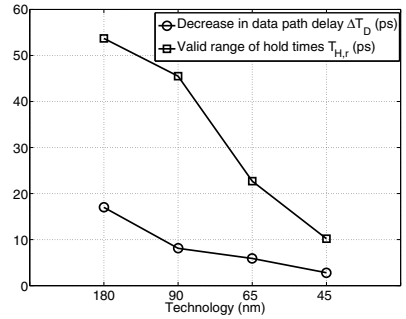


Figure 11: Comparison of the decrease in the delay of a short path with $T_{H,r}$ to evaluate the efficacy of exploiting the interdependence relationship.

A short path can also be generated by abutting the registers. This short path is designed to evaluate the efficacy of exploiting the interdependence relationship in compensating for an increase in the power supply voltage since an increase in V_{DD} reduces the delay of the data path.

These long and short paths are simulated with SPICE, where the power supply voltage is varied by 10%. Specifically, for a long path, the power supply is decreased by 10% while for a short path, the power supply is increased by 10%. The corresponding variation in the delay of a data path is determined by SPICE simulations for each technology. These variations are compared with the range of valid setup times $T_{S,r}$ and hold times $T_{H,r}$, respectively, in Figs. 10 and 11 to evaluate the efficacy of exploiting the interdependence relationship, as described in the following section.

5.3 Compensation of Delay Variations

As illustrated in Fig. 10, the interdependence relationship can be used to compensate for delay variations since the range of valid setup times is higher than the increase in the data path delay except

Table 2: Compensation of delay uncertainty caused by power noise for a critical data path.

Technology (nm)	Critical data path				
	(T_{S1}, T_{H1}) (ps)	Frequency (GHz)	ΔT_D (ps)	(T_{S2}, T_{H2}) (ps)	Compensation (%)
180 nm	(110.5, 30.2)	1.5	57.3	(41,57)	100
		0.6	152.5	(41, 57)	45.6
90 nm	(79, 26.3)	3.2	23.7	(33,49)	100
		1.6	50.7	(33, 49)	90.7
65 nm	(67.9, 14.9)	4	21.2	(25.8, 26.3)	100
		2	47	(25.8, 26.3)	89.5
45 nm	(56.7, 9.2)	4.2	24.3	(15.4, 14.3)	100
		2.3	51.6	(15.4, 14.3)	80.1

for the 180 nm CMOS technology operating at 600 MHz. At this frequency, the delay of the data path is relatively large, causing a higher absolute variation in the delay.

Note that the difference between the range of valid setup times and variation in delay is larger at higher frequencies since the delay of the data path is lower for these frequencies. Exploiting the interdependence relationship is therefore more effective in reducing the delay uncertainty of a critical path operating at higher frequencies. Also note that the absolute variation in delay due to power supply noise somewhat saturates beyond the 130 nm technology node. This behavior is primarily due to the use of multicore processors where the increase in clock frequency is relatively low, as illustrated in Fig. 7.

For a short path, the range of valid hold times is larger than the decrease in data path delay for each technology, as illustrated in Fig. 11. The difference between these two values, however, decreases for more deeply scaled technologies. For a short path, therefore, the interdependence relationship is more effective in reducing delay uncertainty in older technologies. This behavior is due to the significant decrease in the range of valid hold times with scaled technologies.

The procedure described in Section 4.2 has been performed on both long and short data paths. Note that these data paths are designed at the middle point $(T_{S,mid},\ T_{H,mid})$ of the interdependent setup-hold line. For example, for the 90 nm CMOS circuit operating at 3.2 GHz, the delay of the worst case data path increases by 23.7 ps due to a drop in power supply voltage. The hold time of 26.3 ps is increased by 23.7 ps to 50 ps. Since 50 ps is larger than the maximum hold time at this technology, the hold time is increased to 49 ps. An increase in the hold time enables a decrease in the setup time from 79 ps to 33 ps, tolerating 46 ps of delay uncertainty. Note that this delay uncertainty is larger than the initial variation of 23.7 ps, achieving about 100% delay compensation in the critical path.

Similarly, for a short path, the decrease in the delay of the data path is 8.1 ps. The setup time can therefore be increased from 79 ps to 87.1 ps. The corresponding hold time is therefore reduced from 26.3 ps to 22.3 ps, as determined by (6), tolerating 4 ps of delay uncertainty. Since the variation in the delay of the data path is 8.1 ps, interdependence can compensate approximately 50% of the delay uncertainty of a short path. The results of this procedure for other technology nodes are listed in Tables 2 and 3 for, respectively, a worst case data path and a short path.

As listed in Table 2, delay uncertainty caused by power supply noise in a critical data path can be compensated by up to 100% at higher frequencies. At lower frequencies, more than 80% compensation is achieved in more deeply scaled technologies. Alternatively, as listed in Table 3, for a short path, the compensation is lower due to the relatively smaller slope of the function $T_H = f(T_S)$ as compared to $T_S = f^{-1}(T_H)$, as illustrated in Fig. 8.

Table 3: Compensation of delay uncertainty caused by power noise for a short path.

Technology (nm)	Short path			
	(T_{S1}, T_{H1}) (ps)	ΔT_D (ps)	(T_{S2}, T_{H2}) (ps)	Compensation (%)
180 nm	(110.5, 30.2)	17	(127.5, 7.1)	41.8
90 nm	(79, 26.3)	8.1	(87.1, 22.3)	50
65 nm	(67.9, 14.9)	5.9	(73.8, 13.4)	26.2
45 nm	(56.7, 9.2)	2.8	(59.5, 8.9)	10.7

6. CONCLUSIONS

A methodology is proposed to improve the tolerance of a circuit to process and environmental variations. The interdependence between the timing constraints is exploited to achieve a more robust circuit, significantly reducing the delay uncertainty caused by variations. An algorithm is proposed to appropriately determine the (setup, hold) pair during the design process to improve the tolerance of a circuit to variations while achieving a target frequency. A technique is also proposed to efficiently obtain the critical (setup, hold) pairs of a register. A case study is evaluated to validate the significance of setup-hold interdependence in reducing delay uncertainty due to power supply noise, thereby improving the tolerance of a circuit to delay variations.

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