Line Width Optimization for Interdigitated Power/Ground Networks

Renatas Jakushokas
jakushok@ece.rochester.edu

Eby G. Friedman
friedman@ece.rochester.edu

Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627

ABSTRACT

Higher operating frequencies have increased the importance of inductance in power and ground networks. The effective inductance of the power and ground network can be reduced with an interdigitated structure. A closed-form solution for determining the optimal power and ground wire width is described, producing the minimum impedance within an interdigitated structure. The optimal wire width is determined under different physical network dimensions and signal frequencies, suggesting useful trends for interdigitated power and ground networks. In addition, a closed-form expression for the optimal wire width is determined that minimizes the voltage drop over a single metal layer of an interdigitated power/ground network.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]: Miscellaneous—*Power supply networks*

General Terms

Design

Keywords

Power/ground network, interdigitated structure, optimal line width

1. INTRODUCTION

With high operating frequencies and scaled geometries, the power and ground (P/G) distribution network requires enhanced optimization to provide significant current flow. The higher currents increase voltage losses within the P/G network, while decreasing power supply voltages provide lower noise margins.
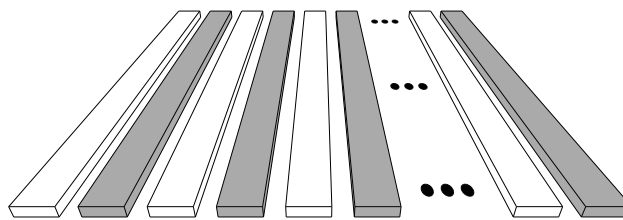
Figure 1: An interdigitated P/G distribution structure. The darker and lighter lines represent the power and ground lines, respectively.

With flip-chip packaging, the package inductance is reduced [1], making the on-chip inductance more significant. Since the voltage variations within a P/G network are due to *IR* [2, 3] and $L\frac{di}{dt}$ [4] voltage drops, the effective resistance and inductance are the primary foci of the optimization process. At higher frequencies, the inductive impedance is dominant, requiring accurate estimation of the effective inductance.

An interdigitated P/G distribution network structure where a few wide lines are replaced by a large number of narrow lines is often used to reduce the inductive effect [5, 6]. Different P/G structures have been compared in [7, 8], where an interdigitated structure is shown to achieve the greatest reduction in inductance.

Each layer of a multi-layer interdigitated structure consists of individual interdigitated power and ground wires, as depicted in Fig. 1. Routing flexibility and reduced inductance are two primary advantages of an interdigitated P/G distribution structure.

The need for efficient P/G networks has been recognized, and several techniques to optimize the P/G distribution network have been developed [9, 10]. More advanced techniques for designing power networks have been described [11, 12]; however, only the package inductance is considered, neglecting the on-chip inductance. With more advanced packaging techniques (such as flip-chip), the on-chip inductive noise ($L\frac{di}{dt}$) is also important [1, 13]. To consider on-chip inductance in power supply networks, a technique to simplify the mesh model of an *RLC* power network is proposed [14], assuming the loads are treated as identical current sources. The significance of the on-chip inductance within paired and interdigitated power/ground network structures is described in [15], where the inductance is treated as a local effect. In [16], the inductance model considers the mutual inductance between close and distant power/ground wires in interdigitated structures. Based on this model, a closed-form expression characterizing a single

layer of an interdigitated P/G network structure is utilized, permitting the optimal width of a power/ground network that minimizes the network impedance to be determined.

The paper is organized as follows. The problem is formulated in Section 2. The resistance and inductance of an interdigitated power and ground structure are discussed in Section 3. In Section 4, a closed-form expression for the line width that produces the minimum impedance for a single metal layer is presented. The accuracy of the optimal line width and related issues are discussed in Section 5. The paper is concluded in Section 6.

2. PROBLEM FORMULATION

An interdigitated P/G distribution network is typically allocated over an entire upper metal layer, where the network is designed for minimum impedance. The overall impedance of a power/ground network is

$$Z_{eff} = R_{eff} + j2\pi f L_{eff}, \tag{1}$$

where R_{eff} and L_{eff} are, respectively, the effective resistance and inductance of the network. f is the target frequency.

The objective is to minimize the overall impedance of a network at a specific frequency, reducing the voltage drop on the power/ground network. For constant area, two design variables, the line-to-line spacing s and width of the lines w, characterize a single metal layer of an interdigitated power/ground network. The absolute value of the effective impedance as a function of line-to-line spacing and line width is

$$|Z_{eff}(s,w)| = \sqrt{R_{eff}^2(s,w) + 4\pi^2 f^2 L_{eff}^2(s,w)}. \tag{2}$$

For constant area, different line widths, shown in Fig. 2, produce a different network impedance. A higher line width reduces the resistance, however, the inductance increases due to the fewer number of interdigitated power/ground pairs. The primary objective is to determine the width that produces the lowest impedance for a single metal layer within an interdigitated power/ground distribution network.

3. IMPEDANCE OF AN INTERDIGITATED P/G DISTRIBUTION NETWORK

The overall impedance of a power/ground network is a combination of the effective resistance and inductance. In the following subsections, a model for the effective resistance and inductance of an interdigitated network assuming a constant area is presented.

3.1 Effective Resistance

The overall area allocated for a power/ground network is

$$A = l\left[N\left(w + s + w + s\right)\right] = 2lN\left(w + s\right), \tag{3}$$

where l and N are, respectively, the length of a single power or ground wire and the number of interdigitated pairs. Since N pairs of an interdigitated power and ground wires are in parallel, the effective resistance of the network R_{eff} is

$$R_{eff} = \frac{1}{N}\rho\frac{2l}{tw}, \tag{4}$$

where t is the thickness of the metal. Substituting (3) into (4), the effective resistance for a constant area is

$$R_{eff} = \frac{4l(w+s)}{A}\rho\frac{l}{tw}, \tag{5}$$
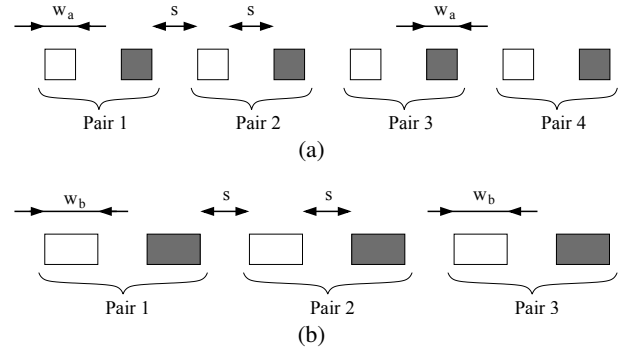
where ρ is the metal resistivity.

Figure 2: For the same physical area, two different interdigitated power/ground networks are presented. The spacing s is maintained constant. The width w is different for each network, where the width w_a of network (a) is thinner than the width w_b of network (b). Increasing the width requires fewer interdigitated power/ground line pairs since the area is maintained constant.

Due to the skin effect, the resistance increases with higher signal frequencies. In this paper, however, the skin effect is neglected since the highest target frequency is 10 GHz, resulting in a skin depth of $0.65\,\mu$m for copper wires. Half the thickness of the highest metal layer for a 65 nm CMOS technology [17] is less than the skin depth, justifying the assumption of a uniform current distribution. In addition, with advancements in technology, the thickness of the metal layers is decreasing, making the skin effect less significant.

3.2 Effective Inductance

The effective inductance of a single metal layer is

$$\frac{1}{L_{eff}} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} + ... + \frac{1}{L_N}, \tag{6}$$

where L_1, L_2, L_3, and L_N are, respectively, the effective inductance of the first, second, third, and N^{th} pair of an interdigitated P/G distribution network (refer to Fig. 2). Assuming the current flows in opposite directions in power and ground wires, the effective inductance of every pair can be determined [18].

The difference in inductance is small among all of the pairs in an interdigitated power/ground network, excluding those pairs closest to the boundary. The effect of the boundary is neglected, assuming all of the individual inductances are equal, permitting the effective inductance of a single layer within an interdigitated P/G distribution network to be determined [16]. A similar assumption is considered in [8], neglecting the mutual inductance between distant pairs, effectively treating the inductance as a local phenomena. By not neglecting distant mutual effects, the effective inductance can be estimated with higher precision. A derivation of the proposed effective inductance expression is presented in [16], based on the Wallis formula [19], resulting in

$$L_{eff} = \frac{1}{N}\frac{\mu_0 l}{\pi}\left[ln\left(\frac{w+s}{w+t}\right) + \frac{3}{2} + ln\left(\frac{2}{\pi}\right)\right], \tag{7}$$

where N and μ_0 are the number of power and ground pairs and the permeability of a vacuum, respectively.

Substituting (3) into (7), the effective inductance of an interdigitated network is

$$L_{eff} = \frac{2l(w+s)}{A}\frac{\mu_0 l}{\pi}\left[ln\left(\frac{w+s}{w+t_{ind}}\right) + \frac{3}{2} + ln\left(\frac{2}{\pi}\right)\right], \tag{8}$$
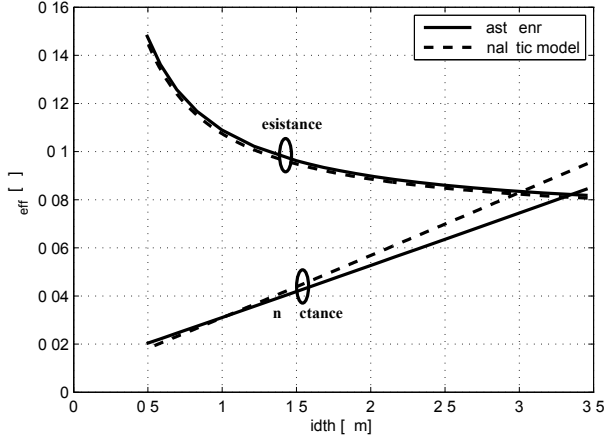
Figure 3: **Effective resistance and inductance at 5 GHz as a function of wire width for a single layer within an interdigitated P/G distribution network. The overall area is maintained constant.**

where the line thickness t is replaced with t_{ind} to simplify the model when determining the optimal width.

4. OPTIMAL WIDTH FOR MINIMUM IMPEDANCE

The effective resistance (5) and inductance (8) as a function of wire width are compared with FastHenry [20] and illustrated in Fig. 3. A 1 x 1 mm^2 area of the top metal layer for a 65 nm CMOS [17] technology is chosen. The target frequency is 5 GHz. For constant area, according to (5), wider power and ground wires reduce the effective resistance. With multiple thin lines, a large area is consumed by the line-to-line spacing, increasing the effective resistance of the network. The inductance under a constant area constraint has the opposite effect since the mutual component of the inductance is dominant in an interdigitated P/G distribution structure. Additional lines increase the mutual inductance, reducing the effective inductance according to (8). Since the effective resistive and inductive impedance in interdigitated structures behaves inversely with increasing wire width, the objective is to minimize the overall impedance of the network at a target frequency.

In the network, the line-to-line spacing is based on the interconnect characteristics. The network impedance from (2) is therefore

$$|Z_{eff}(w)| = \sqrt{R_{eff}^2(w) + 4\pi^2 f^2 L_{eff}^2(w)}, \qquad (9)$$

a function of line width. In Fig. 4, (9) is compared to FastHenry for several line widths.

Since the effective inductance in (8) is a transcendental function of width, a closed-form analytic solution can not be determined for the wire width that minimizes the impedance. A closed-form expression can, however, be determined for the special case where $s = t_{ind}$, resulting in

$$w_{opt}^{(0)} \approx \sqrt[3]{0.91 \frac{s\rho^2}{\mu_o^2 t^2 f^2}}. \qquad (10)$$

A detailed derivation of (10) is presented in the Appendix. A numerical solution based on n iterations of the Newton–Raphson
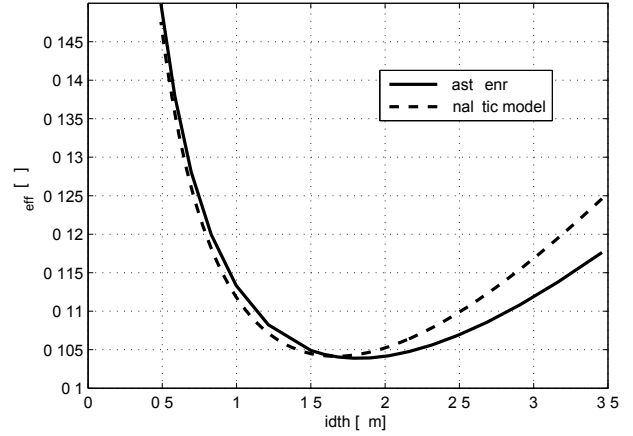

Figure 4: **Magnitude of the impedance of (9) and FastHenry.**

method is used to determine the optimal width for all other spacings,

$$w_{opt}^{(n)} = w_{opt}^{(n-1)} - \frac{F\prime(w_{opt}^{(n-1)})}{F\prime\prime(w_{opt}^{(n-1)})}, \qquad (11)$$

where $F \equiv |Z_{eff}(w)|$ and $w_{opt}^{(n-1)}$ is the $(n-1)^{st}$ estimate of the optimal wire width. The initial estimate is based on (10). The number of iterations can be increased to enhance the accuracy of the optimal width.

Considering resistance and inductance (both self and mutual) of a network, (10) combined with (11) determines the optimal line width of an interdigitated power/ground network. The optimal line width produces the minimum impedance network at a target frequency.

5. OPTIMAL WIDTH CHARACTERISTICS

The optimal width for different thicknesses and spacings is evaluated in this section. The required number of iterations of the Newton–Raphson method is determined. The range of frequency for the optimum width is also reviewed. Finally, the effect of the decoupling capacitance on the optimal width is discussed.

5.1 Effect of Thickness and Spacing

A comparison among FastHenry, (10), and $w_{opt}^{(1)}$ based on the first iteration of the Newton–Raphson method is shown in Fig. 5 for several different metal thicknesses. The spacing is chosen as the mid point between the thinnest and thickest metal layers for a 65 nm CMOS technology. A 5 GHz frequency is assumed. The error between FastHenry and (10) reaches 6%, while the error between FastHenry and $w_{opt}^{(1)}$ is below 1%. For those cases where the target accuracy is below the error of the initial estimate, the closed-form expression of $w_{opt}^{(0)}$ is computationally efficient in determining the P/G line width. If higher accuracy is required, the interdigitated P/G wire width can be determined according to (11).

A comparison among FastHenry, (10), and $w_{opt}^{(1)}$ based on the first iteration of the Newton–Raphson method is shown in Fig. 6 for different spacings. The spacing ranges from 0.54 μm (the lowest permitted spacing) to 15 μm. When the spacing is equal to the thickness, $w_{opt}^{(0)}$ and $w_{opt}^{(1)}$ are equal since the logarithmic term of

Figure 5: Closed-form $w_{opt}^{(0)}$ and $w_{opt}^{(1)}$ based on the first iteration of the Newton-Raphson method as compared with FastHenry for different thicknesses.
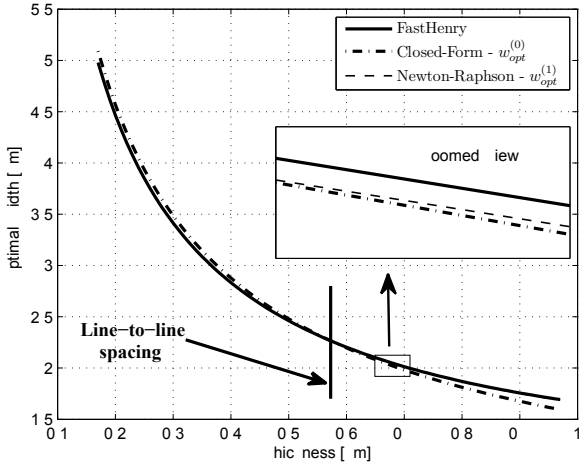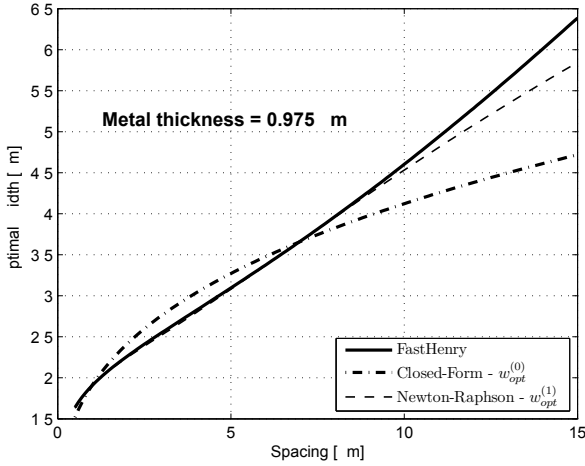

Figure 6: Closed-form $w_{opt}^{(0)}$ and $w_{opt}^{(1)}$ based on the first iteration of the Newton-Raphson method as compared with FastHenry for different spacings.

(8) is zero. At spacings below 7 μm, (10) exhibits an error below 9% as compared to FastHenry. For spacings up to 15 μm, the error between FastHenry and (10) reaches 26%, while the error with only one iteration of the Newton–Raphson method is below 9%. For spacings greater than 15 μm, additional iterations of the Newton–Raphson method are necessary.

The different number of iterations to determine w_{opt} is evaluated in Fig. 7. The error is relative to FastHenry. Note that (10) assumes the spacing and thickness are equal. The closed-form expression is therefore only accurate for small spacings. For wider spacings, the Newton–Raphson method is preferred to accurately determine the optimal width. A larger number of iterations is needed for wider spacings since the error decreases significantly for a large number of iterations. Spacings up to 100 μm are evaluated, suggesting that four iterations are sufficient to determine the optimal width within 10% accuracy as compared to FastHenry.
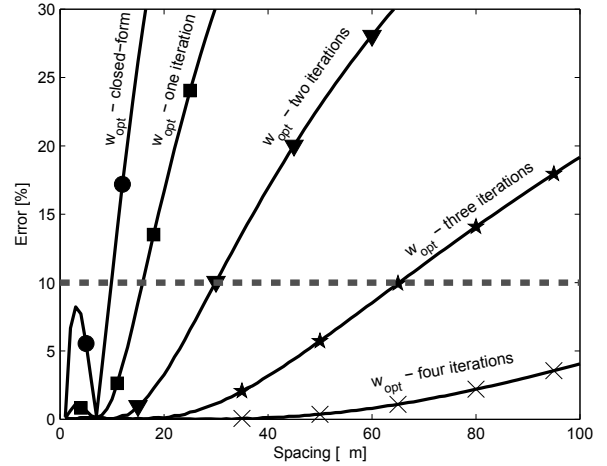

Figure 7: Error of w_{opt} is evaluated for several spacings using closed-form and one to four iterations of the Newton–Raphson method. The error is relative to FastHenry.

5.2 Frequency Range

Since the width is optimized for a target frequency, the effect on the frequency range of interest (from DC to the target frequency) is important. In the following discussion, a target frequency of 5 GHz is assumed. In Fig. 8, the impedance of the network as a function of frequency is depicted. Three values of the width are evaluated - the optimal width, a width four times greater than the optimal width, and a width four times smaller than the optimal width. Note that the area is maintained constant. An increasing width corresponds to a fewer number of interdigitated pairs within the P/G network (a thinner line corresponds to a higher number of interdigitated pairs).

As illustrated in Fig. 8, the minimum impedance at 5 GHz is achieved using the optimal width, while a lower and higher line width increases, respectively, the resistive and inductive component of the overall impedance. At low frequencies, the P/G network with wider lines produces a lower impedance, although more than the required impedance at the target frequency. In the example shown in Fig. 8, the network impedance with wider lines is below the target impedance only below 3.7 GHz. As depicted in Fig. 8, the P/G network with a smaller width satisfies the impedance requirements only up to 2.5 GHz.

5.3 Capacitive Component

The three capacitive components within a P/G distribution network are intentionally placed decoupling capacitance, non-switching circuitry behaving as a capacitance between the power and ground wires, and the line capacitance between the power and ground wires. Since the non-switching circuitry and decoupling capacitance are significantly larger than the line capacitance, the line capacitance can be neglected. The capacitance is therefore not significantly affected by the change in the line width of the P/G network. Note that the overall impedance is different when considering the decoupling capacitance. The optimal width that minimizes the impedance of a network is similarly determined as (11), since the decoupling capacitance is independent of line width.
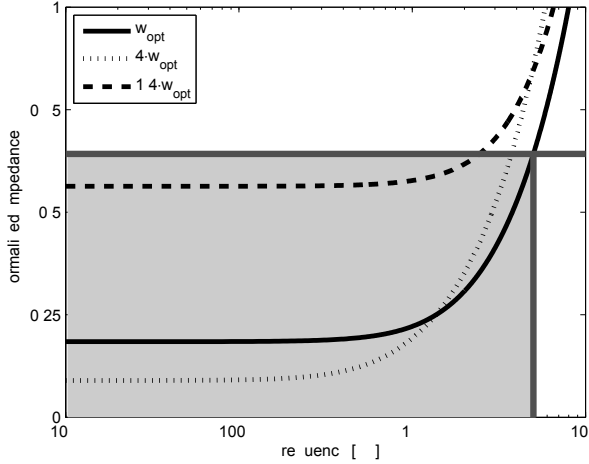
Figure 8: Impedance over the frequency range of interest. Three different P/G network line widths are depicted. The impedance is minimum at the target frequency with the optimum width.

5.4 Minimum Voltage Drop

The problem can be reformulated to determine the optimum wire width that minimizes the voltage drop over a power/ground network. This voltage drop is

$$V_{drop}(w) = i(\tau)R_{eff}(w) + \frac{di(\tau)}{d\tau}L_{eff}(w), \qquad (12)$$

where $i(\tau)$ represents the time dependent load current. A closed-form solution for the wire width that produces the minimum voltage drop assuming $s = t_{ind}$ is

$$w_{opt} = \sqrt{\frac{2\pi\rho s \cdot i(\tau)}{\mu_0 t\left(\frac{3}{2} + ln\left(\frac{2}{\pi}\right)\right) \cdot \frac{di(\tau)}{d\tau}}}. \qquad (13)$$

For all other cases where $s \neq t_{ind}$, an iterative solution can be used to determine the optimal wire width. Note that (13) is a function of τ, requiring the optimal wire width to be determined at a specific time (a worst case condition) or over a specific time interval (average effect).

6. CONCLUSIONS

The characteristics of an interdigitated power and ground network are investigated in this paper. The effect of resistive and inductive impedances under a constant area constraint is observed for different wire widths (or number of interdigitated pairs).

Under a constant area constraint, conflicting behavior of the effective resistive and inductive impedances is observed with increasing wire width. This conflicting behavior is explored to achieve the minimum impedance of a single interdigitated metal layer. A closed-form expression for the line width is determined, achieving high accuracy for small spacings as compared to FastHenry. The accuracy of the optimal width is enhanced over a wide range of spacings utilizing iterative approaches (up to four iterations). The effect of different spacings, thicknesses, and frequencies on the optimal width is reviewed. A design methodology that considers the network resistance and inductance (both self and mutual) of a single interdigitated metal layer network that produces the minimum impedance is presented in this paper. In addition, a closed-form expression for determining the optimal wire width is described that

minimizes the voltage drop over a single metal layer of an interdigitated power/ground network.

APPENDIX

Since the effective inductance is a transcendental function of width, no closed-form analytic solution can be determined for the wire width that minimizes the effective impedance. The effective inductance for an interdigitated structure where the distance between the power and ground wires is equal to the thickness of the metal is

$$\langle L_{eff} \rangle_{s=t_{ind}} = \frac{2l(w+s)}{A}\frac{\mu_0 l}{\pi}\left[\frac{3}{2} + ln\left(\frac{2}{\pi}\right)\right]. \qquad (A-1)$$

The minimum impedance is determined by solving for the root of the derivative of $\left|Z_{eff}(w)\right|_{s=t_{ind}}$,

$$\frac{\partial\left|\left[Z_{eff}(w)\right]_{s=t_{ind}}\right|}{\partial w} = 0. \qquad (A-2)$$

A closed-form solution for the wire width that produces the minimum impedance assuming $s = t_{ind}$ is

$$w_{opt} = \left(\frac{1}{\left[\frac{3}{2} + ln\left(\frac{2}{\pi}\right)\right]^2}\right)^{1/3}\sqrt[3]{\frac{s\rho^2}{\mu_o^2 t^2 f^2}}. \qquad (A-3)$$

7. REFERENCES

[1] H. B. Bakoglu, *Circuits, Interconnects, and Packaging for VLSI*, Addison-Wesley, 1990.

[2] K. T. Tang and E. G. Friedman, "Incorporating Voltage Fluctuations of the Power Distribution Network into the Transient Analysis of CMOS Logic Gates," *Analog Integrated Circuits and Signal Processing*, Vol. 31, No. 3, pp. 249–259, June 2002.

[3] A. H. Ajami, K. Banerjee, A. Mehrotra, and M. Pedram, "Analysis of IR-Drop Scaling with Implications for Deep Submicron P/G Network Designs," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 35–40, March 2003.

[4] K. T. Tang and E. G. Friedman, "Simultaneous Switching Noise in On-Chip CMOS Power Distribution Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 10, No. 4, pp. 487–493, August 2002.

[5] D. A. Priore, "Inductance on Silicon for Sub-Micron CMOS VLSI," *Proceedings of the IEEE Symposium on VLSI Circuits*, pp. 17–18, May 1993.

[6] L.-R. Zheng and H. Tenhunen, "Effective Power and Ground Distribution Scheme for Deep Submicron High Speed VLSI Circuits," *Proceedings of the IEEE International Symposium on Circuit and Systems*, Vol. I, pp. 537–540, May 1999.

[7] M. Popovich, A. V. Mezhiba, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors*, Springer, New York, 2008.

[8] A. V. Mezhiba and E. G. Friedman, "Inductance Properties of High-Performance Power Distribution Grids," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 10, No. 6, pp. 762–776, December 2002.

[9] W. S. Song and L. A. Glasser, "Power Distribution Techniques for VLSI Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 21, No. 1, pp. 150–156, February 1986.

[10] K.-H. Erhard, F. M. Johannes, and R. Dachauer, "Topology Optimization Techniques for Power/Ground Networks in VLSI," *Proceedings of the European Design Automation Conference*, pp. 362–367, September 1992.

[11] K. Wang and M. Marek-Sadowska, "On-Chip Power-Supply Network Optimization Using Multigrid-Based Technique," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 24, No. 3, pp. 407–417, March 2005.

[12] J. Singh and S. S. Sapatnekar, "Partition-Based Algorithm for Power Grid Design Using Locality," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 4, pp. 664–677, April 2006.

[13] A. V. Mezhiba and E. G. Friedman, "Scaling Trends of On-Chip Power Distribution Noise," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 4, pp. 386–394, April 2004.

[14] D. Khalil and Y. Ismail, "Approximate Frequency Response Models for RLC Power Grids," *Proceedings of the IEEE International Symposium on Circuit and Systems*, pp. 3784–3787, May 2007.

[15] N. Srivastava, X. Qi, and K. Banerjee, "Impact of On-Chip Inductance on Power Distribution Network Design for Nanometer Scale Integrated Circuits," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 346–351, March 2005.

[16] R. Jakushokas and E. G. Friedman, "Inductance Model of Interdigitated Power and Ground Distribution Networks," *IEEE Transactions on Circuits and Systems II: Analog and Digital Processing*, Vol. 56, No. 7, pp. 585–589, July 2009.

[17] P. Bai *et al.*, "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 657–660, December 2004.

[18] F. Grover, *Inductance Calculation: Working Formulas and Tables*, Dover, New York, 1962.

[19] J. Wallis, *Opera Mathematica*, Oxonii, Leon: Lichfield Academiæ Typographi, 1656.

[20] M. Kamon, M. J. Tsuk, and J. K. White, "FastHenry: A Multipole-Accelerated 3-D Inductance Extraction Program," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 42, No. 9, pp. 1750–1758, September 1994.