Noise Immunity of Digital Circuits in Mixed-Signal Smart Power Systems

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Abstract— **Experimental data describing circuit and physical design issues that influence the noise immunity of digital latches in mixed-signal smart power circuits are described and discussed. The principal result of this paper is the characterization of the conditions under which substrate noise generated by high power analog circuitry affects digital latches. The experimental data characterize a variety of different noise mitigation techniques for the particular process technology, circuit structures, signal/clocking interdependencies, and related conditions.**

I. Introduction

The correct operation of integrated circuits can be greatly affected by noise, and in particular on-chip substrate coupling noise. Existing research in substrate coupling noise in mixed-signal circuits has concentrated on the problem of the digital circuitry influencing highly sensitive analog circuitry [1–6]. The noise immunity of digital circuits in a smart power environment requires investigation in order to develop reliable design techniques for these mixed-signal systems. Currently, substrate coupling noise does not create a problem in deep submicrometer (DSM) digital processes, but as these technologies continue to scale, substrate coupling noise in DSM CMOS circuits will also require specialized noise mitigation techniques.

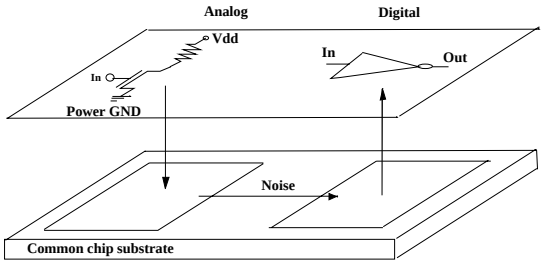

Fig. 1. Noise coupling in smart power circuits.

The interaction between the high power analog circuitry and the digital latches where both are on the same monolithic substrate is graphically shown in Fig. 1. This problem is the topic of this paper. The primary objectives are to investigate the principal processes that generate, transmit, and receive noise in mixed-signal smart power circuits in a high voltage process [7], and to develop techniques to minimize substrate coupling between the analog and digital circuit components.

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The test circuits are described in Section II. The test conditions and set-up are reviewed and discussed in Section III. In Section IV, the test results are presented and discussed. Some conclusions are offered in Section V.

II. Basic elements

A number of test circuits have been designed and fabricated in a high voltage NMOS process [7]. A microphotograph of a test circuit from the main group of test circuits is shown in Fig. 2, and the corresponding floorplan is shown in Fig. 3. Eight groups of analog power drivers, each group containing eight individual drivers, are shown. Each driver is logically selected and driven by the select registers and predrivers blocks. Thirty-two serially connected registers along the length of the chip are used to monitor the generated noise. Other test configurations place the sensitive registers between two groups of power drivers, or below the power drivers. All the registers are master-slave and use a double phase clock distributed from an internal non-overlapping clock generator derived from an external clock signal.

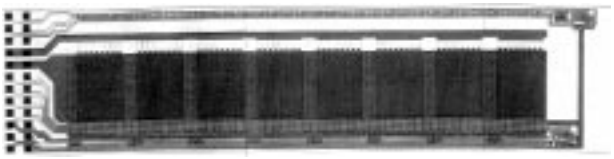

Fig. 2. Microphotograph of the primary mixed-signal test circuit.

III. Test conditions and experimental set-up

A variety of different issues have been evaluated in order to study substrate coupling in smart power systems. These issues are summarized in Table I. Each test configuration is evaluated individually and in combination. The experimental set-up is depicted in Fig. 4. The auxiliary equipment includes power supplies, multimeters, an oscilloscope, a printer, and a Sun Sparc2 workstation.

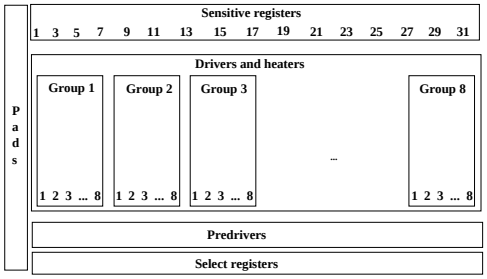

Fig. 3. Layout floorplan of the mixed-signal test circuit.

TABLE I

TEST PLAN FOR ANALYSIS OF SUBSTRATE COUPLING NOISE. EACH ISSUE IS EVALUATED FOR BOTH STATIC AND DYNAMIC REGISTERS.

No.	Issue
1.	Generated noise dependency on power driver voltage and current
2.	Received noise dependency on sensitive register position and orientation
3.	Received noise dependency on substrate contact placement and layout
4.	Generated noise dependency on the time during which the power drivers are on
5.	Received noise dependency on power drivers "on–off"timing with respect to register clocking
6.	Noise spreading dependency on chip temperature
7.	Received noise dependency on ground layout and connectivity
8.	The dependency of the generated noise on the number of active power drivers

IV. TEST RESULTS AND DISCUSSION

As described in the literature on substrate coupling in mixed signal systems [1–6], the noise receptor typically consists of a current source (a transistor with a load resistor). In the experiments described in this paper, however, where the analog circuitry affects the digital circuitry, the sensitive circuitry consists primarily of latched inverters (Fig. 5a). The load is active, and generally consists of a depletion mode NMOS transistor. The noise source consists of high power drivers (see Fig. 5b). In digital switched induced substrate coupling noise [1–5], experimentally observed noise waveforms due to the switching digital logic blocks have been reported. These waveforms are compared with simulation results using MEDICI [8]. A typical noise waveform is shown in Fig. 6. A similar noise waveform has been experimentally observed in the smart power circuits discussed in this paper. In the results presented here, V_{pp} (see Fig. 6) is significant only if it changes the logic state of the sensitive (or victim) digital circuit. Accordingly, in all the experimentally obtained data, the noise level represents the number of registers affected by the substrate noise expressed as the percentage of the total number of target registers.

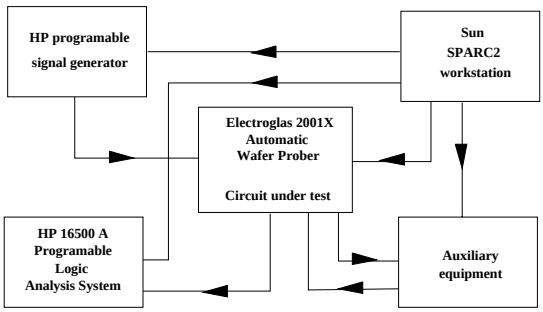

Fig. 4. The experimental test set-up.

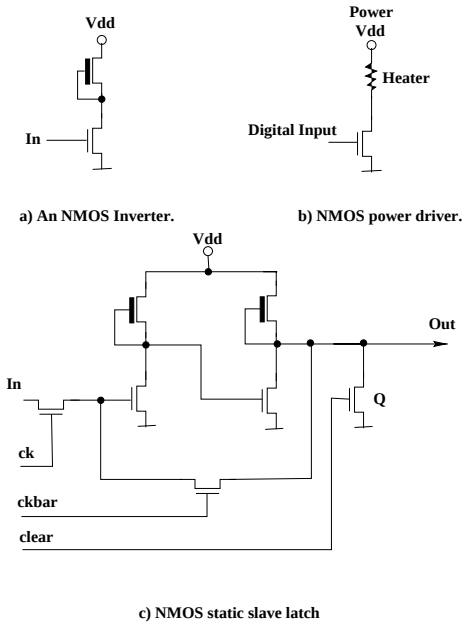

Fig. 5. Circuit schematic of NMOS circuit blocks.

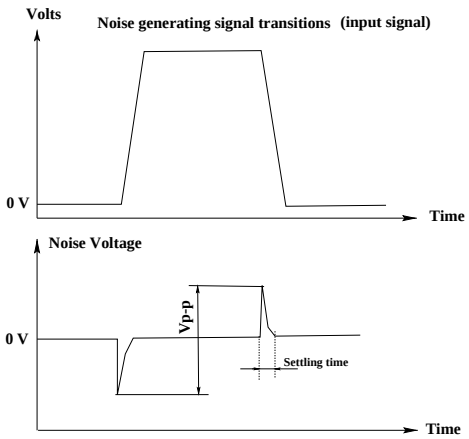

Fig. 6. Characteristic noise waveform caused by digital switching.

The observed tolerance to noise for both the static and dynamic registers which are physically placed as shown in Fig. 3 is summarized in Table II. The noise tolerance is dependent on specific circuit details such as the nature of the latches, circuit differences between the master and slave latches, transistor sizes, and noise margins of the logic family. For static registers, the noise tolerance improves for the 3 and 4 clocking regimes (the exterior input clock is high when the power drivers turn off as shown in Fig. 7) if the sensitive registers are placed between two power driver groups (called the middle groups). The noise tolerance is particularly improved when the registers are placed below the power drivers (called the lower groups). The cause of this improved tolerance can be attributed to the following reasons:

- The substrate contacts of the power drivers of the middle and lower groups are physically closer to the target registers [4].

• The main group of circuits, as shown in Fig. 3, contain no substrate contacts between the power drivers and the registers (due to the power resistors). For the middle and lower groups there are substrate contacts between the power drivers and registers, improving the noise behavior.
• The ground distribution routing criteria for noise immunity [6, 9] improves in the order of the main, middle, and lower groups. Accordingly, the noise immunity for the lower group is better than the middle group, which is better than the main group.
• The orientation of the registers [2] is changed with respect to the noise source. When the depletion transistors are closer to the noise source, the noise behavior is improved by up to 10% versus the case when the enhancement and pass transistors are closer to the noise source.

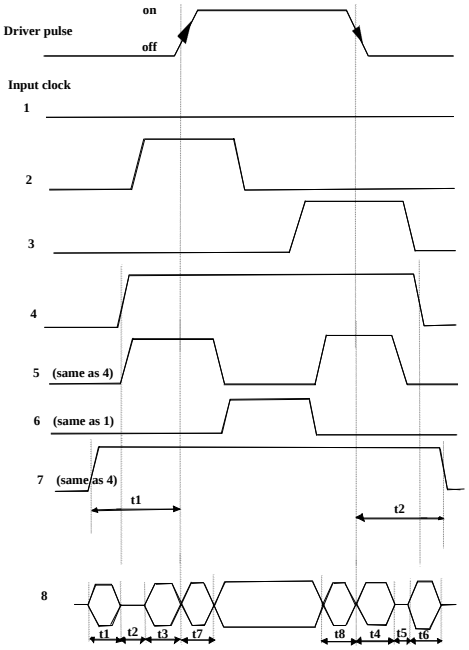

Fig. 7. The relationship between the external input clock signal (clock phases) and the driver on-time, generating different clocking regimes for the analyzed circuits.

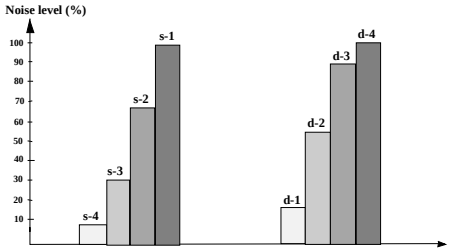

Fig. 8. The noise tolerance as a function of clocking regime for the static and dynamic registers. s=static, d=dynamic, and 1, 2, 3, 4 are according to Table II. The 100% noise level influence is relative, and the dynamic registers are ≈ 1.3X larger than the static registers.

Test chips with vertical distances between 70 μm and 500 μm (see Fig. 3), and up to an ≈ 3000 μm horizontal distance between the sensitive registers and the power drivers are considered and evaluated for each of the 32 registers. The influence of distance on the noise is graphically shown in Fig. 9. No significant influence is noted for very large distances, because of the significantly decreased noise [1, 2].

TABLE II
THE NOISE TOLERANCE OF THE SENSITIVE REGISTERS.

Issue	Static sensitive registers	Dynamic sensitive registers
Register noise induced transition (i-initial, f-final state)	i=1 to f=0 only	i=1 to f=0 i=0 to f=1 P(0-1)>P(1-0)
Dependency of register noise tolerance on the relationship between input clock state and the time when the power drivers are on (see Fig. 7) see Fig. 8	1, 2, 3, 4 1-worst 4-best 5 same as 4 6 same as 1 7 and 8 If t1, t2, t3, t4, t7, and t8<1 μs, ⇒uncertain (any of 1 to 4) –cont–	4, 3, 2, 1 4-worst 1-best 5 same as 4 6 same as 1 –cont– else, ⇒distinctive (any of 1 to 4)

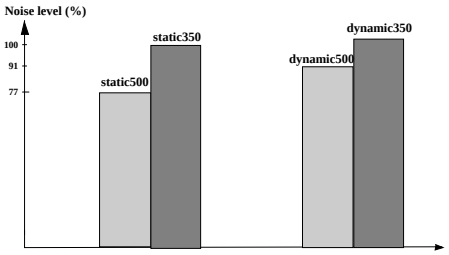

Fig. 9. The dependency of the received noise on the physical separation for the static and dynamic registers. Two distances, 350 μm and 500 μm, are shown. The 100% noise level influence is relative to the maximum noise, and the dynamic registers are ≈ 1.15X larger than the static registers.

The specific registers (of the 32) that are affected depend a great deal on which group of drivers is active. It is shown that a specific group of active drivers has a different influence over specific registers depending on the particular clocking regime, as described in Fig. 7. In Fig. 10, this influence is shown for the case where the group 2 drivers are active (see Fig. 3). Test results demonstrate that the closer the active group is to the right of the chip, the less the register distribution is affected by noise. For example, when the group 5 drivers are active, the distribution of affected registers as a function of clocking regime is more centered.

Effective substrate contact placement reduces the substrate noise and biasing, while incorrect placement of the

substrate contacts can actually increase the noise [1–4, 6]. Ground routing to obtain a uniform substrate bias during switching improves the noise immunity. For the particular (functionally imposed) ground routing and substrate contact placement, a ground biasing effect is noted due to the high currents that are switched. This effect influences the logic circuits and biases the substrate.

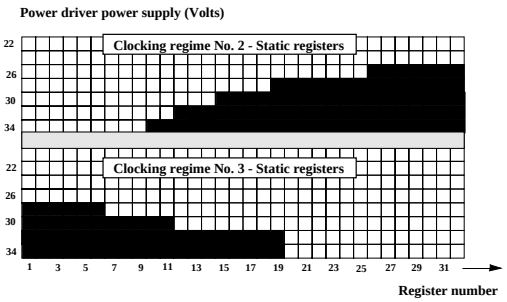

Fig. 10. Noise tolerance affecting specific register location as a function of power driver voltage, substrate bias, clocking regime, ground bias, and active power driver group. Group 2 is active. Black shaded area represents the affected registers.

The generated noise increases as the time during which the power drivers are on increases. Times larger than $5\,\mu$s for high voltages generate excessive power dissipation. The generated noise increases as the driver power supply voltage and current increases, as shown in Fig. 11.

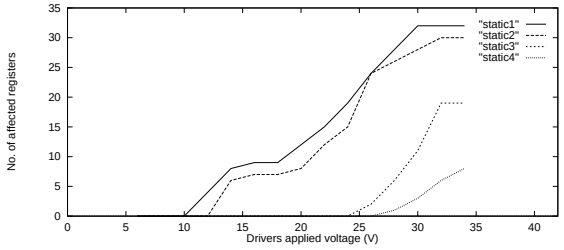

Fig. 11. The number of affected registers as a function of the driver power supply voltage for four clocking regimes (for static registers).

The received noise increases by less than 5% for static registers when the chip temperature is varied between 25°C and 55°C. This variation is even more insignificant for dynamic registers. For temperatures greater than 60°C, however, the proper operation of the circuit is significantly affected.

Under these test conditions, the noise tolerance of both the static and dynamic registers significantly deteriorates when the analog high power and digital grounds are connected off-chip. This behavior is due to the fact that for on-chip connected grounds, the internal nodes of the circuit are discharged to a positively biased ground level (due to the high switching currents). This voltage level can be sufficient to leave the circuit operational in the unaffected state once the switching process is complete. This effect is strongly dependent on the distribution of the analog high power and digital ground lines. Also, the bouncing of the high-power ground (due to the high switching currents) with respect to the digital ground generates extra noise due to a modulation effect of the gate voltage of the power driver.

Finally and not surprisingly, the generated noise increases as the number of drivers that are active increases. This behavior is experimentally shown in Fig. 12.

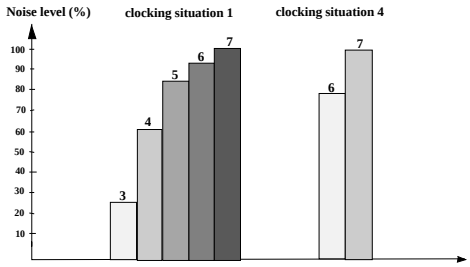

Fig. 12. The relationship between the active drivers (the numbers above each column) and the generated noise for the 1 and 4 clocking regimes and for static registers. The 100% noise level influence is relative, and is ≈ 30X smaller for clocking regime 4 as compared to clocking regime 1.

V. Conclusions

Fundamental questions with respect to the noise characteristics of digital circuitry in a smart power mixed-signal environment are answered. The behavior of the static and dynamic NMOS registers is analyzed under a variety of conditions. Multiple circuit and physical aspects, as well as temperature, power distribution, and clocking regimes, are experimentally analyzed and the behavior explained. Circuit, device, and physical design rules to minimize the effects of substrate coupling noise in high power mixed-signal systems are presently being developed based on the experimental data and related observations.

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