Power Grid Noise in TSV-Based 3-D Integrated Systems

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Abstract: *A 3-D test circuit examining power grid noise in a 3-D integrated stack has been designed, fabricated, and tested. Fabrication and vertical bonding were performed by MIT Lincoln Laboratory for a 150 nm, three metal layer SOI process. Three wafers are vertically bonded to form a 3-D stack. Noise analysis of a power delivery topology is described. The effect of the through silicon via (TSV) density on the noise profile of a 3-D power delivery network is also discussed.*

Keywords: 3-D integration; 3-D power delivery; PDN noise analysis

I. Introduction

An important issue for 3-D integrated circuits (ICs) is the design of a robust power distribution network that can provide sufficient current to every load within a system. In planar ICs where flip-chip packaging is adopted as the packaging technique, an array of power and ground pads is allocated throughout the surface of the integrated circuit. Increasing current densities and faster current transients, however, complicate the power distribution design process. Three-dimensional integration provides additional metal layers for the power distribution networks through topologies that are not available in two-dimensional circuits. With 3-D technologies, individual planes can potentially be dedicated to delivering power.

The challenges of efficiently delivering power across a 2-D circuit while satisfying local current requirements have been explored for decades [1]. Two-dimensional power distribution networks are designed to achieve specific noise requirements. A variety of techniques have been developed to minimize both *IR* drops and $L \cdot di/dt$ noise [2], [3], such as multi-tiered decoupling placement schemes [4]-[6] and power gating [7]. These techniques have been effective with increasing current demands of each progressive technology node. 3-D integrated systems however are in its infancy, and much work is required to design efficient power distribution topologies.

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Power delivery in 3-D integrated systems presents difficult new challenges for delivering sufficient current to each of the device planes. Stacking device planes in the vertical direction leads to higher power densities [8]. The effect of the increased power density on a 3-D power network is significant, as specialized design techniques are required to ensure that each device plane is operational, while not exceeding the target output impedance. This paper focuses on a primary issue in power delivery, the power distribution network, and provides a quantitative analysis of the noise measured on each plane of a three plane 3-D integrated stack.

An analysis of the effects of through silicon vias (TSVs) on *IR* voltage drops and $L \cdot di/dt$ noise is required, as the impedance of the power distribution network is affected by the TSV density. In addition, the impedance of a single TSV is considered as the electrical characteristics of a TSV vary based on the 3-D via diameter, length, and dielectric thickness [9]. A comparison of two different via densities for identical power distribution networks is also discussed in this paper, and implications of the 3-D via density on the power network design process is discussed.

The proper placement of decoupling capacitors can potentially reduce noise within the power network, while enhancing performance. The effect of board level decoupling capacitors on *IR* and $L \cdot di/dt$ noise in 3-D chip circuits is discussed here. Methods for placing decoupling capacitors at the interface between planes to minimize the effects of inter-plane noise coupling are also suggested.

The 3-D test circuit is described in the following section. A brief summary of the MITLL 3-D process is provided in Section III. Experimental results and a discussion of the noise characteristics of the power distribution networks are presented in Section IV. Some conclusions are offered in Section V.

II. Design of the 3-D power distribution networks

The test circuit consists of three blocks. Each block includes the same logic circuit but utilizes a different power distribution architecture. The total area of the test circuit is 2 mm x 2 mm, where each block occupies an

area of approximately 0.3 mm^2, representing a section of a full circuit power delivery network. Each block has a power supply voltage of 1.5 volts. The design kit developed at North Carolina State University was used in the design process [10]. The different power distribution architectures are reviewed in Section II-A, and the common logic circuitry within each power module is described in Section II-B.

A. 3-D power topologies

Interdigitated power/ground lines are used in all of the topologies. There are four main objectives for the test circuit: i) to determine the peak and average noise within the power and ground distribution networks, ii) to determine the effect that the board level decoupling capacitors have on reducing undesired noise, iii) to explore the effects of a dedicated power/ground plane on the power network noise, and iv) to investigate the effects of the TSV density on the noise characteristics of the power network. The three topologies are illustrated in Fig. 1 and address objectives (i) and (ii). Objective (iii) is achieved by comparing noise data from the topologies shown in Figures 1(b) and 1(c), while the two topologies shown in Figures 1(b) and 1(c) address objective (iv). The difference between the upper left and upper right topologies is the number of TSVs, where the latter topology includes 50% more TSVs. There are 1152 3-D vias located on the periphery of the power distribution network shown in Fig. 1 (a), whereas the topology shown in Figs. 1 (b) uses 2304 vias with additional TSVs inserted on the power lines crossing through the middle of the circuit block.

B. 3-D circuit architecture

Each test block includes identical circuitry. The basic logic blocks are shown in Fig. 2. Power supply noise generators deliver varying current to the power lines. These noise generators are placed on each plane of each power network topology. Voltage sense circuitry is included on all of the planes of each test block to measure the noise on both the power and ground lines. The second plane of the power delivery network, illustrated in Fig. 1 (c), does not include noise sense circuitry or noise generation circuitry as this plane is dedicated to power and ground. The voltage range and average voltage of the sense circuitry on each plane for each test block is described for the topology shown in Fig. 1.

III. 3-D IC fabrication technology

The manufacturing process developed by MITLL for fully depleted silicon-on-insulator (FDSOI) 3-D circuits is described in [11], [12]. The MITLL process is a wafer level 3-D 150 nm integration technology with up to three FDSOI 150 mm wafers bonded to form a 3-D circuit. The technology includes one polysilicon layer and three metal

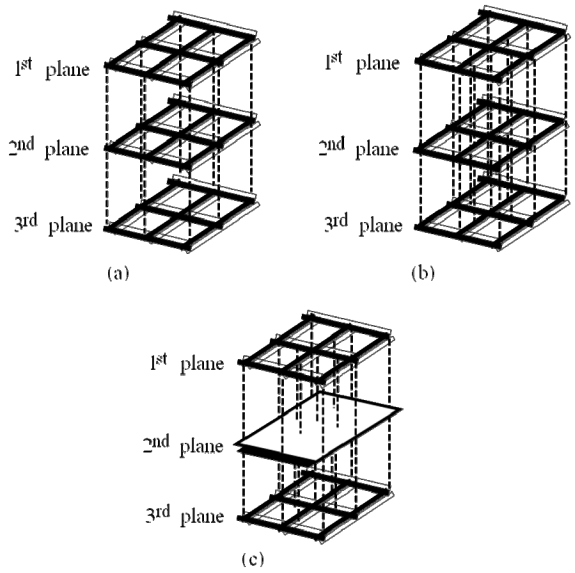

Figure 1: Power distribution network topologies. (a) interdigitated power network on all planes with the 3-D vias distributing current on the periphery, (b) interdigitated power network on all planes with the 3-D vias distributing current on the periphery and through the middle of the circuit, and (c) interdigitated power network on planes 1 and 2 and power/ground planes on plane 2 with the 3-D vias distributing current on the periphery.

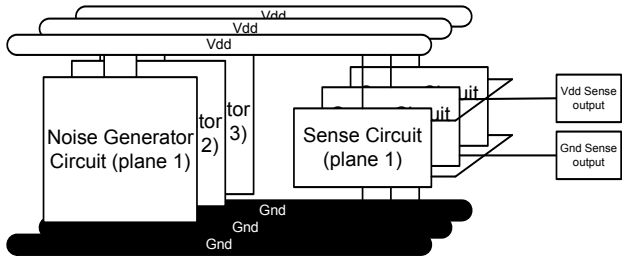

Figure 2: Circuit used to analyze power and ground noise.

layers interconnecting the devices on each wafer. A backside metal layer also exists on the upper two planes, providing the starting and landing pads for the TSVs, and the I/O, power supply, and ground pads for the overall 3-D circuit. An attractive feature of this process is the high density TSVs. The dimensions of these vias are 1.25 μm x 1.25 μm, much smaller than many existing 3-D technologies [13], [14]. An intermediate step of the fabrication process is illustrated in Fig. 3. As depicted in this figure, this process includes both face-to-face and face-to-back plane bonding. The SOI device layers are used for both monolithic [15] and wafer level 3-D integrated systems. SOI is an effective technology for 3-D circuits since the wafers can be aggressively thinned as compared to standard bulk CMOS technologies [16]. This capability results in significantly shorter TSVs, a critical issue in 3-D systems. The primary obstacle for 3-D SOI technologies is the high thermal resistance of the oxide which impedes the heat removal process [17]

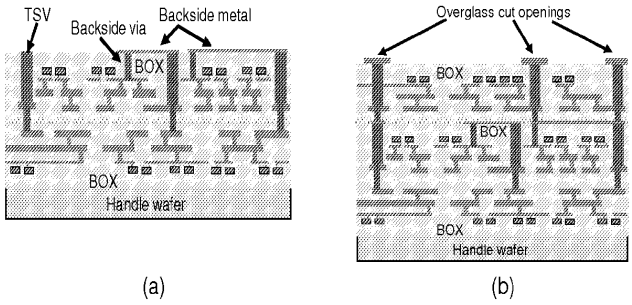

Figure 3: Cross-sectional schematic of a 3-D circuit based on the MITTLL process, (a) an intermediate step and (b) fully fabricated 3-D stack [11]. The second plane is flipped and bonded with the first plane, while the third plane is bonded face-to-back with the second plane. The backside metal layer and vias and the through silicon vias are also shown.

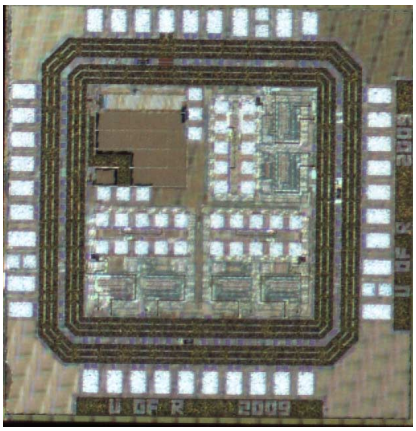

Figure 4: Fabricated test circuits examining three different power distribution networks and a distributed DC-to-DC power converter.

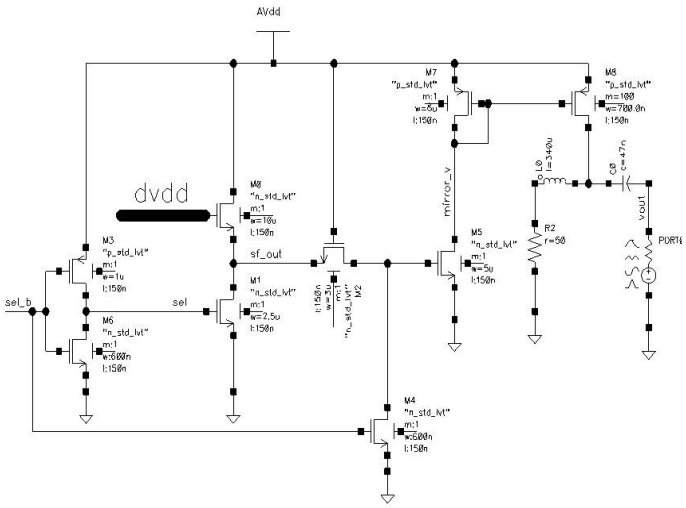

Figure 5: Source follower sense amplifier circuit used to detect noise on the digital power rail.

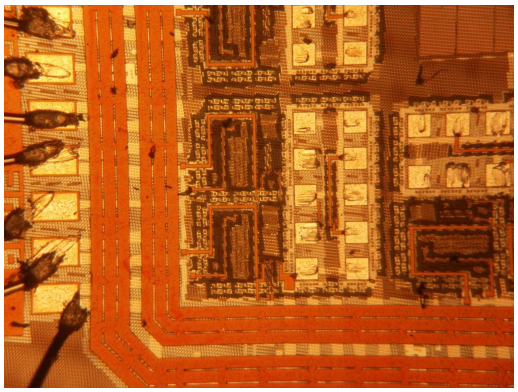

Figure 6: One quadrant of the test circuit examining noise on the power distribution network.

IV. Experimental results and analysis

The noise generated on the power distribution network is detected by a source follower based amplifier circuit. A schematic of the amplifier circuit is depicted in Fig. 5. Noise from the digital circuit blocks is coupled into the sense circuit through the node labeled *dvdd*. The gain of the circuit is controlled by adjusting the analog voltage, labeled as *AVdd* in Fig. 5.

A voltage is measured after the intrinsic capacitance of the bias junction that couples the noise into the oscilloscope and spectrum analyzer. The node at which the noise is detected is labeled *vout* in Figure 5. The noise voltage measurements for varying reference currents within the noise generation circuits, and varying values of AV_{dd} are listed in Table 1. The measurements listed in Table 1 are for the power distribution network depicted in Figure 1 (c). The other two topologies shown in Figure 1 are currently under test, and the resulting voltage measurements will be used to compare the three different power distribution topologies.

The measurements indicate that the total current drawn from the digital power distribution network remains approximately the same, ranging from 3.8 mA to 4.2 mA, despite the increasing reference current. The relative noise generated on the power distribution network, however, trends upward, as indicated by examining the DC and AC V_{rms} values and the peak-to-peak voltage $V_{p\text{-}p}$. Examining the $V_{p\text{-}p}$ noise for AV_{dd} = 1.5 V, as the reference current increases from 0 to 3.07 mA, $V_{p\text{-}p}$ trends upward from 25.5 mV to 33.3 mV. The maximum $V_{p\text{-}p}$ voltage is approximately 40 mV, as detected by the sense circuit for all values of the reference current and AV_{dd} bias conditions. This behavior is due to the source follower transistor switching into the triode region. The upward trend indicates that although less net current is drawn from the power supply, there is an increase in the peak-to-peak noise on the power rail. With regard to 3-D power delivery, the noise voltage at the output of the sense circuits is from all three device planes, but is not discerned from the resulting voltage waveform.

Table 1: Noise produced by the 3-D power distribution network within block 1 (see Figure 1(c)).

V_{dd} (V)	I_{vdd} (mA)	AV_{dd} (V)	I_{ref} (mA)	V_{max} (mV)		V_{min} (mV)		V_{p-p} (mV)		V_{rms} AC (mV)		V_{rms} DC (mV)	
				min	max	min	max	min	max	min	max	min	max
0	-0.6	1.5	0	0.615	1.40	-3.08	-2.34	3.06	4.22	0.52	0.57	0.82	0.87
1.5	4.2	1.3	0	7.97	19.6	-20.9	-6.70	19.5	40.3	1.33	1.52	1.34	1.63
1.5	4.0	1.5	0	11.57	19.7	-20.9	-10.3	25.5	40.4	2.18	2.34	2.09	2.43
1.5	3.8	1.7	0	19.3	19.3	-20.7	-20.7	40.0	40.0	-------	-------	4.67	6.49
1.5	4.2	1.3	0.82	7.36	19.6	-20.9	-6.87	17.9	40.4	1.34	1.57	1.36	1.67
1.5	4.0	1.5	0.81	13.5	19.7	-20.8	-12.9	32.2	40.4	2.46	2.57	2.42	2.76
1.5	3.9	1.7	0.81	19.3	19.3	-20.7	-20.7	40.0	40.0	-------	-------	4.70	5.42
1.5	4.1	1.3	1.51	6.81	19.5	-20.9	-6.3	16.4	40.2	1.31	1.47	1.34	1.63
1.5	4.0	1.5	1.51	12.4	19.5	-20.7	-11.8	31.1	40.2	2.29	2.39	2.22	2.61
1.5	3.8	1.7	1.51	19.3	19.3	-20.7	-20.7	40.0	40.0	-------	-------	4.99	6.48
1.5	4.2	1.3	2.23	7.07	19.7	-20.9	-6.95	17.1	40.4	1.34	1.56	1.38	1.65
1.5	4.1	1.5	2.23	13.7	19.6	-20.9	-11.9	30.8	40.3	2.44	2.56	2.26	2.88
1.5	3.85	1.7	2.23	19.3	19.3	-20.7	-20.7	40.0	40.0	-------	-------	4.59	5.62
1.5	4.2	1.3	3.07	4.92	19.7	-20.9	-4.7	12.7	40.4	1.49	1.74	1.49	1.87
1.5	4.0	1.5	3.08	15.5	19.7	-20.8	-14.0	33.3	40.4	2.88	3.12	2.66	3.55
1.5	4.0	1.7	3.07	19.3	19.3	-20.7	-20.7	40.0	40.0	-------	-------	4.79	6.62

V. Conclusions

The design of a power distribution network for application to 3-D circuits is considerably more complex than the design of a two-dimensional power network. Three topologies to distribute power within a 3-D circuit have been designed, and an analysis of the peak noise voltage, voltage range, and average noise for both power and ground is described for one of the topologies. The remaining two power distribution topologies are currently being measured, and will be used for comparison with the described topology.

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