

# Test Circuits for 3-D Systems Integration

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**Abstract**— Three test circuits have been developed to experimentally demonstrate and stress the state-of-the-art in 3-D integrated systems. Several critical elements of this emerging technology, synchronization, power delivery, and thermal management, are just beginning to be explored. The three test circuits explore these three fundamental design issues. The first test circuit examines multi-plane synchronization for a stacked system of three device planes. Experimental data compare skew, slew, and power consumption for different network topologies. The second test circuit examines power delivery in a three plane 3-D system. The noise propagation characteristics within the power and ground networks are experimentally assessed by varying the through-silicon via (TSV) density and using dedicated planes. The third 3-D circuit includes five CMOS planes, two logic planes and three memory planes, and includes multiple circuits that examine a range of 3-D design issues. The test structures are designed to evaluate thermal coupling between CMOS device planes and decoupling capacitance in 3-D power delivery networks. These test circuits are discussed, and trends and challenges are outlined.

**Index Terms**— 3-D integration, clock distribution, noise propagation, power distribution, thermal coupling, decoupling capacitor placement.

## I. INTRODUCTION

Three of the most omnipresent and challenging issues in high performance 3-D systems are synchronization, power delivery, and thermal management. The interdependence of these issues is of critical importance in 3-D systems, as noise on the power network can adversely affect the clock network, current loads can produce severe hot spots within a 3-D stack, and the location of the hot spots can adversely affect multiplane synchronization. Enhanced understanding of these interrelated 3-D design challenges is therefore necessary to develop design techniques and methodologies to effectively deliver clock and power while managing thermal effects.

Each of these three individual topics is examined independently through three recent test circuits. The first test circuit examines the effects of the clock delivery topology on the clock skew at the leafs of each device plane and is shown in Fig. 1a. The second test circuit focuses on power delivery in 3-D integrated systems. The objective of this test circuit is to provide a quantitative analysis of the

noise characteristics of each plane within a three plane 3-D integrated system. A microphotograph of the second test circuit is shown in Fig. 1b. The third test circuit has been designed to examine cross-plane thermal coupling between adjacent device planes. Thermal effects can potentially alter the performance of the clock and power networks due to hot spots. A microphotograph of the third test circuit is shown in Fig. 1c.

In the following section, the test circuit examining clock delivery in 3-D systems is discussed. This section is followed by a discussion of the 3-D power delivery test circuit in Section III. A description of the third test circuit examining cross-plane thermal coupling and decoupling capacitor placement is provided in Section IV. Some conclusions are offered in Section V.

## II. CLOCK DISTRIBUTION IN 3-D SYSTEMS

The reliable distribution of the clock signal to the many hundreds of thousands of sequential elements distributed throughout a synchronous circuit [1], [2] is further exacerbated in 3-D ICs as sequential elements belonging to the same clock domain can be located on multiple planes. In 2-D circuits, symmetric interconnect structures are widely used to distribute the clock signal across a circuit [2], permitting the clock signal to arrive at the leaves of the tree at approximately the same time. Maintaining this symmetry within a 3-D circuit, however, is a difficult task. This first test circuit on multiplane synchronization has provided insight into the benefits and challenges of asymmetric clock structures in 3-D circuits.

Three topologies to globally distribute a clock signal within a 3-D circuit have been evaluated. A 3-D test circuit, based on the MITLL 180 nm CMOS 3-D manufacturing process with 1.75  $\mu\text{m}$  diameter TSVs [3], is experimentally demonstrated to operate at 1.4 GHz [4].

The test circuit consists of three blocks. Each block includes the same logic circuit but implements a different clock distribution topology. The total area of the test circuit is 3 mm  $\times$  3 mm, where each block occupies an approximate area of 1 mm<sup>2</sup>. Each block contains about 30,000 transistors with a power supply voltage of 1.5 volts. The different clock distribution topologies are reviewed in Section II-A, and experimental results are discussed in Section II-B.

### A. 3-D clock topologies

Several clock network topologies for 3-D ICs are described in this section. These topologies are commonplace in 2-D

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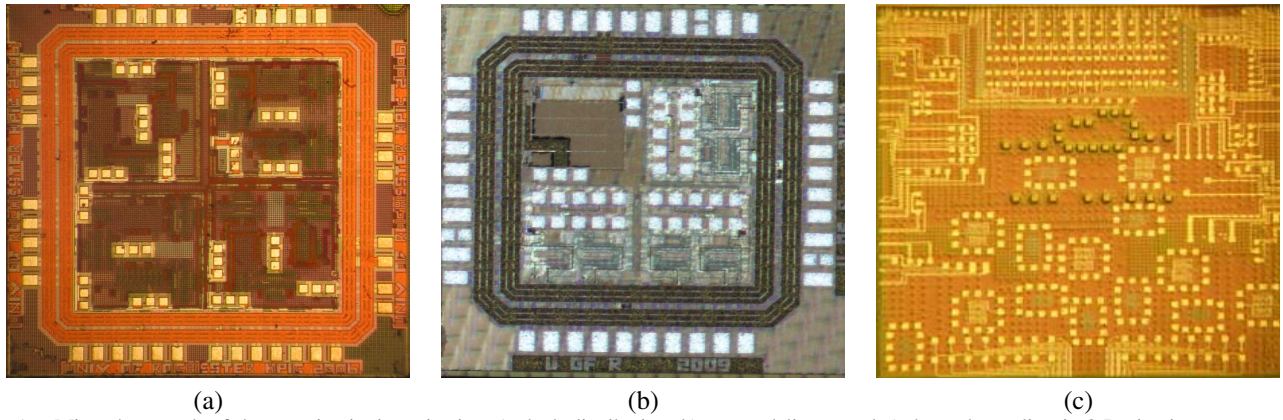


Fig. 1. Microphotograph of the test circuits investigating a) clock distribution, b) power delivery, and c) thermal coupling in 3-D circuits.

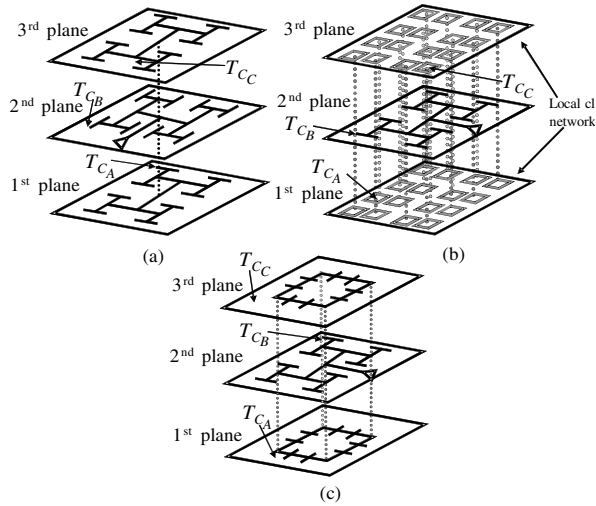


Fig. 2. Three 3-D clock distribution networks within the test circuit, (a) H-trees, (b) H-tree and local rings, and (c) H-tree and global rings.

circuits, such as H-trees, rings, and meshes [2]. Each of the three blocks includes a different clock distribution structure, which is schematically illustrated in Fig. 2. The dashed lines depict vertical interconnects implemented by groups of through silicon vias. Multiple TSVs at the connection points between the clock networks lower the resistance of the vertical path while enhancing reliability.

A primary objective is to evaluate the effects of the TSVs on clock skew. Load balancing the global rings is shown to reduce the delay of the clock signal due to the TSVs. Local meshes are preferable since the distribution of the clock signal to the sinks is limited within a physical plane. Stacks of TSVs connect the sinks on other planes through local rings. This topology offers the advantage of limiting most of the clock paths within one physical plane, while distributing the signal vertically to localized areas within neighboring planes.

The effects that these topological choices have on the clock skew are experimentally described in Table I. Equidistant signal propagation in a 3-D system is complicated by the different impedance characteristics of the vertical and horizontal interconnects. Consequently, the objective is to provide a global clock topology that produces sufficiently low skew (or

TABLE I  
CLOCK SKEW AMONG THE PLANES OF EACH BLOCK AND THE AVERAGE POWER CONSUMED BY EACH TOPOLOGY.

Clock distribution network	Average power (mW)	Clock skew (ps)	Frequency (MHz)				
			10	40	160	500	1000
H-tree (Fig. 2a)	260.5	$t_{BA} = t_B - t_A$	59.0	59.7	—	18.7	26.2
		$t_{BC} = t_B - t_C$	66.8	88.5	—	20.1	30.2
		$t_{AC} = t_A - t_C$	7.8	28.8	—	1.4	4.1
Local rings (Fig. 2b)	228.5	$t_{BA} = t_B - t_A$	122.5	82.3	70.0	159.1	112.1
		$t_{BC} = t_B - t_C$	70.8	48.9	38.0	144.5	131.1
		$t_{AC} = t_A - t_C$	51.7	33.4	32.0	14.5	19.1
Global rings (Fig. 2c)	168.3	$t_{BA} = t_B - t_A$	—	23.6	30.4	—	68.3
		$t_{BC} = t_B - t_C$	—	38.2	42.2	—	18.6
		$t_{AC} = t_A - t_C$	—	14.6	11.8	—	49.7

predictable skew for delay compensation) within (intra-plane) and among (inter-plane) the planes of a 3-D circuit. The symmetry of an H-tree and the load balancing characteristics of the rings and meshes are exploited. The power consumed by each 3-D clock architecture is also considered due to the importance of thermal issues in 3-D circuits.

### B. Experimental results

The clock skew between the planes of each block is listed in Table I. The difference in the arrival time of the clock signal between planes  $i$  and  $j$  is denoted as  $t_{ij}$ , and represents the clock skew between these two locations. The average power consumed by the buffers for each clock distribution topology is also listed in Table I.

The clock skew measurements indicate that a topology combining the symmetry of an H-tree on the second plane and global rings on the remaining two planes results in low clock skew in 3-D circuits while consuming a moderate amount of power. This structure, however, produces the greatest root to leaf clock delay as compared to the other topologies. Alternatively, for the H-tree and local rings topologies, the lowest power is consumed.

### III. POWER DELIVERY FOR STACKED TECHNOLOGIES

Power distribution networks for 3-D systems are naturally more complex than a two-dimensional power network. In addition, power delivery in 3-D integrated systems presents difficult new challenges for delivering sufficient current to each device plane [5], while leading to high power densities

[6]. Specialized techniques are therefore required to ensure that each device plane is operational, while not exceeding a target output impedance [7]. The  $IR$  voltage drops and  $L \cdot di/dt$  switching noise are affected by the density and electrical characteristics of the TSVs [8]. A comparison of two different via densities for identical power distribution networks is presented, and the effects of the 3-D via density on the power network design process are discussed.

The fabricated test circuit is  $2 \text{ mm} \times 2 \text{ mm}$ , and composed of four equal area quadrants (see Fig. 1b). Three quadrants are used to evaluate the effects of the power distribution network topology on the noise propagation characteristics, and one quadrant is dedicated to DC-to-DC conversion. Each stacked power network is  $530 \mu\text{m} \times 500 \mu\text{m}$ , and includes three discrete two-dimensional power networks, one network on each of the three device planes. The total area occupied by each block is less than  $0.3 \text{ mm}^2$ , representing a portion of a power delivery network. Each block includes the same logic circuit but utilizes a different power distribution architecture. The power supply voltage is 1.5 volts for all of the blocks. The third MITLL 3-D multi-project wafer includes  $1.25 \mu\text{m}$  diameter TSVs, and CMOS devices with channel lengths of 150 nm. The different power distribution topologies are reviewed in Section III-A, and experimental results are provided in Section III-B.

### A. 3-D power topologies

Three topologies to distribute power within a 3-D circuit have been designed and manufactured, and an analysis of the peak noise voltage, voltage range, and average noise for the power and ground network is described. Interdigitated power/ground lines are used in all of the topologies. The four main objectives for the test circuit are to i) determine the peak and average noise within the power and ground distribution networks, ii) determine the effects of the board level decoupling capacitors on reducing undesired noise, iii) explore the effects of a dedicated power/ground plane on the power noise, and iv) investigate the effects of the TSV density on the noise characteristics of the power network. The three power network topologies are illustrated in Fig. 3. The difference between the left (Block 1) and central (Block 2) topologies is the number of TSVs, where the latter topology contains 50% more TSVs. The third topology (Block 3) replaces the interdigitated power and ground lines on the second device plane with two metal planes to evaluate the benefit of dedicated power and ground planes on delivering current within a 3-D system.

### B. Experimental results

The peak noise for each topology, with or without a board level decoupling capacitance, is shown in Fig. 4. No single topology contributes the largest noise voltage at any specific bias voltage. The average noise for each topology is approximately 75% to 90% lower than the peak-to-peak voltage, indicating that a majority of the data is located within close proximity of the nominal power and ground voltages.

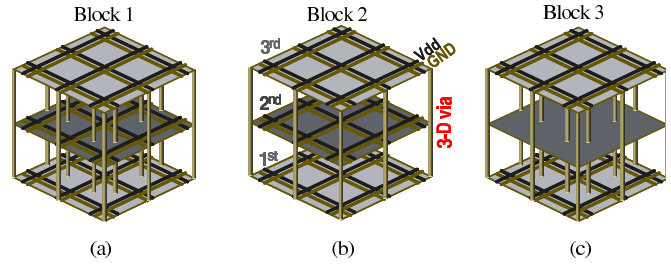


Fig. 3. Power distribution network topologies. (a) interdigitated power network on all planes with the 3-D vias distributing current on the periphery and through the middle of the circuit, (b) interdigitated power network on all planes with the 3-D vias distributing current on the periphery, and (c) interdigitated power network on planes 1 and 3 and power/ground planes on plane 2 with the 3-D vias distributing current on the periphery and through the middle of the circuit.

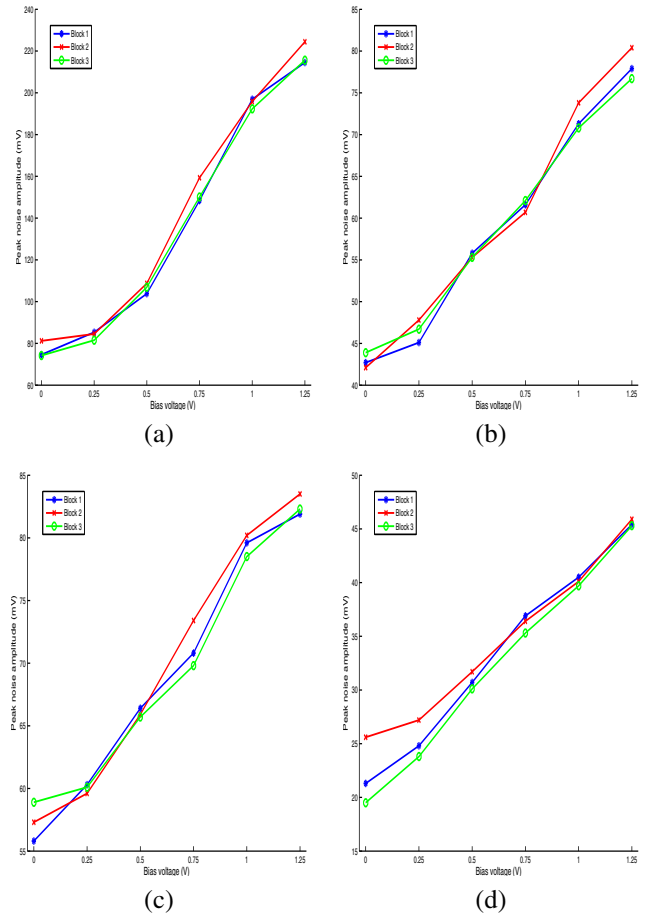


Fig. 4. Peak noise voltage on the power and ground distribution networks with and without board level decoupling capacitance. (a) peak noise of power network without decoupling capacitance, (b) peak noise of power network with decoupling capacitance, (c) peak noise of ground network without decoupling capacitance, and (d) peak noise of ground network with decoupling capacitance.

In addition, the saturation voltage of the detection circuitry at the output node (port0) is approximately 230 mV when the gain is  $-4.2 \text{ dB}$ . The noise detection range is approximately 600 mV centered around 1.5 volts and 0 volts, respectively, for the power and ground lines. The detection circuits for the power network, therefore, detect noise that ranges from 1.2 volts to 1.8 volts, and for the ground networks from  $-0.3$  volts to 0.3 volts.

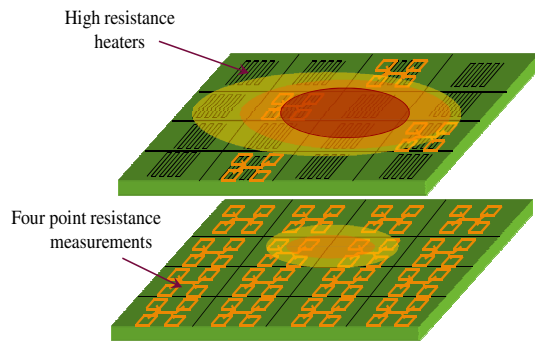


Fig. 5. Test structure to evaluate cross-plane thermal coupling including resistive thermal sources and four-point resistance measurement based thermal sensors.

#### IV. THERMAL COUPLING IN 3-D INTEGRATED SYSTEMS

The third test circuit has been fabricated by Tezzaron Semiconductor in a 130 nm CMOS technology with 1.2  $\mu\text{m}$  diameter TSVs. The test structures have been developed to evaluate thermal coupling between adjacent planes and decoupling capacitor placement within a 3-D system. This test circuit was designed to better understand the effect of inter- and intra-plane thermal resistances on hot spot formation. The test structures that investigate thermal coupling between adjacent planes include both thermal sources and thermal sensors, as shown in Fig. 5. Each thermal source is paired with a thermal sensor on an adjacent metal level, and these pairs are distributed throughout each plane within a 3-D stack. The thermal sources are heater resistors with a target resistance of 8 ohms and a maximum applied voltage of 40 volts. The temperature sensor provides a calibrated four-point measurement tested with a low current to avoid joule heating.

The test circuit on decoupling capacitor placement evaluates the effect of board level decoupling capacitors on  $IR$  and  $L-di/dt$  noise in 3-D circuits. A schematic diagram of the four topologies used to analyze decoupling capacitor placement is depicted in Fig. 6. The first two topologies do not include an on-chip decoupling capacitor. The structure pictured in Fig. 6(b) includes a board level capacitor. Test structures with on-chip capacitors are shown in Figs. 6(c) and 6(d). The larger capacitors shared between the two planes are depicted in Fig. 6(c), and a more standard 2-D approach to decoupling capacitor placement where localized point-of-load capacitors are distributed within each plane is shown in Fig. 6(d).

#### V. CONCLUSIONS

Three test circuits examining the critical physical design issues in 3-D systems are reviewed in this paper. Test data examining clock and power distribution networks in 3-D integrated circuits indicate that the choice of 3-D topology greatly affects the skew and noise propagation characteristics, respectively, of clock and power networks. The third test circuit on intra- and inter-plane thermal coupling is currently being fabricated, and is expected to produce insight into thermal management methodologies and decoupling capacitor relocation algorithms.

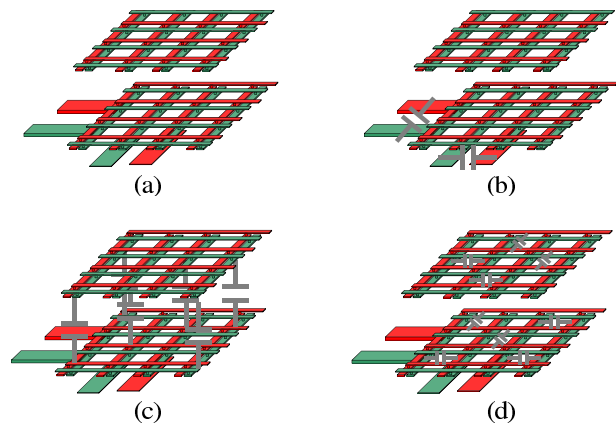


Fig. 6. Schematic diagram of test circuit examining decoupling capacitor placement for a) no decoupling capacitors, b) board level decoupling capacitors, c) inter-plane shared capacitors, and d) point-of-load decoupling capacitors.

3-D integration requires clock and power topologies that are infeasible in 2-D circuits. The ability of 3-D integrated circuits to dedicate multiple planes to the clock or power network supports the development of novel clock and power topologies, permitting die area and metal resources to be strategically allocated. As demonstrated by the experimental data described in this paper, a topology incorporating power and ground planes reduces the maximum noise voltage within a power network by 2% to 18% as compared to more standard interdigitated structures. The experimental data also verify that the block with an H-tree topology on all three device planes produces the lowest skew between planes at the expense of increased power consumption. The topology with H-trees on all three planes operates at 1.4 GHz, the highest frequency of the three clock topologies.

The interdependencies among synchronization, power delivery, and thermal management in 3-D systems demand greater attention. These test circuits provide experimental insight to enhance the development of next generation 3-D integrated circuits.

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