Noise Coupling in TSV-Based Heterogeneous 3-D ICs

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***Abstract*— The evaluation and analysis of noise coupling in TSV-based heterogeneous 3-D ICs is presented in this paper. Both TSV-to-substrate and TSV-to-TSV coupling noise are discussed. Models of capacitive coupling from the TSVs into the heterogeneous substrate are presented. The accuracy of the noise coupling models is evaluated in the time domain, and the effects of the ground network impedance on the sensitivity of the victim devices is determined. Topologies for TSV bundles are compared in terms of TSV-to-TSV capacitive and inductive noise.**

I. INTRODUCTION

A three-dimensional (3-D) structure is an effective platform for integrating heterogeneous circuits within a single system, as illustrated in Figure 1. Each layer of a 3-D integrated circuit (IC) is typically independently fabricated using different substrate materials for different applications. The 3-D structure is a natural platform for modern diverse applications including mobile and wearable devices.

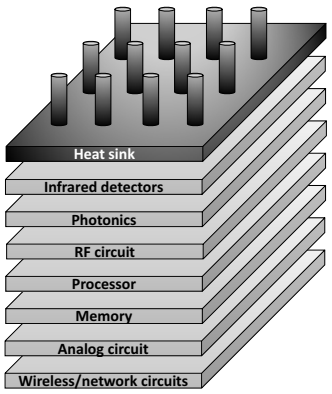

Fig.1. Heterogeneous 3-D integrated circuit.

Noise coupling is a key issue in IC design [1], [2]. This issue is aggravated in 3-D circuits since multiple layers (each with an individual substrate) are placed above each other, allowing signals to propagate across the 3-D structure. Through substrate vias (TSVs) connect the different layers within the 3-D system, carrying power, clock, and data. TSVs, a seminal component of 3-D technology, are short vertical interconnections between the different layers that can support global signaling requirements [3]. TSVs penetrate the substrate of a layer and connect to either the first or last metal within that layer [4]. Typical TSV dimensions are 20 μm in length and 2 μm in diameter [5]. Similar to two-dimensional (2-D) substrate coupling, the signals within the TSVs can couple capacitive and inductive noise into the substrate, affecting nearby victim circuits or other TSV signals.

The rest of the paper is composed of the following sections. Compatible substrate materials are reviewed in Section II. Noise coupling for TSV-to-substrate and TSV-to-TSV scenarios is evaluated in, respectively, Sections III and IV. Some conclusions are offered in Section V.

II. 3-D SUBSTRATE CHARACTERISTICS

The electrical resistivity and thermal conductivity of different substrate material used in common ICs are listed in Table I. Some commonly used materials in modern integrated circuits are silicon (Si), gallium arsenide (GaAs), germanium (Ge), and mercury cadmium (MerCad) telluride (HgCdTe) [6]–[8]. The electrical resistivity of the substrate materials is a key parameter in noise coupling. Therefore, due to the wide range of resistivities, as listed in Table I, an individual noise coupling mode for each of the substrate materials is required. Previous work has addressed noise coupling from the TSVs into the substrate and adjacent TSVs in *homogeneous* circuits (processor/memory stacks), typically on a silicon substrate [9], [10] rather than *heterogeneous* systems.

Each of the substrate materials listed in Table I is beneficial for a specific circuit application. Si is typically lower cost and more mature as compared to the other materials and therefore used for mainstream processor and memory applications. The superior electron mobility of GaAs makes it attractive for high performance analog devices. Ge is a favorable substrate material for photovoltaic and photodetector applications due to the high absorption coefficient of Ge. Military and space application that require high quality infrared detectors commonly use HgCdTe [11] which has a tunable bandgap ranging from 0.1 eV to 1 eV. This property of HgCdTe supports detection of long wavelength light.

TABLE I
COMMON CIRCUITS AND COMPATIBLE SUBSTRATE TYPES

Applications	Substrate materials	Electrical resistivity $\Omega \cdot$ cm	Thermal conductivity $\frac{W}{m^\circ C}$
Processor/ memory	Silicon (Si)	1 to 10	138
RF/analog	Gallium Arsenide (GaAs)	$4 \cdot 10^7$	40
Photonics	Germanium (Ge)	$1 \cdot 10^{-3}$	45
Space applications/ detectors	Mercury Cadmium Telluride (HgCdTe)	2	0.2

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TABLE II

COMPARISON OF LUMPED, DISTRIBUTED, AND SHORT-CIRCUIT MODELS FOR SI, GAAS, GE, AND HGCDTE SUBSTRATES FOR DIFFERENT GROUND NETWORK INDUCTANCES

Model	Ground inductance nH	Si		GaAs		Ge		HgCdTe	
		Peak noise mV	Settling time nsec	Peak noise mV	Settling time nsec	Peak noise mV	Settling time nsec	Peak noise mV	Settling time nsec
Short-circuit	0.1	-	-	-	-	11.1	0	-	-
	1	-	-	-	-	645.5	1.46	-	-
	10	-	-	-	-	954.4	8	-	-
Lumped	0.1	159.8	1.57	$3.8 \cdot 10^{-8}$	0	8.5	0	152	0.36
	1	162.4		$3.8 \cdot 10^{-8}$		638.5	1	162.9	0.36
	10	186.3		$3.8 \cdot 10^{-8}$		950.8	6	276.2	0.31
Distributed (3 sections)	0.1	161.8	1.55	$3.9 \cdot 10^{-8}$	0	8.7	0	153.9	0.36
	1	164.5		$3.9 \cdot 10^{-8}$		637.5	1	164.8	0.4
	10	188.6		$3.9 \cdot 10^{-8}$		950.1	6	279.3	0.31

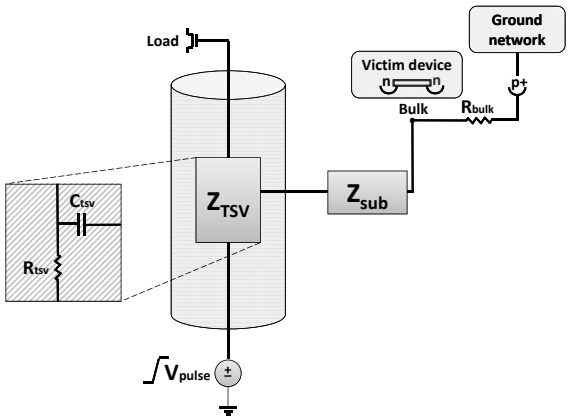

Fig.2. Electrical model of TSV-to-substrate noise coupling.

III. TSV-TO-SUBSTRATE NOISE COUPLING

A model for noise coupling from a TSV into the surrounding substrate is depicted in Figure 2 [12]. This model includes the impedance of the substrate Z_{sub} which varies with the particular substrate material. For Si and HgCdTe, $Z_{sub} = R_{Si/HgCdTe}$, the resistance of the Si and HgCdTe substrate. For Ge and GaAs, however, Z_{sub} becomes, respectively, zero (a short circuit) and infinite (an open circuit). The element Z_{TSV} characterizes the resistance of the TSV and the coupling capacitance from the TSV into the substrate. In the example shown in Figure 2, a lump model of Z_{TSV} is presented; however, a distributed model with three identical sections (three Z_{TSV} elements connected in series) is also evaluated.

A comparison of a lumped model versus a distributed model with three sections is listed in Table II for Si, GaAs, Ge, and HgCdTe. For Ge, a third "short-circuit" model ($Z_{sub} = 0$) is also compared. This model, therefore, only exhibits a coupling capacitance from the TSV to the substrate [13]. The models are evaluated using SPICE with a 10 ps input ramp from 0 to 1 volt (Vpulse) applied to simulate switching by the aggressor digital circuits. The voltage is evaluated at the victim node. Both the peak noise voltage and settling time (2% of the final value) are evaluated for three different ground network inductances.

The error of the lumped model as compared to the distributed model for Si is 1.2%. A lumped model can therefore be used to accurately characterize a silicon substrate. As observed from the results listed in Table II, the inductance of the ground network can significantly affect the peak noise voltage. A worst case difference (from 0.1 to 10 nH) of 26.5 mV (14.2%) is noted.

The peak noise voltage for both a lumped and distributed model for GaAs is in the range of picovolts and is, therefore, negligible in most applications. The proposed model in this case is an "open circuit" model ($Z_{sub} = \infty$) that ignores the capacitive coupling. Also observed from Table II is that the inductance of the ground network has no effect on the peak noise voltage. This behavior is due to the resistivity of the substrate, which is sufficiently large to shunt the inductance of the ground network.

The accuracy of the short-circuit, lumped, and distributed models is listed in Table II. Ge is highly dependent on the inductance of the ground network. Comparing the lumped and distributed models, a distributed model provides negligible improvement in accuracy as compared to a lumped model. The worst case difference in peak noise voltage is 0.2 mV (2.3%), while the settling time is similar. The lump model, which incorporates fewer nodes, is therefore preferable. The short-circuit model deviates from the lump model by 2.6 mV (23.4%) and 2 nsec (25%) for, respectively, the peak noise voltage and settling time. A lump model, similar to the model for silicon, should therefore be used. If the circuit specifications are not particularly strict (a higher peak noise voltage and longer settling times are allowed), a short-circuit model can be used to reduce computational time.

For a HgCdTe substrate, the deviation of peak noise in the lump model as compared to the distributed model is 1.2%. Both models exhibit a similar settling time. A lump noise coupling model should therefore be used for a HgCdTe substrate material. Similar to the Ge substrate, the inductance of the ground network can significantly increase the peak noise coupled into the HgCdTe substrate.

IV. TSV-TO-TSV NOISE COUPLING

The evaluation of coupling among TSVs within a bundle of TSVs is presented in this section. Both capacitive and inductive coupling are considered. These TSV bundles typically carry logically related multiple signals (*e.g.*, a multi-bit

data bus) or uniformly distributed power/ground lines between layers [14]. Alternatively, a TSV bundle may be used to transfer a single signal surrounded by shielding TSVs. In this case, the primary signal could be a clock signal, a signal within a critical path, or a highly sensitive analog signal.

The standard structure of a basic TSV bundle is a three by three mesh topology, as shown in Figure 3(a), where p is the pitch. This basic topology can be replicated for larger TSV bundles (*e.g.*, five by five, seven by seven). The structure shown in Figure 3(a) however is not completely symmetric. While the distance from the TSV in the center to the four TSVs in the middle of the horizontal and vertical axes is p, the distance from the TSV in the center to the four TSVs on the two diagonal axes (the corner TSVs) is $\sqrt{2}p$. This structure is replicated in larger TSV bundles, making modeling and parasitic extraction of these TSV bundles challenging. Alternatively, the basic hexagonal TSV bundle, as shown in Figure 3(b)), is fully symmetric [15]. This symmetry is maintained in larger TSV bundles. The hexagonal bundle has six edges and the number of TSVs on each edge is n. In the example shown in Figure 3(b), a hexagonal bundle with $n = 1$ is depicted.

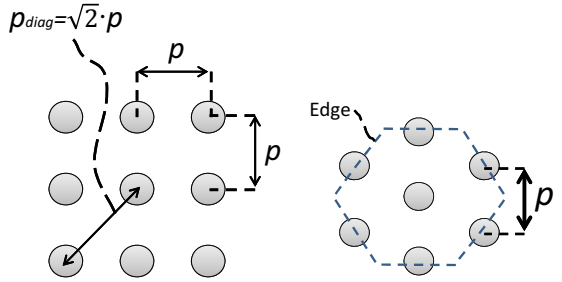

Fig.3. Top view of TSV bundle topologies. (a) Mesh, and (b) hexagonal bundle.

The minimum pitch between any two adjacent TSVs within both the mesh and hexagonal topologies, shown, respectively, in Figures 3(a) and 3(b), is p. The number of TSVs within an n-by-n mesh bundle is n^2. The number of TSVs within a hexagonal bundle N_{hexa} with n TSVs on each edge is

$$N_{hexa} = 1 + 6 \cdot \sum_{i=1}^{n} (3i - 2) \quad . \tag{1}$$

A. Capacitive coupling

Characterization of the coupling capacitance enhances noise coupling analysis and parasitic extraction within 3-D integrated circuits. An electrical model of the capacitive coupling with respect to a reference TSV for both the basic mesh and hexagonal TSV bundles is depicted in Figure 4. The reference TSV T_{ref} is the center TSV in each bundle topology; specifically, TSV number 5 in the mesh topology and TSV number 7 in the hexagonal topology. The coupling capacitance of a basic TSV bundle C_{bundle} is the total capacitive coupling from the surrounding TSVs within a bundle to the reference

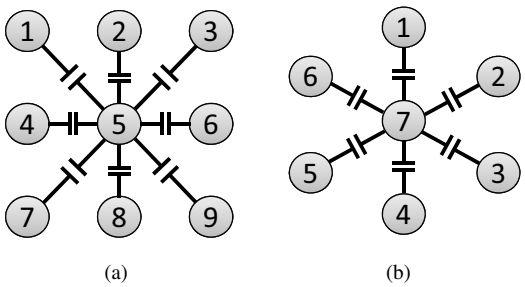

Fig.4. Capacitive coupling within basic TSV bundles for (a) mesh, and (b) hexagonal topologies.

TSV. Two types of coupling capacitance (with respect to T_{ref}) exist within a mesh bundle, (1) from the TSVs on the horizontal and vertical axes of the bundle, and (2) from the TSVs at the corners of the bundle. As depicted in Figure 4(a), these capacitances are, respectively,

$$C_{1,T_{ref}} = C_{3,T_{ref}} = C_{7,T_{ref}} = C_{9,T_{ref}} \triangleq C_{diag}^{mesh} \tag{2}$$

$$C_{2,T_{ref}} = C_{4,T_{ref}} = C_{6,T_{ref}} = C_{8,T_{ref}} \triangleq C_{orth}^{mesh} \quad . \tag{3}$$

Due to the natural symmetry within the hexagonal bundle, the coupling capacitance (with respect to T_{ref}) is identical for all of the surrounding TSVs, as depicted in Figure 4(b). The coupling capacitance to T_{ref} from all of the surrounding TSVs for the basic hexagonal bundle is

$$\begin{aligned} C_{1,T_{ref}} =& C_{2,T_{ref}} = C_{3,T_{ref}} = C_{4,T_{ref}} \\ =& C_{5,T_{ref}} = C_{6,T_{ref}} \triangleq C^{hexa} \quad . \end{aligned} \tag{4}$$

The coupling capacitance of the mesh and hexagonal topologies is, therefore, respectively,

$$C_{bundle}^{mesh} = \sum_{i=1}^{8} C_{i,T_{ref}} = 4(C_{diag}^{mesh} + C_{orth}^{mesh}) \tag{5}$$

$$C_{bundle}^{hexa} = \sum_{i=1}^{6} C_{i,T_{ref}} = 6 \cdot C^{hexa} \quad . \tag{6}$$

The capacitive coupling between the TSVs is a strong function of the pitch between the TSVs. To compare the mesh and hexagonal bundle topologies in terms of capacitive coupling, a relationship in terms of the pitch is required. A closed-form expression for the coupling capacitance between two TSVs, previously described in [5], is approximated to characterize the coupling capacitance in terms of the pitch p between two TSVs,

$$C_c = 7 \cdot 10^{-22} p^{-1.398} \quad . \tag{7}$$

As depicted in Figure 3(a), $p_{diag} = \sqrt{2}p$. Substituting this expression into (7) reveals the relationship between C_{diag}^{mesh} and C_{orth}^{mesh},

$$\begin{aligned} C_{diag}^{mesh} =& 7 \cdot 10^{-22} (p_{diag})^{-1.398} = 7 \cdot 10^{-22} (\sqrt{2}p)^{-1.398} \\ =& (\sqrt{2})^{-1.398} 7 \cdot 10^{-22} p^{-1.398} = 0.616 \cdot C_{orth}^{mesh} \quad . \end{aligned} \tag{8}$$

TABLE III
INDUCTANCE OF THE MESH AND HEXAGONAL TSV BUNDLES.

Bundle topology	Number of TSVs in bundle	Total mutual inductance [pH]	Average mutual inductance [pH]
Mesh	9	-3.06	-0.383
	25	-3.65	-0.152
Hexagonal	7	$-1.4 \cdot 10^{-3}$	$-2.33 \cdot 10^{-4}$
	31	$5.54 \cdot 10^{-2}$	$1.85 \cdot 10^{-3}$

The coupling capacitance between any two TSVs with pitch p is the same regardless of the topology. Therefore, $C_{orth}^{mesh} = C^{hexa}$. Substituting (8) into (5) yields

$$\begin{aligned} C_{bundle}^{mesh} =& 4(0.616 \cdot C_{orth}^{mesh} + C_{orth}^{mesh}) \\ =& 6.464 \cdot C_{orth}^{mesh} = 6.464 \cdot C^{hexa} \quad . \end{aligned} \tag{9}$$

Finally, from (6), a comparison between the coupling capacitance of the mesh and hexagonal bundles is

$$C_{bundle}^{hexa} = 0.93 \cdot C_{bundle}^{mesh} \quad . \tag{10}$$

The coupling capacitance of the hexagonal topology is therefore 7% smaller than the coupling capacitance of the standard mesh topology.

B. Inductive coupling

The average mutual inductance L_{mutual}^{avg} is the total mutual inductance from all of the surrounding TSVs within the bundle to the reference TSV (excluding the self-inductance of the reference TSV in the center of the bundle) divided by the number of surrounding TSVs. The average mutual inductance is used here as a figure of merit to compare the size and topology of the two types of TSV bundles.

The total inductance of a TSV bundle for both a mesh and hexagonal topology has been numerically evaluated using Ansys Q3D Extractor. The mesh bundle is a 5 by 5 structure, while the hexagonal bundle has two TSVs on each edge ($n = 2$). Both bundles consist of uniformly distributed power and ground TSVs. The total number of TSVs in the mesh bundle is $5^2 = 25$. For the hexagonal bundle and from (1) for $n = 2$, the total number of TSVs is 31. These TSV bundles consist of TSVs with a radius of 1 μm, length of 20 μm, and copper material. A minimum pitch of 10 μm is used for both bundle topologies. A comparison of the inductive properties between the mesh and hexagonal TSV bundle topologies is listed in Table III. The total and average mutual inductance of the hexagonal topology are both approximately two to three orders of magnitude lower than the mesh topology. The reduction in mutual inductance is due to the symmetry of the hexagonal bundle. For each power TSV there is a ground TSV. The power and ground TSVs carry current in opposite directions, effectively canceling the mutual inductance with respect to the reference TSV. This trait significantly reduces delay uncertainty caused by the mutual inductance.

V. CONCLUSIONS

Noise coupling in heterogeneous TSV-based 3-D ICs is characterized in this paper. TSV-to-substrate peak noise is evaluated for different substrate materials, and compatible circuit models are determined. Lump models are compatible for medium range resistance substrates such as Si and HgCdTe, while for the highly resistive GaAs substrate, the coupling noise can be ignored. In Ge, a low resistivity substrate, the noise easily couples into the victim. A short-circuit model should therefore be used. TSV-to-TSV coupling noise within TSV bundles is also evaluated. Capacitive and inductive coupling noise are compared for the mesh and hexagonal bundle topologies. The hexagonal topology exhibits 7% lower capacitive coupling noise than the mesh topology. The hexagonal topology exhibits superior inductive coupling characteristics, up to three orders of magnitude lower total mutual inductance than the mesh topology.

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