Passivity-Based Automated Design of Stable Multi-Feedback Distributed Power Delivery Systems

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Abstract: *Distributed on-chip power regulation is necessary for delivering high quality power to modern high performance systems. Stability is a primary concern in these ICs. An automated design flow for stable, high quality power delivery is proposed. A distributed power delivery system is designed based on the proposed approach and fabricated in 28 nm CMOS technology, exhibiting high performance and stable response.*

Keywords: on-chip power delivery; LDO; stability; automated design.

Introduction

A critical challenge in modern high performance integrated circuits is delivering high quality power. While the quality of a power supply can be efficiently addressed with a point-of-load (POL) power delivery system, the complexity of a distributed POL power supply system is a significant design issue [1]. To cope with design complexity in complex analog circuits, automated modeling, optimization, and synthesis techniques are typically considered [2]. To automate the design of a power delivery system, accurate methods to evaluate performance metrics (*e.g.*, quality of transient response, stability, and power) are required. A distributed system with multiple low-dropout (LDO) regulators delivering power to a single grid can exhibit degraded stability due to complex interactions among the LDO regulators, power distribution network, and current loads. The stability of these parallel connected voltage regulators is therefore a primary performance concern and needs to be accurately evaluated.

A distributed power delivery system with two or more power supplies driving a single power grid is depicted in Figure 1. The stability of a single closed loop system is traditionally determined by the phase margin of the open loop response. In systems with multiple dependent loops, as shown in Figure 1, the open loop approach is not practical because no straightforward method exists to identify the unstable loop. An alternative stability criterion has recently been proposed that imposes a passivity condition on the power grid output impedance [3]. Automating the design process of a power delivery system is proposed in this work based on the passivity-based stability criterion with a parametric circuit performance modeling techniques.

Parametric IC Performance Modeling Technique

The performance of an individual power supply is typically determined by a set of parameters, such as the DC gain, phase margin, DC offset, slew rate, and power.

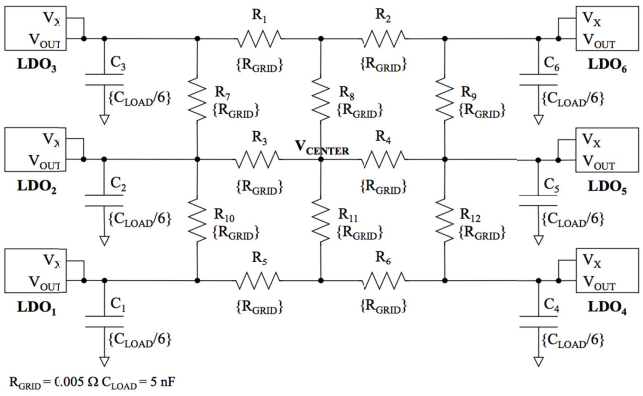


Figure 1. Model of distributed LDO and power distribution network.

Alternatively, a distributed power delivery system should be evaluated based on both the performance of the individual power supply and additional performance metrics of the combined system, such as the *phase margin of the output impedance*. To reduce the design complexity of modern distributed power delivery systems, the passivity-based stability criterion should be integrated within existing automated design methodologies. An automated flow for designing a stable distributed power delivery system is shown in Figure 2. During the first stage, an LDO regulator is synthesized based on the specific LDO topology and design objectives. The output of the first stage is used during the second stage to determine the number and location of the parallel connected power supplies in the proposed distributed power delivery system. During this second stage, a distributed power delivery system with a different number and location of voltage regulators is iteratively evaluated based on the passivity-based stability criterion and distributed power supply placement algorithms. During

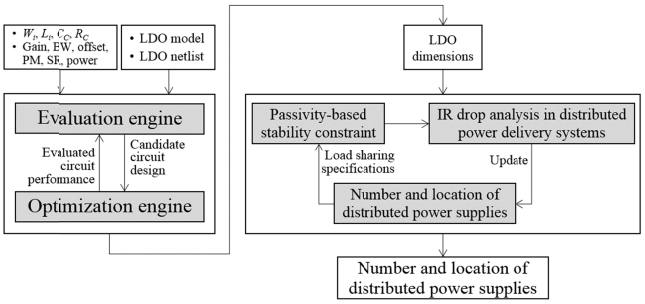


Figure 2. Automated PBSC-based design flow for a distributed power delivery system.

each iteration, the worst-case load sharing scenario is determined for the specific power delivery system. The passivity-based stability of the distributed system is evaluated based on the individual current loads. If required, the number and location of the power supplies are updated. Finally, the number and location of the parallel connected power supplies that satisfies the quality of power and stability requirements of the distributed power delivery system are determined.

The operation of the second stage of the automated PBSC-based design flow is demonstrated here based on the ISPD'11 placement benchmark suite circuits [4]. The floorplan of the superblue5, superblue10, superblue12, and superblue18 circuits is illustrated in Figure 3. Each of the

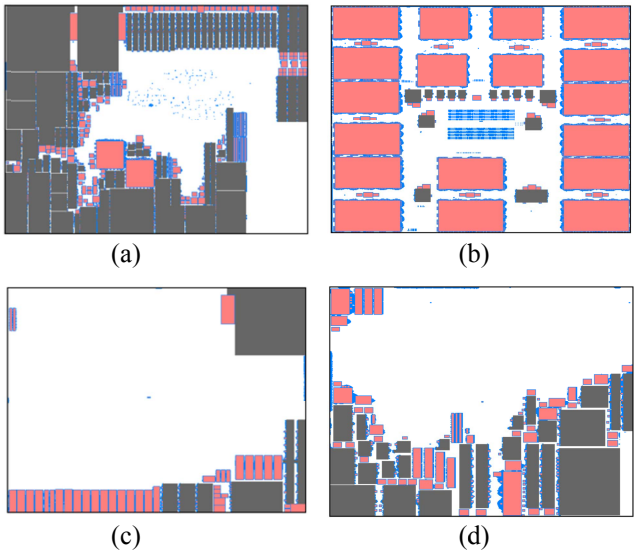


Figure 3. Floorplan of ISPD'11 circuits (a) superblue5, (b) superblue10, (c) superblue12, and (d) superblue18.

circuits is composed of thousands of fine grain rectangular shapes. To reduce the complexity of the circuit evaluation, the fine grain shapes are combined into larger rectangular nodes. Out of the combined nodes only the largest nodes are considered, exhibiting a reduced floorplan. Magnitude of the distributed current loads within a circuit is determined proportionally to the size of these nodes with a total load current of 1 A. The location of each of the current loads is determined in the center of the corresponding rectangular node. The number of the fine grain shapes, large nodes, coverage of reduced floorplan, and power grid data is listed in Table 1. Note, that the nodes in the reduced floorplan occupy more than 85 % of the total active circuit area.

Ideally a constant voltage is distributed to all the current loads within a circuit. Practically, the quality of power is degraded in modern circuits due to parasitic on-chip impedance. The voltage drop map of the superblue5 circuit without on- chip power supplies is shown in Figure 4, yielding a maximum voltage drop of 23.4 %, assuming off-chip voltage supply of 1V. To address the quality of on-chip

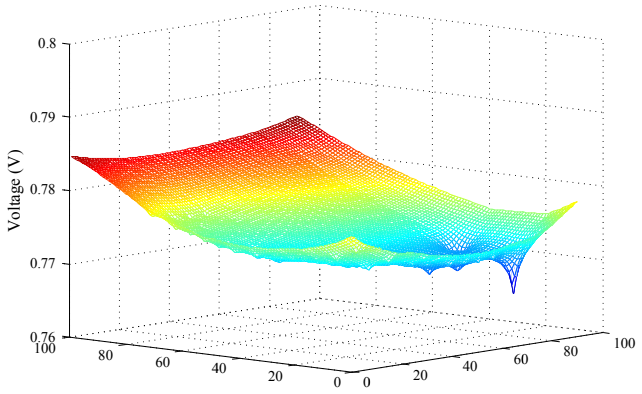


Figure 4. Voltage drop map of the superblue5 circuit.

power supply, power delivery systems with a single on-chip power supply (case 1), six on-chip power supplies (case 2), and twelve on-chip power supplies (case 3) are considered. For each of the three cases, *IR* drop of the distributed power delivery system is analyzed based on the *IR* drop algorithm for a power grid with multiple power supplies and current loads [5]. The location of power supplies in cases 1 and 2 is modeled as a mixed integer nonlinear programming problem, and optimized based on the general algebraic modeling system (GAMS) [6]. In case 3 the power supplies are uniformly distributed on-chip. Stability is evaluated in each of the three cases based on the passivity-based criterion. The map of the voltage drops and phase of the output impedance within superblue5 with different number of on-chip power supplies is shown in Figure 5. The maximum voltage drop is efficiently reduced with increasing number of power supplies, exhibiting reduction in the maximum voltage drop of, respectively, 14.23%, 20.29%, and 22.29% with a single, six, and twelve on-chip power supplies. Alternatively, the output current of the individual regulators changes with the number of power supplies, affecting the phase of the output impedance and

Table 1. Properties of ISPD benchmark circuits.

Circuit	Number of fine grain shapes	Number of large combined nodes	Coverage of reduced floorplan	Power grid size	Number of nodes in the power grid
superbule5	29,736	129	85.0%	774 × 713	551,862
superbule10	2,318	30	89.2%	638 × 968	617,584
superbule12	3,578	15	98.4%	444 × 518	229,992
superbule18	6,776	71	99.5%	381 × 404	153,924

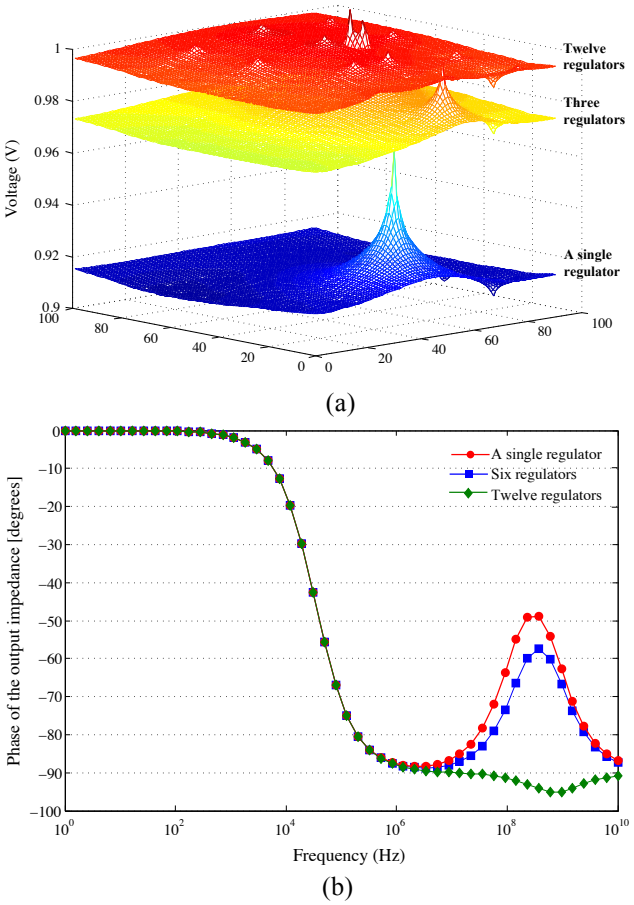


Figure 5. Superblue5 circuit with a single, three, and twelve on-chip power supplies, (a) map of voltage drops, and (b) phase of the output impedance.

stability characteristics of the distributed system. Based on the passivity-based stability criterion, the under aggressive transient response. Thus, a stable system with smaller number of power supplies should be preferred to deliver power to the superblue5 circuit while addressing both quality of power and stability challenges.

The second stage of the automated PBSC-based design flow, shown in Figure 2, is implemented in Matlab. Pseudo-code of the algorithm is summarized in Algorithm 1. A typical LDO model [7] is used to describe a small signal response of the on-chip power supplies, and evaluate the output impedance of the power supplies and overall power

Algorithm 1. Automated PBSC-based design flow.

```
1.  LDOModel; // A typical LDO model [7]
2.  CircInfo; // Supply voltages, load currents and locations
3.  CircNodes; // All nodes in the evaluated circuit
4.  NumRegsList; // List of numbers of LDOs to evaluate
5.  PreferredNumRegs ← 0; // Preferred number of LDOs
6.  PreferredLocs ← N/A; // Preferred location of LDOs
7.  PreferredIRDrop ← 1; // Maximum allowed IR drop
8.  for all NumRegs ← NumRegsList do
9.    for all RefNode ← CircuitNodes do
10.       // Find optimal LDO locations [6]
11.       OptLocs←OPT_LOC(CircInfo, NumRegs);
12.       // Analyze IR drop in a power grid [5]
13.       IRDrop(RefNode) ← CALC_IR_DROP(CircInfo,...
14.                                      OptLocs, ...
15.                                      RefNode);
16.       // Calculate the output impedance of the LDOs
17.       for all LDO ← LDOs do
18.          ISupply ← Current delivered by the LDO;
19.          Z_OUT^LDO (LDO) ← CALC_Z_OUT(LDOModel,...
20.                                       ISupply);
21.       end for
22.       // Calculate the output impedance of the system
23.       Z_OUT^SYS ← ( ∫_LDOs 1 / Z_OUT^LDO(LDO) )^-1 ;
24.       if max{|∠ Z_OUT^SYS|} < 90° then
25.         if max{IRDrop} < PreferredIRDrop then
26.           PreferredIRDrop ← max{IRDrop};
27.           PreferredNumRegs ← NumRegs;
28.           PreferredLocs ← OptLocs;
29.         end if
30.       end if
31.   end for
32. end for
```

delivery system. Power delivery systems for the ISPD'11 benchmark circuits superblue5, superblue10, superblue12, and superblue18 have been generated and evaluated based on the proposed algorithm. The maximum *IR* drop and stability results are listed in Table 2. Based on the evaluated benchmark circuits, the maximum voltage drop is significantly reduced with the increasing number of on-chip

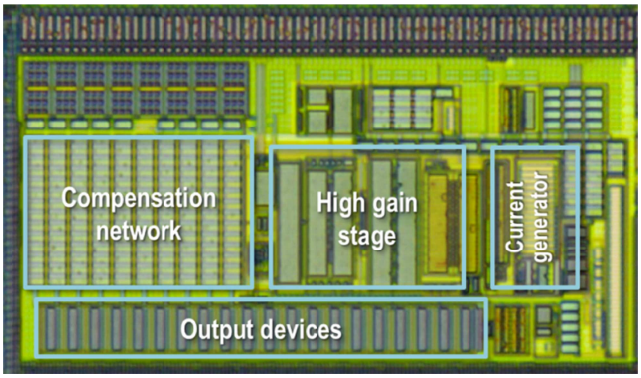
Table 2. Maximum *IR* drop and stability in ISPD benchmark circuits.

circuit	No regulators		A single regulator		Six regulators		Twelve regulators	
	Maximum *IR* drop	Stability	Maximum *IR* drop	Stability	Maximum *IR* drop	Stability	Maximum *IR* drop	Stability
superblue5	23.4%	N/A	9.17%	Stable	3.11%	Stable	1.11%	Not stable
superblue10	23.0%	N/A	10.8%	Stable	4.75%	Stable	2.43%	Not stable
superblue12	23.6%	N/A	10.7%	Stable	6.39%	Stable	4.88%	Not stable
superblue18	22.7%	N/A	10.7%	Stable	4.43%	Stable	1.54%	Not stable

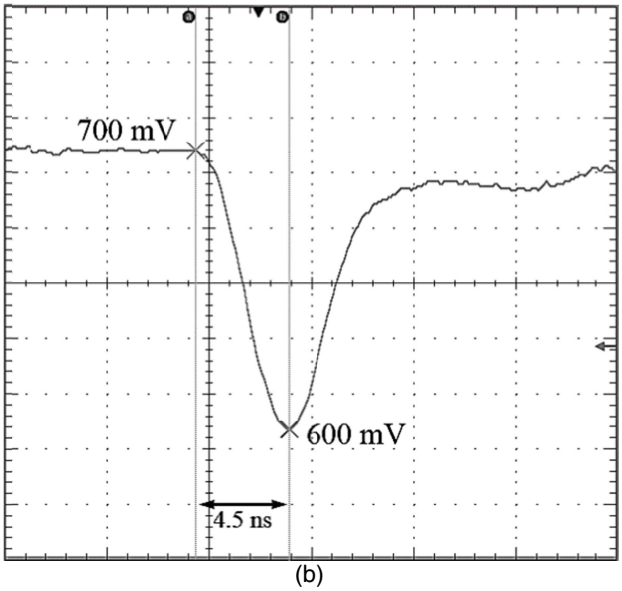
power supplies. Alternatively, stability of the distributed power delivery system is a function of specific load distribution and affected by characteristics of POL power delivery system. The proposed automated PBSC-based design flow generates a distributed power delivery system that addresses both the quality of power and stability requirements.

Experimental results

A power delivery system with six LDO regulators has been designed and evaluated based on the proposed passivity- based stability criterion. The system has been fabricated in an advanced 28 nm CMOS technology. The area occupied by the LDO with all capacitors is 85 µm × 42 µm. A die microphotograph of the LDO, and measured transient response for load current step (stepped from 52 mA to 788 mA in 5 ns), and nominal input and output voltages of, respectively, 1.0 volt and 0.7 volts is illustrated in Figure 6.



(a)



(b)

Figure 6. Experimental results, (a) die microphotograph of a single LDO regulator and current generating circuit, and (b) measured transient response.

Based on these experimental results, the system of six parallel LDO regulators yields a stable response and voltage droop of 0.1 volts.

Conclusions

Evaluation of the stability of distributed on-chip power delivery systems is a primary concern in modern high performance integrated circuits, and is not practical with the traditional phase margin criterion. A design automation flow is proposed in this work based on passivity-based stability criterion. The proposed design flow is demonstrated on a set of benchmark circuits with different number of parallel connected voltage regulators, yielding an efficient technique for the automated design of stable distributed power delivery systems. A distributed power delivery system with six LDO regulators is evaluated based on the results of the stability analysis. The system is fabricated in 28nm CMOS technology, and tested under aggressive load step, exhibiting high performance and stable response.

Acknowledgements

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