Global Signaling for Large Scale RSFQ Circuits

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***Abstract*—The increasing complexity of modern rapid single flux quantum (RSFQ) circuits has made on-chip signal routing an issue of growing importance. In this paper, several methods for routing large scale RSFQ circuits are described, and a methodology is presented for determining when to use either passive microstrip transmission lines (PTL) or active Josephson transmission lines (JTL). The effect of the JTL inductor and Josephson junctions on the length of a JTL chain to achieve a target delay is also discussed. A novel PTL driver and receiver configuration is proposed. Tradeoffs among the number of JJs, inductance, and length of the PTL stripline in the receiver and driver circuits are reported. The energy dissipation is evaluated for two different interconnects and is compared with CMOS. The tradeoff between the proposed PTL circuits and a JTL in terms of energy dissipation and delay is also discussed. Guidelines for choosing the optimal element values are determined, and a margin of ±29% for the bias current of the proposed receiver operating at 20 GHz in a 10 kA/cm^2 technology is achieved. The bias margin of the PTL is -21% and +29% by directly connecting an OR gate to a PTL line and -10% and + 29% by connecting to a D flip flop. Summarizing, guidelines and design tradeoffs appropriate for automated layout and synthesis are provided for driving long interconnect in SFQ VLSI complexity circuits.**

***Index Terms*—Single flux quantum, superconducting integrated circuits, superconductive digital electronics.**

I. Introduction

CONVENTIONAL integrated circuit technology is based on CMOS devices and standard metal interconnects. The scaling of CMOS technology, however, has significantly slowed in recent years. Advanced nanoscale fabrication facilities have become prohibitively expensive, and the energy consumption of CMOS circuits is increasing. An attractive alternative to advanced semiconductor technologies for large scale ultra-high speed and ultra-low power digital applications is Josephson junction (JJ) based digital superconducting circuits [1]. Superconductive IC technology has produced the highest performance digital circuits [2]. Rapid single flux quantum (RSFQ) is a popular digital logic family within this promising beyond CMOS superconductive technology. In RSFQ, information is represented in the form of picosecond wide voltage pulses within a quantized area, called a single flux quantum (SFQ) pulse. Recent research efforts suggest the use of this technology for high performance, energy efficient supercomputers to achieve DoE exascale computing objectives [3], [4].

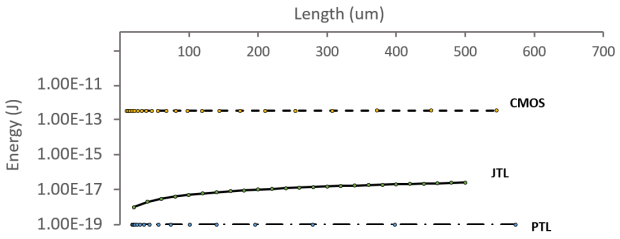

Fig. 1. Energy vs. length of CMOS (dash line), JTL (solid line), and proposed PTL (dash-dotted line).

The primary characteristics of these circuits are high speed digital logic with low power, ideal (no DC resistance) interconnects, quantum accuracy, scalability, and relatively low manufacturing complexity [2]. A comparison of the energy dissipated by interconnect for CMOS and SFQ is shown in Figure 1. The energy of a 16 nm CMOS interconnect technology is evaluated with an RLC model. The energy of the CMOS interconnect is approximately six orders of magnitude greater than the energy dissipated by a passive superconductive interconnect.

With only a modest number of researchers worldwide, significant progress has recently been achieved in enhancing RSFQ circuit performance and operational frequencies [2]. Complex RSFQ circuits have been experimentally tested [5], and high operating clock frequencies in microprocessors [6], [7] and network switches [8] beyond 20 GHz [9] have been successfully demonstrated. RSFQ digital-RF receiver circuits with tens of thousands of Josephson junctions have been experimentally verified up to an operating frequency of 30 GHz [10]. Furthermore, recent progress in SFQ manufacturing processes has resulted in device densities of over 600,000 JJ/cm^2 [11].

Combined with recent efforts to develop EDA tools for superconducting electronics [12], [13], the complexity of RSFQ circuits is expected to greatly increase. Current *ad hoc* practices in many stages of the SFQ circuit design process need to be replaced with quantitative guidelines. Automated routing and clock tree synthesis (CTS) are examples of these practices, where methodologies for signal and clock routing are currently not well established.

While general synchronization principles and techniques commonly used in CMOS are applicable to SFQ technology, several notable differences exist. Sub-terahertz clock frequen-

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cies and pulse-based logic in SFQ present unique challenges for providing an accurate and stable clock signal. One of the primary concerns of the automated layout and CTS methodologies in conventional integrated circuits is the interconnect characteristics. SFQ-based automated layout and clock tree synthesis tools require specialized guidelines to determine the optimal interconnect structure for each line. Furthermore, in a standard cell flow, the optimal driver and receiver configuration needs to be determined for the interconnect lines.

To propagate a signal within the interconnect between RSFQ gates, Josephson transmission lines (JTL) or passive transmission lines (PTL) are typically used [14]. The JTLs in RSFQ interconnects consume power and add delay due to the switching JJs. Furthermore, JTLs are placed within the standard cell layers, resulting in increased congestion. Although not a significant issue in current MSI RSFQ circuits, the greater power, delay, and area pose a significant challenge for future RSFQ VLSI circuits.

A PTL is another type of SFQ signal wiring method, consisting of a superconductive microstrip or a stripline. SFQ pulses ballistically propagate along a PTL at the speed of light within the medium. Utilizing PTLs rather than JTLs for long lines in RSFQ VLSI circuits reduces the output delay, power consumption, and congestion [15], [16], [17].

Many models for interconnect delay estimation are utilized in conventional CMOS-based routing tools, and multiple techniques exist to reduce or increase wire delay to achieve a target clock skew, such as wire sizing and wire snaking [18], [19]. Since the delay of a PTL only depends on the line length and not the capacitance, and the pulse propagation speed in a PTL approaches the speed of light, CMOS-like techniques are inappropriate in superconducting electronics. If necessary, pulses can be delayed by inserting JTL stages within the signal and clock lines.

In this paper, SFQ interconnects - PTLs and JTLs - are discussed in section II. The effects of line width on the interconnect structures, dependence of the JTL inductance on the physical layout, and different PTL driver and receiver circuit configurations are also described in section II to provide guidelines for driving long interconnect. The effect of different driver/receiver circuit parameters on impedance matching between a PTL line and the driver/receiver circuits is also described; specifically, to achieve shorter delay, smaller area, and lower power as well as greater bias margins. In section III, a novel PTL driver and receiver circuit is introduced. The characteristics of a PTL stripline when inserting a repeater (driver/receiver pair) or a JTL, are also discussed in section III. The bias current margins of the proposed PTL topology are described in section IV by directly connecting an RSFQ gate to a PTL line assuming the proposed PTL circuit topology. The paper is concluded in section V.

II. SFQ INTERCONNECT

The propagation of an SFQ pulse plays an important role in the performance of complex SFQ circuits. Two different transmission line types are used for SFQ interconnect: active Josephson transmission lines and passive transmission lines.

A JTL is an active interconnect, which can transfer an SFQ pulse without reflections, providing noise discrimination by regenerating the pulse at each stage. A PTL consists of a passive microstrip or a stripline with an active driver and receiver. The PTL output delay therefore scales linearly with line length.

In this section, each of these interconnect types is described. The properties of the interconnects such as delay for a constant length, physical area, energy dissipation, and reflections determine when to use a PTL or JTL interconnect. The properties of a Josephson transmission line and the effects of the JTL linewidth on area are discussed in subsection II-A. Utilization of standard PTLs in VLSI oriented SFQ circuits is discussed in subsection II-B.

A. Josephson transmission lines

Josephson transmission lines are typically used as basic cells to connect RSFQ gates. A JTL is typically composed of uniformly sized Josephson junctions with a uniform inductance L between junctions. Consequently, the length and area of a JTL within a standard cell library only change in terms of the number of stages. In this subsection, the length and area of a JTL for different number of stages are described for different line widths of the niobium (Nb) inductor, where the characteristics of the inductance are based on MIT Lincoln Laboratory SFQ5ee design rules [20].

The geometric parameters, such as the shape of the Josephson junction layout (orientation of the shunt resistor) and the width of the inductor, affect the area of a JTL cell [21]. Two different layouts of a JJ with an external shunt resistor are depicted in Figure 2. A straight line layout is assumed for the shape of a JTL for all shunt resistors and inductors, as shown in Figure 2(a). The area of a standard cell-based circuit in an active layer can be further decreased by utilizing bends in the layout of the superconductive inductors and JJs. By maintaining a constant inductance and increasing the linewidth, the area and length of a JTL increase to maintain the same output delay. The dependence of the area and delay on the linewidth of the JTL inductance is discussed below.

Consider a linewidth of a JTL inductor ranging from 350 nm to 1 μm (see Figure 2). The length and area of a JTL are, respectively, on the order of 20 to 32 μm and 55 to 80 μm^2 for a single JTL stage. The inductance L is 2 pH. A comparison of two different JTL linewidths is shown in Figure 3. The minimum linewidth is 350 nm, based on SFQ5ee design rules [20], while the maximum linewidth depends upon the JTL layout, and is chosen, somewhat arbitrarily, to be 1 μm.

The output delay of a JTL with two JJs is about 5 ps. The delay of a chain of JTLs increases linearly with the number of JTLs. For a constant inductance and therefore constant delay, the length and area of the JTL significantly increase with wider inductors, as shown in Fig. 3 for two widths, 350 nm and 1 μm.

As a JTL consists of actively switching JJs in the top layer, a JTL-based SFQ interconnect consumes additional area, power, and delay. To lower the area, power, and delay in large scale circuits, PTLs are used to connect distant RSFQ gates.

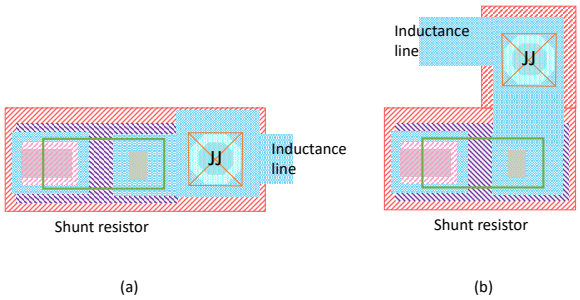

Fig. 2. Layout of a Josephson junction with a shunt resistor, (a) straight line, and (b) bent line.

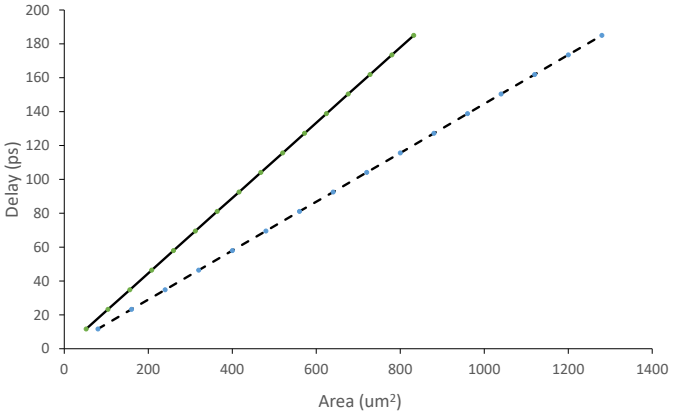

Fig. 3. Delay vs. area of a JTL with a linewidth of 350 nm (straight line) and 1 μm (dash-dotted line).

B. Passive transmission lines

A typical PTL consists of a superconductive stripline, one JJ, and a small inductance in the driving circuit, and two JJs with a small inductance in the receiving circuit [22]. The parameters affecting the pulse propagation characteristics are the bias current, size of the internal inductance, number and size of the JJs, and length, width, and impedance of the stripline between the driver and receiver.

For long lines, it is desirable to use PTLs rather than JTLs as a PTL only requires active JJs in the driver and receiver. Furthermore, the power consumed by a PTL line is independent of length [15], [16], [17]; less power is consumed in long lines. Unlike JTL interconnect, a PTL also offers greater flexibility and less routing congestion [23].

A typical PTL requires at least one additional JJ in the driving cell, resulting in additional area, power, and delay. Furthermore, the number of bias connections for a PTL driver and receiver depends upon the number of JJs. With three bias current sources for a typical PTL driver and receiver, additional area and energy is introduced into the bias network. In this paper, a PTL topology without a driver circuit is proposed in section III. The PTL is driven by the output JJ of the cell without any additional circuitry. For this novel topology, a comparison of PTL and JTL wiring methodologies is discussed.

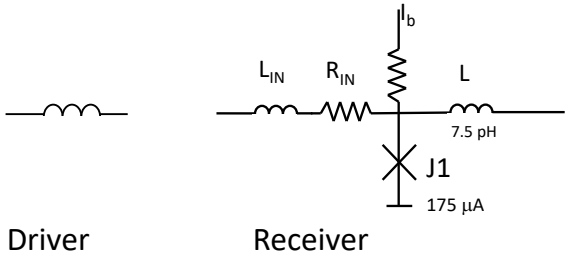

Fig. 4. Proposed driver and receiver circuits.

III. Novel SFQ PTL driver/receiver

A topology for a PTL interconnect in a 10 kA/cm^2 technology is proposed in this section. The proposed PTL circuits are shown in Fig. 4. The PTL driver is represented by a small parasitic inductance between the active layer and the routing layer (the via) and contains no Josephson junctions. The PTL receiver consists of one JJ with a Stewart-McCumber parameter (β) corresponding to a slightly underdamped state and a large inductance. The input inductor in the receiver is a parasitic inductance due to the via from the logic gate layers to the PTL routing layer.

In this paper, a PTL is modeled as a transmission line exhibiting an impedance in the range of 10 to 15 ohms and a linewidth ranging from 2 to 5 μm (assuming a straight line structure). SFQ pulses are produced by the output JJ within the last RSFQ gate driving the PTL line. The driver and receiver provide sufficient signal power and impedance matching (at a clock frequency of 20 GHz) between the PTL and the load. Removing the separate driver circuit decreases the output delay, area, and energy dissipated by the PTL, while degrading the matching characteristics as compared to a PTL with a standard driver circuit. A larger β improves the impedance matching characteristics and increases the amplitude of the SFQ voltage pulse. Furthermore, a large inductance and input resistor within the receiver improve the impedance matching characteristics while lowering reflections and increasing the delay.

In the proposed PTL receiver, the effect of the large inductance on delay is shown in Figure 5. A larger inductance improves circuit operation while significantly increasing the delay. The optimal inductance to minimize reflections while maintaining reasonable delay for the proposed receiver technology is about 7.5 pH.

The input resistor in the PTL receiver dissipates additional energy. The energy dissipated by the proposed PTL is discussed in subsection III-A. The number and size of the JJs in the PTL affect the output delay and physical characteristics of the interconnect. The effects of the proposed topology on area and delay are discussed in subsection III-B. The properties of the PTL interconnect described in this section and the JTL described in section II provide guidelines to when to use a PTL or JTL.

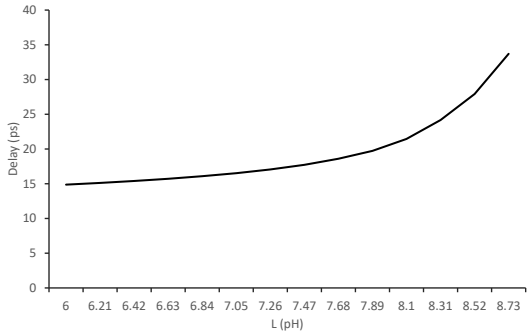

Fig. 5. Effect of inductance on propagation delay.

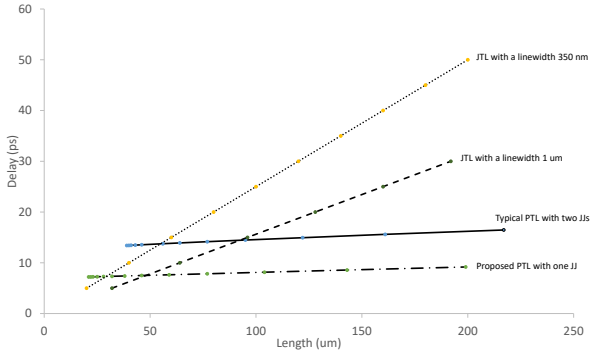

Fig. 6. Delay vs. length of a JTL with a linewidth 350 nm (dotted line) and 1 μm (dash line), and typical PTL with two JJs (solid line) and proposed PTL with one JJ (dash-dotted line) in the receiver.

A. Energy

Resistors are typically inserted into a PTL to improve the matching characteristics, prevent current redistribution and flux trapping in long superconductive loops, and provide additional damping for signal reflections. The resistors in a PTL, however, also reduce the signal power available at the receiver and dissipate additional energy. In the operational range of resistances, the maximum dissipated energy in the PTL resistors is approximately $10^{-19}J$ per bit, five times lower than the switching energy of a JJ, $\Phi_0 \times I_C = 5.17 \times 10^{-19}$J for a 250 μA Josephson junction. The resistive energy dissipation is therefore negligible and can be ignored when selecting between a PTL and a JTL.

The energy of an SFQ PTL, composed of an ideal transmission line, input resistor, and one JJ, is approximately 6×10^{-19} J. The PTL line exhibits a constant energy independent of length. The energy of a JTL, composed of two JJs, is approximately 10^{-18} J. The energy of a chain of JTLs increases linearly with the number of JTLs.

B. Length and Area of Interconnect

The effect of two different PTL receiver topologies (two JJs and one smaller inductance, and one JJ and a large inductance) on the length of the interconnect as compared to the JTL interconnect is shown in Figure 6. The length of the driver and receiver within both the proposed PTL and a typical PTL in the active gate layer are, respectively, 19 and 40 μm. The length of the line within the routing layer is dependent upon the distance between the two gates. The minimum length of the proposed PTL interconnect including the vias, receiver, and routing line is 21 μm. The minimum length of a single stage JTL within the active gate layers is about 20 μm. The delay of the proposed PTL with one JJ and the JTL is, respectively, about 8 and 5 ps.

For complex RSFQ circuits, automated routing and CTS algorithms need to choose between different interconnect types depending upon the physical characteristics of the interconnect within the active gate (JJ) layers or the routing layers. The length and area of the PTL interconnect affect both the JJ layer and the routing layer. The JTL interconnect only requires additional area within the JJ layer. Congestion in the routing layer, assuming space within the cell layers is available, can make a JTL the preferable choice for interconnect despite the greater area, power, and bias requirements.

The area of the proposed PTL in the active gate layer can be reduced by removing the JJ in the driver and the number of JJs and bias current in the receiver. The area of the PTL line in the routing layer is dependent upon the length of the PTL. The minimum area of a PTL in the routing layer is on the order of 4 to 25 μm^2 for a linewidth ranging from 2 to 5 μm. Considering the minimum length of a PTL in the routing layer and the area of the driver and receiver in the active gate layer, the area of the proposed PTL is, respectively, 40 to 60 μm^2 for two different PTL linewidths in the routing layer, 2 and 5 μm. The minimum area of a typical PTL is about 80 to 100 μm^2.

By lowering the overhead of the driver/receiver circuits, a PTL can more effectively drive a shorter line. The proposed PTL exhibits a lower delay for the same area for both short and long interconnect. Unlike standard PTL circuits, the proposed PTL circuit requires only one bias current source. This feature reduces the area of the bias network.

The delay of a typical PTL is lower than the delay of a JTL for long interconnect. For short interconnect, however, the PTL requires greater area than a chain of JTLs. For a short line, a JTL with a 350 nm linewidth requires less area with the same delay as compared to both a JTL with a 1 μm linewidth and a standard PTL. For the same interconnect length, the proposed PTL exhibits a lower delay.

IV. Margin Analysis

A bias margin analysis to determine the optimal parameters is discussed in this section. The margins are evaluated by connecting the proposed PTL within a chain of JTL cells. The bias margins of a PTL with one JJ and two JJs in the receiver are, respectively, approximately ±29% and ±12%. The bias margins of the proposed receiver are larger than the margins of a standard PTL with two JJs in the receiver for all lengths, despite the larger inductance in the receiver. The delay increases with a larger inductance in the receiver, however, the bias current margin improves when the inductance is in the range of 6 to 9 pH. A large inductance in the proposed receiver improves the bias margin by 8% as compared to a

small inductance for the same bias current. By increasing the inductance, the impedance matching characteristics are also enhanced.

As perfect matching of an RSFQ gate to a stripline is impossible to achieve, the SFQ pulses combine with the reflections from the driver and the receiver as the signal propagates along a PTL line. The reflections depend upon the connection between the PTL line and an RSFQ gate. A PTL line at the output of an RSFQ gate without any JTL buffer cells behaves as a load, and can produce reflections and signal fluctuations. A JTL buffer cell between the RSFQ logic cell and a PTL line can decrease the effect of the load and reflections, improving the margins but increasing the area and delay. The performance of the proposed driverless PTL topology is evaluated by directly connecting an RSFQ logic cell to a PTL without any JTL buffer cells.

The performance of the proposed PTL is evaluated by connecting a PTL to a D flip flop (DFF). The circuit topology is shown in Fig. 7. J4 behaves as a memory for the DFF and a driver for the PTL line. Due to reflections between the PTL and the DFF output, the delay of the receiver increases and the bias margin of the receiver decreases. The margin of a PTL directly connected to a DFF is approximately -10%, +29%. By changing the bias current, the bias margins can be shifted to ±17%. To improve the bias margins, a single JJ and bias current source (half of a JTL stage) can be placed after the DFF. This stage decreases the load of the PTL line and lowers the reflections, while adding delay and area. With this stage, the margin is approximately -23%, +28%. By increasing the bias current, the margin becomes ±25%.

The proposed PTL line is also connected to an OR gate to determine the performance and margins of the proposed PTL when used for routing between logic gates. The circuit configuration is shown in Fig. 8. In this configuration, the PTL line is directly connected to the last internal inductance, L7 and L8, of the OR gate. Reflections between these inductances and the PTL line result in incorrect functionality of the gate. The output of the OR gate is shown in Fig. 9. To improve the performance of the circuits and decrease the reflections, one JJ is added to the output of the OR cell. The correct operation of the OR gate and receiver are also shown in Fig. 9. The margin of the proposed PTL with a single JJ at the output of the OR gate is approximately -21%, +29% with low reflections at the output of the OR gate. By increasing the bias of the current source of the receiver, the margins become ±24%. Using two JJs as a buffer instead of one JJ produces slightly better margins, but significantly greater area and delay.

From this margin analysis, the use of the proposed driverless PTL depends upon the cell library and target bias margins. The proposed approach provides significant benefits for connecting buffered and robust gates (such as a DFF and JTL), and requires additional JTL buffer stages when connecting sensitive gates (such as an OR gate).

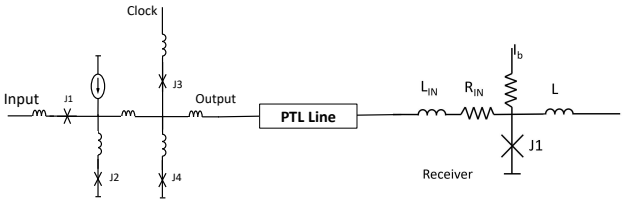

Fig. 7. Circuit configuration of a DFF connected to a PTL line.

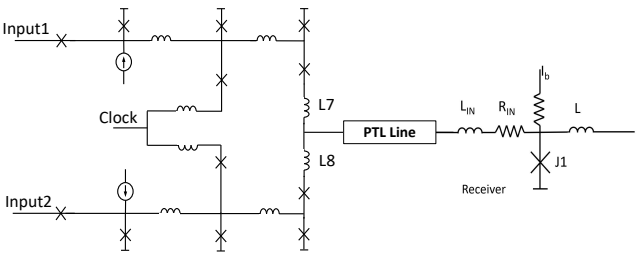

Fig. 8. Circuit configuration of an OR gate connected to a PTL line.

V. Conclusions

In this paper, the interconnects for prospective cryogenic RSFQ IC technology are described, evaluated, and compared to CMOS interconnects. Different routing approaches for RSFQ VLSI circuits are also discussed. Specific guidelines are required for different RSFQ interconnect structures (PTL and JTL) for use in EDA tools such as automated layout and clock tree synthesis. In this paper, several PTL and JTL configurations are presented, and tradeoffs among the different configurations are discussed. A PTL with no driving circuit and one JJ in the receiver is proposed. The proposed PTL exhibits a higher margin as compared to a standard PTL. A margin of ±29% for the proposed receiver operating at 20 GHz in a 10 kA/cm^2 technology is achieved with a JTL at the input. The bias margin for a PTL connected to a DFF is -10%, +29% without additional JTL buffers.

The delay of the proposed PTL is lower than the delay of a JTL interconnect for long lines. By reducing the number of JJs and bias sources, the proposed PTL interconnect also dissipates less power while reducing the complexity of the bias network. The proposed PTL interconnect has lower complexity, area, and delay, making the structure appropriate for automated layout and clock tree synthesis.

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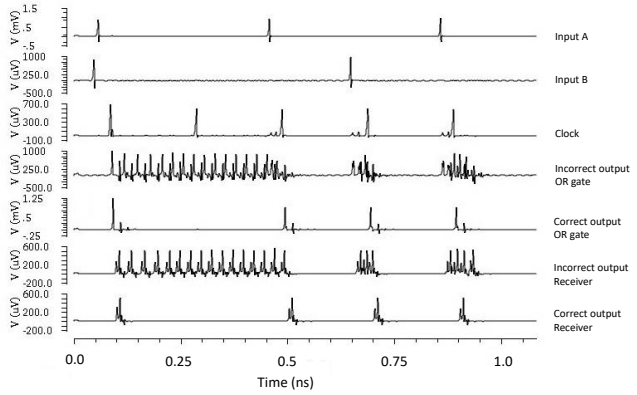

Fig. 9. OR gate with a direct connection to a PTL line. Note both the incorrect and correct operation of the OR gate and receiver.

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