Dynamic Logic Operating at Cryogenic Temperatures

Nurzhan Zhuldassov and Eby G. Friedman

Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627
nzhuldas@ur.rochester.edu

***Abstract*—Cloud computing is increasing the demand for large scale, energy efficient, and fast computing systems. A CMOS circuit style satisfying these goals is dynamic logic. Since portability is not required for cloud computing centers, these systems can support cryogenic operation. Cryogenic operation eliminates the seminal issue of dynamic circuits, loss of logic state due to leakage currents. At higher temperatures, static logic circuits are preferable since these circuits are unaffected by leakage currents. The operating temperature therefore affects the choice of circuit style: dynamic or static. The operation of dynamic CMOS circuits at different temperatures and the temperature at which dynamic logic is preferable to static logic are discussed here. Dynamic logic operating above 1.209 GHz can be used at temperatures up to 300 K, room temperature for a 160 nm technology node. At lower frequencies, static circuits should be used. Below 77 K, liquid nitrogen temperature, dynamic logic is stable above 29.7 MHz. At temperatures below 11 K, dynamic logic circuits operating above one hertz can be used. Since dynamic logic circuits operate at DC below 4.5 K, dynamic logic is preferable at any frequency below this temperature, including liquid helium temperature, 4.2 K.**

***Index Terms*—Cryogenics, liquid helium temperature, CMOS, MOSFET, dynamic logic**

I. Introduction

Cloud computing requires high performance, energy efficient processors and can support cryogenic operation since portability is not desired. Higher frequency circuits, required in cloud computing systems, can utilize dynamic logic circuits for improved performance. As compared to static logic circuits, dynamic circuits are faster, lower power, and require less area. Room temperature (RT, 300 K) dynamic logic circuits cannot however operate at low frequencies and are highly sensitive to noise. Dynamic circuits at RT operate correctly only above certain frequencies since the state is temporarily stored on a capacitor. This drawback makes developing complex systems based on dynamic circuits challenging, since low frequency operation of these circuits is a difficult issue. Dynamic circuits operating at cryogenic temperatures bypass these issues [1].

Significant improvements in performance can be achieved by cooling the environment [2]. Cryogenic electronics plays an important role in meteorology, quantum computing, high energy physics, and space-based technologies. Furthermore, applications which require a high signal-to-noise ratio and/or receive weak input signals benefit when operated at cryogenic temperatures [3]. Cryogenic environments also avoid thermal runaway in semiconductors [4]. Nevertheless, static logic is preferable at RT since these circuits are not affected by leakage currents. At cryogenic temperatures, alternatively, dynamic circuits are preferable due to the aforementioned speed, power, and area advantages [5]. One issue is at what temperature do dynamic logic circuits outperform static circuits. In this paper, this temperature is determined for different frequencies. The key temperatures discussed in this paper are liquid helium temperature (LHT), 4 K, liquid nitrogen temperature (LNT), 77 K, and room temperature, 300 K. The relative performance of dynamic logic at these temperatures is also discussed.

The paper is organized as follows: the characteristics of static and dynamic circuits are highlighted, and insight into MOSFET operation at cryogenic temperatures is described in Section II. The power consumption of a MOSFET at cryogenic temperatures is discussed in Section III. Dynamic circuit operation is characterized at cryogenic temperatures in Section IV, and the temperature at which dynamic logic can be used rather than static logic is discussed in Section V. Some conclusions are offered in Section VI.

This research is supported in part by the National Science Foundation under Grant No. CCF-1716091, IARPA under Grant No. W911NF-17-9-001, and by a grant from Qualcomm.

DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited.

II. Background

Modern high complexity digital systems primarily deploy static logic. These systems can be enhanced by dynamic logic if operated at cryogenic temperatures. The temperature at which static logic should be replaced by dynamic logic depends upon the leakage currents; specifically, the subthreshold leakage current. The effects of subthreshold leakage current varies based on the style of logic circuit. Differences between static and dynamic logic are described in subsection II-A. The behavior of a MOSFET operating at cryogenic temperatures is reviewed in subsection II-B.

A. Static and dynamic logic circuits

Many types of MOSFET logic circuits have been developed since the 1970's. These circuits primarily fall into two categories, static logic and dynamic logic.

To reduce power consumption, static logic can operate at lower frequencies or placed into standby mode [1]. Dynamic logic, alternatively, temporarily stores information on a capacitor. Thus, dynamic logic cannot operate at low frequencies due to the leakage of charge on the capacitors and exhibits a low tolerance to noise [6]. Since leakage current at cryogenic temperatures becomes negligible, the charge on the capacitors requires additional time for the state to leak. This property allows dynamic logic to operate at lower frequencies, essentially DC at 4.2 K, which reduces the power consumption and supports low frequency testing.

At cryogenic temperatures, a MOSFET exhibits enhanced physical properties such as higher transient currents, negligible leakage currents, and increased subthreshold slope [7]. These properties are discussed in the following subsection.

B. MOSFET characteristics operating at cryogenic temperatures

Silicon MOSFETs operating at cryogenic temperatures exhibit significant improvements in performance and reliability as compared to room temperature operation. Since the late 1980's, cryogenic MOSFETs have, until recently, received little attention. The first studies on the behavior of MOSFETs at cold temperatures are described in [8]–[14]. The topic has once again become important due to the growing interest in cloud computing, enhancing the need for energy efficient, stationary computing platforms.

The carriers within the substrate of a CMOS transistor start to freeze out at 77 K [15]. With a voltage applied between the source and drain, the carriers, driven by energy from an applied electric field, form an inversion layer, becoming conductive. The mobility of the channel increases at lower temperatures due to less carrier scattering caused by lattice vibrations, but is limited by Coulombic scattering at lower gate voltages and surface roughness at higher gate voltages [16]. As a result, the speed of MOSFET devices operating at cryogenic temperatures is greater than at room temperature. For example, a 62% improvement in speed has been observed in a ring oscillator operating at 4 K [15]. A MOSFET operating at cryogenic temperatures exhibits the following advantages as compared to 300 K behavior: negligible leakage currents, higher sub-threshold slope, insignificant electromigration, fewer thermal induced failures such as oxide degradation, higher transconductance, and no latch-up [15].

The MOSFET considered in these simulations is a 160 nm CMOS transistor [5]. The transistor has a width of 2.32 μm and a channel length of 160 nm with a thin oxide. The drain current I_D at 4.2 K is 40% larger than the drain current at room temperature due to the higher carrier mobility. As compared to room temperature operation, the threshold voltage increases from 0.55 volts to 0.7 volts and the subthreshold slope (SS) is 3.8 times steeper at LHT than RT, increasing from 87.0 mV/decade to 22.8 mV/decade [17].

III. Cryogenic Power Consumption in CMOS

To evaluate the performance of CMOS logic circuits operating at cryogenic temperatures, the power consumption of a MOSFET within a cryogenic environment is reviewed. Power loss mechanisms within a CMOS circuit operating at low temperatures are described in subsection III-A. Subthreshold leakage current, the primary power loss mechanism at cryogenic temperatures, is described in subsection III-B.

A. Types of power loss in CMOS circuits

Power dissipation in CMOS consists of transient and static power consumption. Transient power consumption is a combination of switching power loss and short-circuit power loss, while static power consumption consists of gate leakage current and subthreshold leakage current [18], as described by

$$P_{leakage} = \overbrace{P_{Switching} + P_{Short-circuit}}^{\text{Transient leakage}} + \overbrace{P_{Gate-leakage} + P_{Subthreshold-leakage}}^{\text{Static leakage}} \quad . (1)$$

Dynamic power consumption is quadratically proportional to the supply voltage. With scaling, static power

consumption has become the dominant power component at dimensions below 0.18 μm [18]. Subthreshold leakage current flows through the channel when the transistor operates in the cut-off region, while gate leakage current occurs when the charges tunnel through the gate oxide within the MOSFET. Gate leakage current is negligible as compared to subthreshold leakage current [7]. Subthreshold leakage current is discussed in the next subsection.

B. Subthreshold leakage current

Drain current in the subthreshold regime can be modeled [7] as

$$I_{DS} \approx I_S \mathrm{e}^{\frac{q(V_{GS}-V_T)}{nkT}} \left(1 - \mathrm{e}^{-\frac{qV_{DS}}{kT}}\right), \tag{2}$$

where I_S is the current at the threshold voltage of the device, q is the charge of an electron, n is the subthreshold slope factor, k is the Boltzmann constant, and T is the absolute temperature. Note that I_{DS} is exponentially dependent on the threshold voltage, temperature, and subthreshold slope factor.

The current at the threshold voltage at different temperatures is [19]

$$I_S = \frac{W}{L}\mu C_{ox}\left(\frac{kT}{q}\right)^2 (n-1). \tag{3}$$

W and L are the CMOS dimensions, μ is the carrier mobility, and C_{ox} is the CMOS gate oxide capacitance. The subthreshold slope factor n [17] is

$$n(T) = 1 + \frac{C_{dep}(T)}{C_{ox}}, \tag{4}$$

where $C_{dep}(T)$ is the channel and bulk depletion capacitance.

The subthreshold slope [17] is

$$SS(T) = \left[\frac{\partial \log I_D}{\partial V_{GS}}\right] = \ln(10)\frac{nkT}{q} = 2.3\frac{nkT}{q}. \tag{5}$$

At cryogenic temperatures, however, due to incomplete ionization of the dopants, carrier freeze-out occurs [15]. This effect causes the SS to no longer be linearly proportional to the temperature at LHT.

With scaling, the threshold voltage significantly decreases, greatly increasing the leakage current in the subthreshold region. $I_{subthreshold}$ is the primary source of leakage current in CMOS, producing substantial power losses at room temperature.

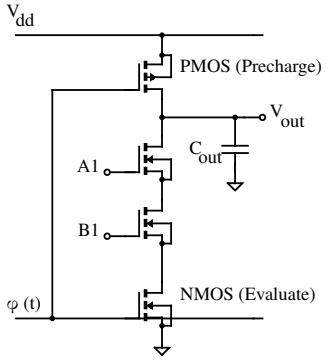

Fig. 1: Two input dynamic NAND gate.

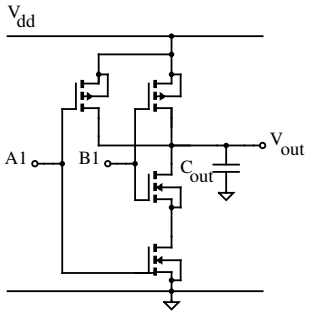

Fig. 2: Two input static NAND gate.

IV. Decay Time of Dynamic Logic at Cryogenic Temperatures

A two input dynamic NAND gate is shown in Fig. 1. The circuit consists of four transistors and a capacitive load, $C_{out} = 0.1fF$. The voltage supply V_{DD} is 1 volt. The NMOS logic network behaves as a composite switch. The output voltage V_{out} is stored on a capacitive load C_{out}. As previously noted, at RT, V_{out} decays due to leakage currents. Operation of a dynamic NAND gate where leakage current is a significant issue is exemplified by the following case. In a dynamic NAND gate during the precharge phase (see Fig. 1), $A1$ is set to 1 and $B1$ is set to 0, while the voltage across the output charges to logic 1. During the evaluation phase, although the NMOS transistors are on, the output remains at logic 1 since a signal is only transmitted if both $A1$ and $B1$ are on. The clock signal and output voltage at RT operating at a frequency of 20 GHz are shown in Fig. 3a. During the evaluation phase, the output voltage degrades due to leakage currents. If the frequency is sufficiently high, the voltage does not drop below the noise margin high (which, in this example, is 0.65 volts at RT, labeled in Figure 3 as logic 1).

The Phillips MOS11 HSpice model is used to model a 160 nm CMOS transistor operating at cryogenic temperatures [5]. Temperature dependent parameters, such as the threshold voltage, subthreshold slope factor, and carrier mobility, have been modified to fit experimental

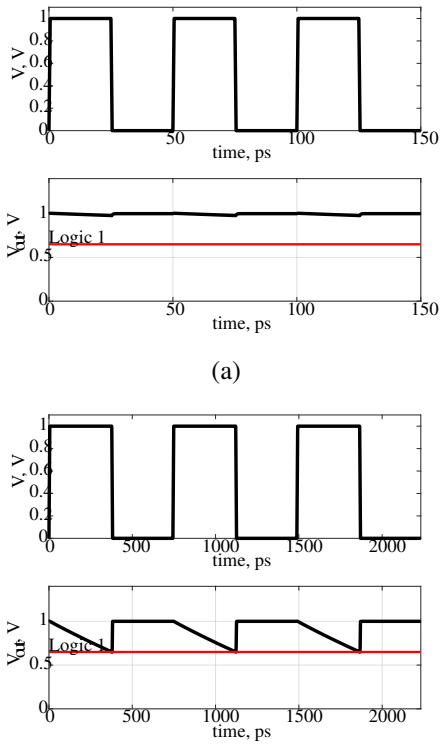

Fig. 3: Dynamic circuit operating at RT, (a) 20 GHz, and (b) 1.344 GHz. Note that the circuit operates normally at 20 GHz while 1.344 GHz is the minimum operational frequency.

data. The subthreshold slope factor n for LHT, LNT, and RT, and the carrier mobility are extracted from [17]. The subthreshold slope factor changes exponentially [17], [20], and is extrapolated at other temperatures. In thin oxide CMOS considered here, the kink effect is not present and therefore ignored [17]. For smaller technology nodes, the precise breakpoint temperature changes. However, as the temperature dependent characteristics of CMOS devices experience similar changes at cryogenic temperatures [7], the cryogenic behavior of the 160 nm CMOS technology model [5] used here can be extended to more deeply scaled, thin oxide CMOS technologies.

To determine the decay time, the subthreshold current, described by (2), is equated to the capacitor current,

$$I_S \mathrm{e}^{\frac{-qV_T}{nkT}} \left(1 - \mathrm{e}^{-\frac{qV_{out}}{kT}}\right) = C_{out} \frac{\partial V_{out}}{\partial t}. \qquad (6)$$

The decay time t of capacitor C_{out} is

$$t = \frac{C_{out} kT}{I_S q} \mathrm{e}^{\frac{qV_T}{nkT}} \ln\left[\mathrm{e}^{\frac{q}{kT}} \left(V_{dd} - V_{out}\right) - 1\right]. \qquad (7)$$

The threshold voltage is highly temperature dependent due to the carrier freezeout effect and subsequent changes in the Fermi potential [21]. The threshold voltage increases by about 30% when the temperature decreases from 300 K to 4 K [17]. For a 1 volt system, the threshold voltage at RT is 0.25 volts and at LHT is 0.33 volts [22].

V. Temperature Breakpoint of Static and Dynamic Logic

The operating temperature at which dynamic logic (Fig. 1) is preferable to static logic (Fig. 2) is discussed here as the breakpoint temperature. The range of temperature being considered is between 4.2 K (LHT) and 300 K (RT). Operation of dynamic circuits at LHT, LNT, RT, and at certain transitional temperatures are described, and the breakpoint temperatures between static and dynamic logic are discussed in this section.

Dynamic circuit operation at a specific temperature depends upon the frequency of operation. If the dynamic logic cannot operate at a specific temperature and frequency due to leakage currents, static logic is preferred. This temperature-frequency point where the output voltage of the dynamic logic drops below the noise margin high is the breakpoint temperature. To determine this breakpoint temperature, (7) is evaluated at different temperatures and frequencies.

Based on (7), the decay time of V_{out} for $V_T = 0.25$ volts and $T = 300$ K is 0.414 ns. The minimum frequency to correctly operate at room temperature is analytically determined to be 1.209 GHz. In simulation, the minimum frequency of operation is 1.344 GHz, within 11% of the analytically determined frequency. The simulated output voltage at this frequency is shown in Fig. 3b. During the evaluation phase, the charge on the output capacitor drops below the threshold voltage. In the next stage, this voltage is no longer at logic 1. 1.344 GHz represents a decay time of 0.372 ns. The difference between the simulation and analytic solutions for the decay time is 10%. These delay times are listed in Table I.

Table I: Operating frequency at different temperatures

Temperature	**Minimum Frequency**		**% Error**
	(Simulated)	**(Analytic)**	
300 K (RT)	1.209 GHz	1.344 GHz	10.0%
90 K	49.9 MHz	56.8 MHz	12.1%
77 K (LNT)	29.7 MHz	33.6 MHz	11.6%
4.2 K (LHT)	DC	DC	—

The breakpoint temperature at different frequencies is shown in Fig. 4. The breakpoint temperature-frequency characteristic is exponential, as described by (7). A scaled version of the temperature-frequency characteristic at temperatures below 100 K is shown in Fig. 5.

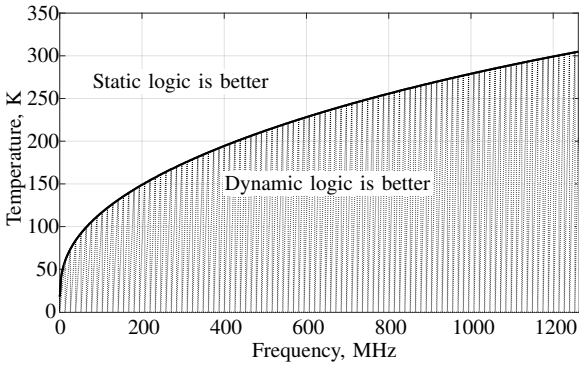

Fig. 4: Breakpoint temperature at which dynamic logic is preferable to static logic at different frequencies, 160 nm CMOS technology.

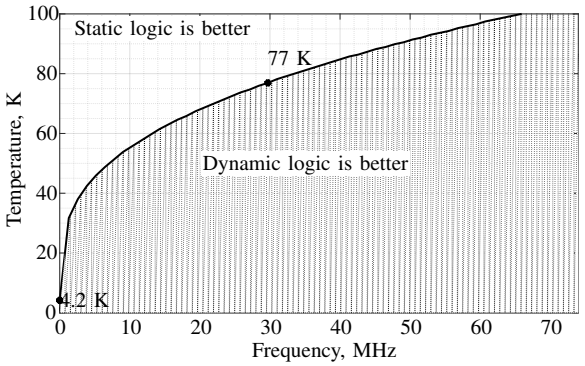

Fig. 5: Breakpoint temperature below 100 K at which dynamic logic is preferable to static logic at different frequencies.

As noted in Fig. 4, when operating at RT at frequencies below 1.344 GHz, the charge leaks away before arrival of the following clock pulse. An example of this condition is shown in Fig. 6a, where the frequency is 50 MHz. Note that the charge on the output capacitor has completely leaked away during the evaluation phase. The temperature should be below 90 K to maintain proper operation at this frequency (50 MHz), as depicted in Fig. 5. At these lower frequencies, static logic is necessary. At lower temperatures, the frequency at which dynamic logic functions correctly can be decreased. As the temperature approaches liquid nitrogen, the breakpoint curve becomes steep due to the exponential nature of the subthreshold leakage current. At 77 K, dynamic logic should be used when operating at frequencies above 29.7 MHz.

Note that the frequency can be further reduced at lower temperatures, allowing dynamic logic at 4.2 K to operate at DC. In comparison to dynamic logic operating at RT and 50 MHz, the same circuit at LHT exhibits no drop in voltage at 50 MHz, as shown in Fig. 6b, agreeing with the analytic solution. Dynamic logic is therefore

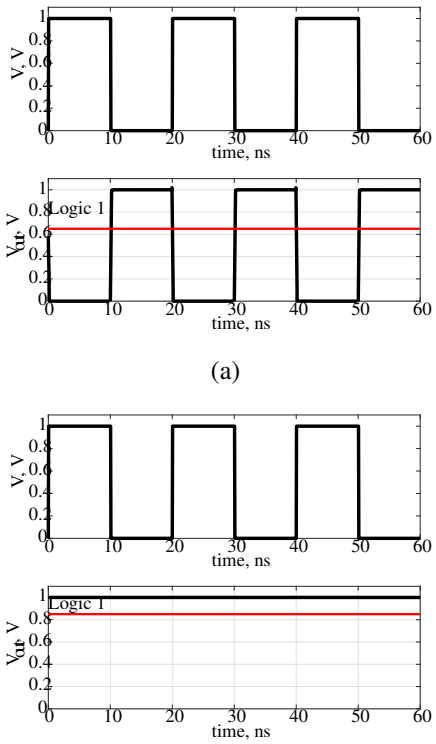

Fig. 6: Dynamic circuit operating at 50 MHz, (a) RT, and (b) LHT. The circuit produces an incorrect output at RT, while the circuit operates properly at LHT.

preferable at LHT.

DC operation, however, is available at temperatures higher than LHT. The charge leakage time at different temperatures is shown in Fig. 7. The concept of application age is introduced, where the age of the application indicates the time during which a circuit has to retain sufficient charge to maintain the logic state. As shown in Fig. 7, the application age is one month at 5.5 K, one year at 4.6 K, and three years at 4.5 K. Therefore, if system operation requires an age of three years, the circuit should be operated at or below 4.5 K.

Summarizing, as the frequency increases from 1 Hz to 1.209 GHz, the breakpoint temperature increases, respectively, from 11 K to 300 K, as shown in Fig. 4. Therefore, if the circuit operates below 1.209 GHz at a temperature above 300 K, static logic should be used. Dynamic logic can operate at 1 Hz at temperatures below 11 K and at DC below 4.5 K, as illustrated in Figs. 5 and 7.

VI. Conclusions

Interest in cloud computing has been growing, demanding energy efficiency. Due to the stationary nature of these platforms, cloud computing can support

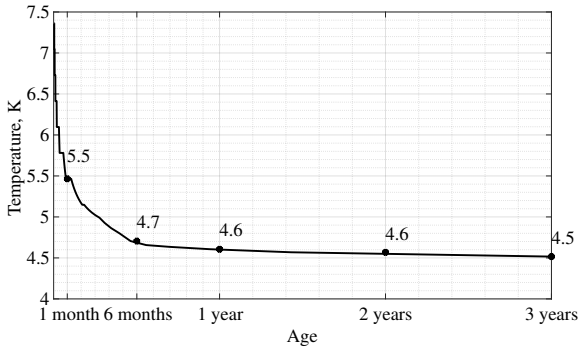

Fig. 7: Age of application at different temperatures to maintain DC operation.

cryogenic operation. This characteristic suggests the use of dynamic logic in cloud computing centers operating at cryogenic temperatures and high frequencies while dissipating low power. The primary objective of this paper is to clarify at which temperature and frequency dynamic logic is preferable to static logic.

Dynamic logic operating from liquid helium temperature to room temperature is considered here. The performance of dynamic circuits operating at the transitional temperatures between room temperature and liquid helium temperature are evaluated at several frequencies. At liquid helium temperature, dynamic circuits can operate at DC. Dynamic logic is therefore preferable over static logic at any frequency if operated at LHT. At higher temperatures, the time during which the charge leaks away is exponentially reduced. Furthermore, if DC operation requires holding the charge for one month or less, the temperature can be increased from LHT to 5.5 K. Dynamic logic is preferable at temperatures below 11 K when operated above 1 Hz. At liquid nitrogen temperature, dynamic logic is preferable when operating above 29.7 MHz. Above 1.209 GHz, dynamic logic can be used at any temperature.

REFERENCES

[1] J. P. Uyemura, *CMOS Logic Circuit Design*, Springer, 2002.

[2] A. Akturk *et al.*, "Device Modeling at Cryogenic Temperatures: Effects of Incomplete Ionization," *IEEE Transactions on Electron Devices*, vol. 54, no. 11, pp. 2984–2990, October 2007.

[3] A. Van Der Ziel, "Thermal Noise in Field-Effect Transistors," *Proceedings of the IRE*, vol. 50, no. 8, pp. 1808–1812, August 1962.

[4] Y. Feng *et al.*, "Josephson-CMOS Hybrid Memory With Ultra-High-Speed Interface Circuit," *IEEE Transactions on Applied Superconductivity*, vol. 13, no. 2, pp. 467–470, July 2003.

[5] N. Zhuldassov and E. G. Friedman, "Cryogenic Dynamic Logic," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1–5, October 2020.

[6] L. Wanhammar, *DSP Integrated Circuits*, Elsevier, 1999.

[7] H. Homulle, L. Song, E. Charbon, and F. Sebastiano, "The Cryogenic Temperature Behavior of Bipolar, MOS, and DT-MOS Transistors in Standard CMOS," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 263–270, January 2018.

[8] A. Jonscher, "Semiconductors at Cryogenic Temperatures," *Proceedings of the IEEE*, vol. 52, no. 10, pp. 1092–1104, October 1964.

[9] R. W. Keyes, E. P. Harris, and K. Konnerth, "The Role of Low Temperatures in the Operation of Logic Circuitry," *Proceedings of the IEEE*, vol. 58, no. 12, pp. 1914–1932, December 1970.

[10] G. B. Craig and S. S. Sesnic, "Investigations of Field Effect Transistors at Cryogenic Temperatures," Texas University Austin Electronics Research Center, Technical Report, January 1970.

[11] S. Sesnic and G. Craig, "Thermal Effects in JFET and MOSFET Devices at Cryogenic Temperatures," *IEEE Transactions on Electron Devices*, vol. 19, no. 8, pp. 933–942, August 1972.

[12] A. R. Tokuda and P. Lauritzen, "MOSFET Thresholds at 4.2 K Induced by Cooling Bias," *IEEE Transactions on Electron Devices*, vol. 21, no. 9, pp. 606–607, September 1974.

[13] B. Lengeler, "Semiconductor Devices Suitable for Use in Cryogenic Environments," *Cryogenics*, vol. 14, no. 8, pp. 439–447, August 1974.

[14] R. L. Maddox, "P-MOSFET Parameters at Cryogenic Temperatures," *IEEE Transactions on Electron Devices*, vol. 23, no. 1, pp. 16–21, January 1976.

[15] Y. Feng *et al.*, "Characterization and Modelling of MOSFET Operating at Cryogenic Temperature for Hybrid Superconductor-CMOS Circuits," *Semiconductor Science and Technology*, vol. 19, no. 12, p. 1381, October 2004.

[16] J. C. Whitaker, *The Electronics Handbook*, CRC Press, 2005.

[17] R. M. Incandela *et al.*, "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 996–1006, April 2018.

[18] E. Salman and E. Friedman, *High Performance Integrated Circuit Design*, McGraw-Hill Professional, August 2012.

[19] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, May 2013.

[20] A. Beckers *et al.*, "Cryogenic Characterization of 28 nm Bulk CMOS Technology for Quantum Computing," *Proceedings of the European Solid-State Device Research Conference*, pp. 62–65, September 2017.

[21] Z. Chen *et al.*, "Temperature Dependences of Threshold Voltage and Drain-Induced Barrier Lowering in 60 nm Gate Length MOS Transistors," *Microelectronics Reliability*, vol. 54, no. 6-7, pp. 1109–1114, June 2014.

[22] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOSFET threshold voltage model," *Proceedings of the IEEE European Solid-State Device Research Conference*, pp. 94–97, September 2019.