Thermal Analysis Methodology for Single Flux Quantum ICs

Ana Mitrovic and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, NY 14627
Email: ana.mitrovic@rochester.edu, friedman@ece.rochester.edu

***Abstract*—The maturing of rapid single flux quantum (RSFQ) circuits into a VLSI complexity technology has focused the need for advanced design and analysis capabilities. The significant temperature dependence of RSFQ circuits requires a thermal analysis methodology. A methodology for evaluating the thermal properties of RSFQ integrated circuits, targeting both small and large scale systems, is presented here. This methodology is comprised of a thermal model and a multi-stage partitioning algorithm. The algorithm, based on a layout of the IC, separates a circuit into blocks. The thermal model is applied to the partitioned structure, producing a netlist for thermal simulation. The algorithm is evaluated at several granularities and validated using a numerical solver. An error of less than 1% between the model and numerical simulations is achieved.**

***Keywords*—Single flux quantum, thermal model, thermal analysis, superconductive integrated circuits, superconductive digital electronics.**

I. Introduction

Since the introduction of rapid single flux quantum (RSFQ) in 1985, this technology has become the primary superconductive digital logic family [1]. In cryogenic superconductive integrated circuits the heat is produced by Josephson junctions (JJ) and resistors. Increasing frequencies and higher JJ fabrication densities lead to an increase in on-chip ambient temperature. The heating of Josephson junctions and niobium interconnects results in reduced margins and/or functional failure, along with heat load issues that affect the refrigeration characteristics [2]–[4]. Due to the sensitivity of RSFQ circuits to temperature, a methodology for exploring the thermal behavior of integrated systems has become necessary. This methodology can be used to predict the effects of heat on circuit behavior and avoid operational failure while managing the heat transfer process [1], [2], [5].

A compact thermal model of SFQ circuit structures has not been included in early analytic models of superconductive systems [3], [6]. The primary objective of this work is to provide a sufficiently accurate, computationally efficient, compact thermal model applicable to both small scale and large scale RSFQ systems. The model is applied to large scale ICs and utilizes a multi-stage partitioning algorithm for evaluating the thermal behavior. The algorithm receives a circuit layout as an input, evaluates the peak temperature of each block, and produces a netlist. A SPICE simulation of the netlist is used to determine the average temperature of each block. The methodology is calibrated for the MIT Lincoln Laboratory SFQ5ee fabrication technology [7], [8] and is validated using a 3-D numerical solver, COMSOL Multiphysics® [9]. The geometric specifications of the fabrication technology and the material parameters are described in [2].

The paper is organized as follows. In Section II, a thermal model of small scale and large scale RSFQ integrated circuits is presented. In section III, a multi-stage partitioning algorithm for analyzing the thermal behavior of RSFQ ICs is proposed. Validation of the model and algorithm is described in Section IV. The paper is concluded in Section V.

II. Thermal Model

Based on a thermal-electrical analogy [10], the model describes heat flow rate as a current source, thermal resistance as an electrical resistance, and temperature as a voltage. The thermal model of small scale RSFQ circuits is used to determine the temperature of each heating element. This model is described in Section II-A. The thermal model of a block is used within the thermal algorithm to determine the average temperature of each block. This model is described in Section II-B. The peak thermal model is described in Section II-C.

A. Thermal model of a small scale circuit

The analytic thermal model is based on a resistive mesh, as shown in Fig. 1 [11]. The current sources represent the power dissipated by each element. The heat flux of the bias resistor – the source of static power - can be evaluated as Joule heating. To evaluate the power dissipated by the JJs and shunt resistors, the RMS voltage V_{rms} across a resistively shunted junction is determined. This voltage can be obtained from SPICE simulations of the circuit or approximated assuming a triangular wave approximation [2], [12],

$$V_{rms} = 2c_s\sqrt{f\frac{\Phi_0 V_c}{3}}, \tag{1}$$

where c_s is the switching coefficient of a JJ, f is the operating frequency, Φ_0 is a single flux quantum pulse (2.07 mV·ps)

The effort depicted is supported in part by the National Science Foundation under Grant No. 2124453 (DISCOVER Expeditions) and Grant No. 2308863, Department of Energy under FOA number DE-FOA-0002950, and by a grant from Qualcomm Corporation.

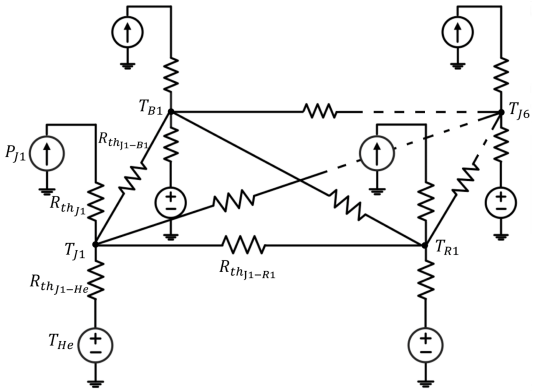

Fig. 1. Thermal model of a small scale SFQ circuit

[13], [14], and V_c is the characteristic voltage corresponding to a critically damped Josephson junction [8].

The resulting analytic expression for the heat flux sourced from a shunt resistor, based on Joule heating, is

$$q_{sh} = \frac{{V_{rms}}^2}{R_{sh}A_{sh}}. \tag{2}$$

In (2), A_{sh} is the area of the shunt resistor, and R_{sh} is the resistance of the shunt resistor, evaluated assuming a critically damped Josephson junction [2].

The heat flux due to heating a Josephson junction q_{JJ} is evaluated from the resistance of the junction in the normal state R_n [15],

$$q_{JJ} = \frac{{V_{rms}}^2 J_c}{I_c R_n}. \tag{3}$$

The thermal resistance of heating element *el* is

$$R_{th_{el}} = \frac{1}{\kappa_{el}} \frac{d_{el}}{A_{el}}, \tag{4}$$

where κ_{el} is the thermal conductivity of the material, A_{el} is the area of the element, and d_{el} is the thickness of the element. Convective cooling is modeled by the thermal resistance between the element and the cryogen,

$$R_{th_{el-He}} = \frac{1}{h_{eff_{el}}} \frac{1}{\alpha_{el} A_{el}}. \tag{5}$$

In (5), $h_{eff_{el}}$ is the effective heat transfer coefficient of the element, estimated from the resistance of the vertical heat paths [2]. Parameter α_{el} is a unitless coefficient that describes the increase in the effective area of an element cooled due to the lateral dispersion of heat [2], [3].

The inter-node thermal resistance consists of three parts,

$$\begin{aligned} R_{th_{el1-el2}} = &\frac{R_{thb}}{A_{el1}} + \frac{R_{thb}}{A_{el2}} \\ &+ \frac{1}{\kappa_{mat}} \frac{s_{el1-el2}}{\left(\frac{d_{el1}+d_{el2}}{2}\right) \cdot \max\left(w_{el1},\ w_{el2}\right)}. \end{aligned} \tag{6}$$

The first two components of the thermal resistance are the thermal boundary resistance at the interface between the elements and the medium. The third component is the thermal resistance of the material between heating elements. In (6), κ_{mat} is the thermal conductivity of the material conducting heat between elements $el1$ and $el2$, w_{el1} and w_{el2} is, respectively, the width of element $el1$ and $el2$, and $s_{el1-el2}$ is the distance between the elements.

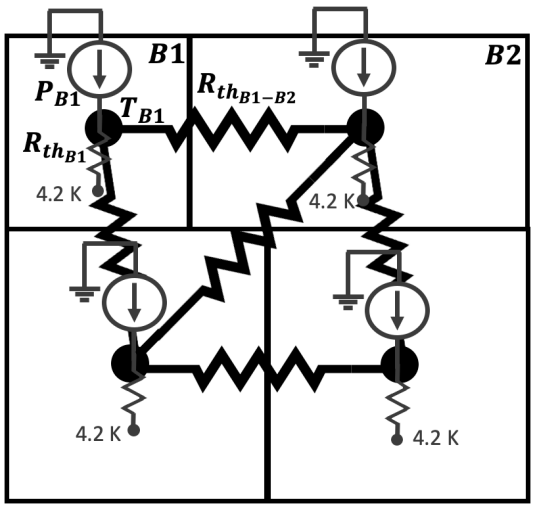

Fig. 2. Block level thermal model of RSFQ ICs. P_{B1} represents the power produced by block B1, $R_{th_{B1}}$ is the thermal resistance of block B1, and $R_{th_{B1-B2}}$ is the thermal resistance of the path between blocks B1 and B2. The temperature of block B1 T_{B1} is evaluated as the voltage at node B1.

B. Thermal model of block

The thermal model of a block is portrayed in Fig. 2. The power dissipated within a block is the total power dissipated by all of the heating elements within the block,

$$P_{block} = \Sigma P_{JJ} + \Sigma P_{shunt} + \Sigma P_{bias}. \tag{7}$$

The thermal resistance of each block, aggressor or victim, is

$$R_{th_{block}} = \frac{1}{A_{block} h_{eff}}, \tag{8}$$

where A_{block} is the area of the block.

To model heat conduction between blocks, the thermal resistance between adjacent blocks is introduced. The thermal resistance between two blocks, B1 and B2, either victims or aggressors, is

$$R_{th_{B1-B2}} = \frac{1}{\kappa_{mat}} \frac{s_{B1-B2}}{(d_{heating\_layers})w}. \tag{9}$$

s_{B1-B2} is the physical distance between the center of the blocks. $d_{heating\_layers}$ is the thickness of the material layers where the heating elements (JJs and resistors) are located. w is the width of the boundary between two blocks.

The thermal resistance between two adjacent blocks, where B1 is an aggressor block and B2 is a victim block, is

$$R_{th_{B1-B2}} = \frac{1}{\kappa_{mat}} \frac{s_{elB1-B2}}{(d_{heating\_layers})w}. \tag{10}$$

$s_{elB1-B2}$ is the physical distance between the boundary of the nearest heating element within the aggressor block B1 and the center of the victim block B2.

C. Peak thermal model

The peak thermal model of the aggressor blocks is based on the thermal model of a small scale circuit, as described in Section II-A [2]. The increase in temperature of the largest heater within a block is

$$\Delta T_{el} = \frac{P_{el}}{h_{eff_{el}} \alpha_{el} A_{el}}. \tag{11}$$

The heat in those victim blocks that do not contain heat generating elements originates from neighboring aggressor blocks. At the site of the highest temperature inside a victim block, the increase in temperature is [17], [18]

$$\Delta T(x) = \Delta T_{el_s} * e^{-\frac{x}{\eta}}, \tag{12}$$

where ΔT_{el_s} is the increase in temperature in the block directly adjacent to the heating element, x is the distance between the heating element and the edge of the victim block, and η is the thermal healing length quantifying the decrease in lateral temperature [2], [4], [18], [19].

III. Multi-stage partitioning algorithm for thermal analysis of SFQ ICs

The objective of the thermal algorithm is to produce a netlist to support the thermal simulation of large scale RSFQ ICs [4]. The algorithm produces a thermal profile of an IC based on a thermal model of the individual blocks, as well as a thermal profile of the hotspots within a small scale circuit. A flow diagram of the multi-stage algorithm is shown in Fig. 3. The aggressor partitioning stage of the multi-stage algorithm combines the heating elements into blocks. This stage of the algorithm is described in Section III-A. The victim partitioning stage of the algorithm, described in Section III-B, places the remaining circuit elements within the blocks. The average thermal algorithm, described in Section III-C, produces a netlist for thermal simulation using SPICE. The algorithm used to evaluate the peak temperature is described in Section III-D.

A. Aggressor partitioning algorithm

The temperature is greatest in the area surrounding the high power, heat generating elements. The primary objective of the aggressor partitioning stage of the algorithm is therefore to form aggressor blocks by partitioning a system into blocks composed of those nearby heating elements. The circuit layout is described as a weighted undirected graph G_a with the heating elements forming a set of graph vertices U_a. E_a is the set of edges connecting each pair of vertices. Each edge is characterized by a weight representing the Euclidean distance between nodes [20].

During the aggressor partitioning stage, the heating elements within a specific radius are clustered. A smaller radius produces a smaller block and provides local information about temperature, while increasing the granularity (and computational complexity) of the resistive mesh for SPICE simulation [4]. Once G_a is formulated, a parameter describing the minimum radius of an element r_{el} is used to characterize the complexity of a block, where subgraph $G_a^S \in G_a$ ensures that each pair of vertices $u_i, u_j \in U_a^S$,

$$w(\{u_i, u_j\}) < \ r_{el}. \tag{13}$$

The computational complexity of the aggressor partitioning stage of the algorithm is $O(|U_a|^2)$. This stage of the algorithm produces a set of aggressor blocks Q. An example of the output of the aggressor partitioning stage of the algorithm is illustrated in Fig. 4a, depicting the boundary of the heating blocks.

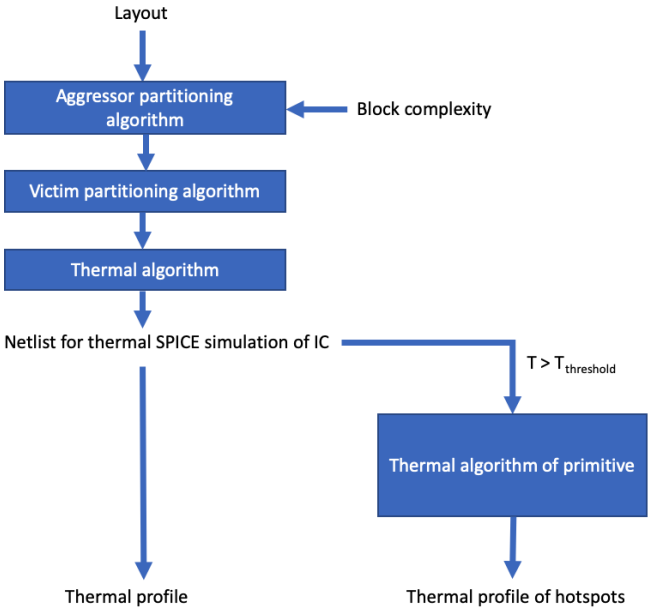

Fig. 3. Flow diagram of multi-stage thermal analysis algorithm for large scale RSFQ systems

B. Victim partitioning algorithm

After grouping the heating elements, the remaining portion of the circuit is clustered into blocks. This process is performed within the victim partitioning stage of the algorithm. The structure is represented by the set of vertices Γ formed from the coordinates of the heating blocks produced by the aggressor partitioning algorithm.

The lower coordinates of the new victim block are found from the minima of the x- and y-coordinates of the vertices. The upper coordinate of the new victim block is set by finding the nearest subsequent partitioned region [4]. After the vertices of the new victim block are added to Γ, any duplicate pairs $(x, y) \in \Gamma$ are deleted. The algorithm continues to partition the circuit into blocks until no remaining vertices in Γ exist. The computational complexity of the victim partitioning stage of the algorithm is $O(|Q|^2)$. An example of the output of the victim partitioning stage of the algorithm is illustrated in Fig. 4b, depicting the boundary of the victim blocks.

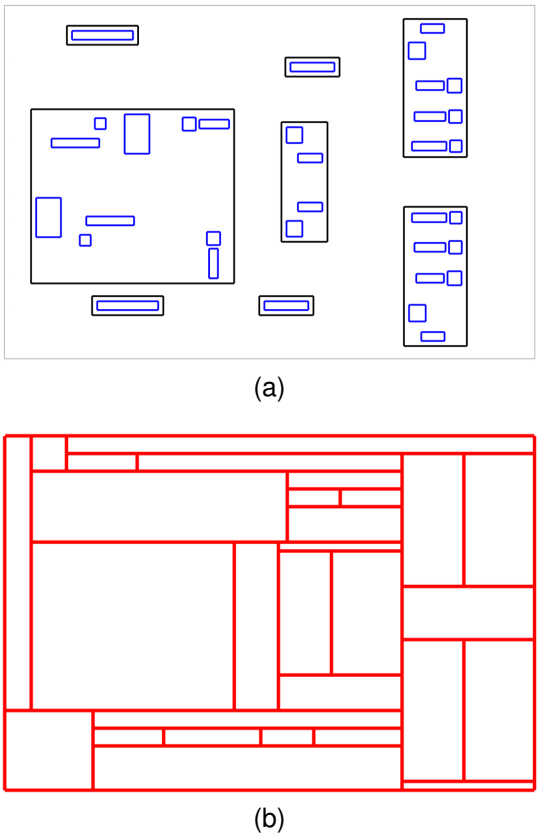

Fig. 4. Partitioning structure into blocks, (a) location of heating blocks from the aggressor partitioning stage, and (b) location of victim blocks from the victim partitioning stage

C. Average thermal algorithm

Once the boundary of all of the blocks is determined, the thermal algorithm formulates a graph from the partitioned structure. The structure can be described as a loopless undirected simple graph $G(B, R)$, where each block is represented as a node within the set of nodes B, and R is the set of thermal resistances connecting the nodes [21], [22].

The algorithm produces a netlist for thermal simulation. The temperature is evaluated by extracting the node voltages from a SPICE simulation. The computational complexity of the thermal stage of the algorithm is $O(|U_a| + |B|^2)$.

D. Peak thermal algorithm

An algorithm is presented here to evaluate the peak temperature, specifically, for hotspot detection [4]. To evaluate the peak temperature of a block, a subset of N elements $C[0...N\text{-}1]$ is extracted. The elements in C contribute to the peak temperature of a block. For each aggressor block, C is the set of heating elements within that block. For those victim blocks that do not contain heating elements, C is based on the proximity between the aggressor and victim blocks.

For each block within the partitioned structure, C is used to determine the set of element temperatures, $T[0...N\text{-}1]$. The peak thermal algorithm finds the element k within each set such that $T[k]$ is the maximum temperature within that set.

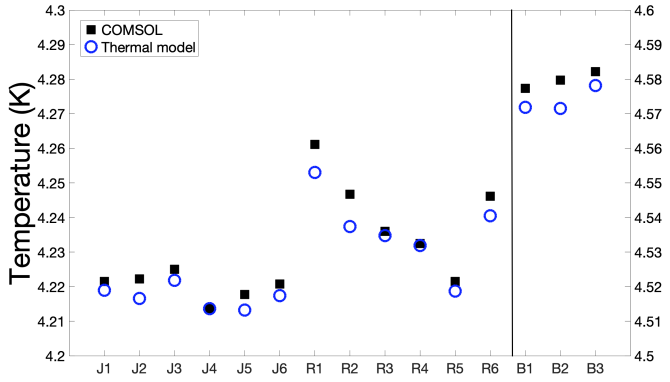

Fig. 5. Comparison of the analytic thermal model with COMSOL

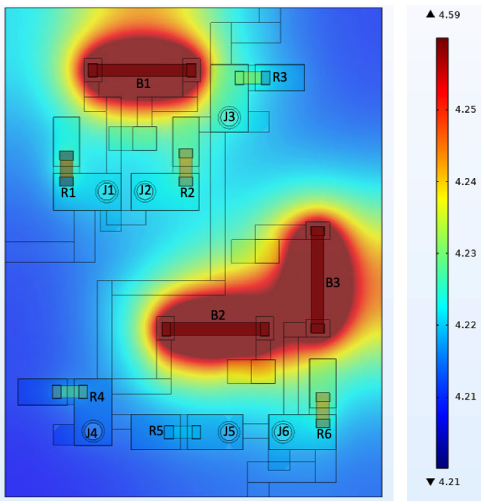

Fig. 6. Thermal profile of a D flip flop simulated in COMSOL Multiphysics. For visibility, the color bar is limited to between 4.2 K and 4.26 K. The minimum and maximum temperature is, respectively, shown at the bottom and top of the color bar.

The computational complexity of the peak thermal algorithm is $O(|U_a| + |Q| * |B \backslash Q|)$.

IV. Case Study

An RSFQ D flip flop is evaluated to validate the thermal model of a small scale circuit. The layout is based on SFQ5ee design rules [23]. The results of the thermal simulation are shown in Fig. 5. For clarity, the values on the right vertical axis are attributed to the bias resistors. The thermal profile of the D flip flop, simulated in COMSOL, is shown in Fig. 6.

The accuracy of the thermal model is listed in Table I, where $|D| = |T_{numerical} - T_{model}|$ is the absolute difference, and

$$\delta = \frac{|T_{numerical} - T_{model}|}{average(T_{numerical},\ T_{model})} \tag{14}$$

is the relative difference between the thermal model and a numerical simulator. Note that the greatest discrepancy between numerical simulation and the thermal model is 9 mK (an error of 0.2%).

TABLE I
ACCURACY OF THERMAL MODEL OF SMALL SCALE RSFQ CIRCUITS AS COMPARED TO THE NUMERICAL SIMULATOR.

Nr. of thermal resistances	$\|D\|_{ave}$ (mK)	$\|D\|_{max}$ (mK)	δ_{ave} (%)	δ_{max} (%)
135	4.3	9.4	0.1	0.22

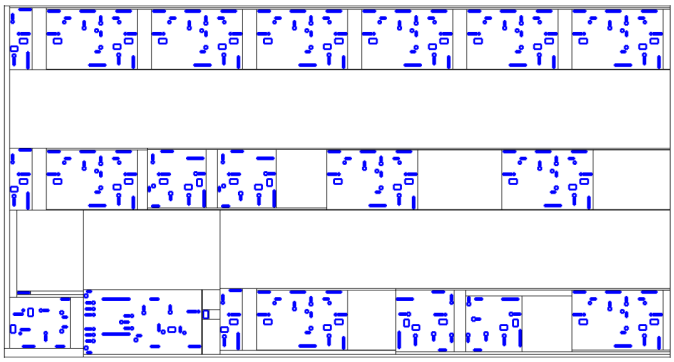

Fig. 7. Portion of the RSFQ AMD2901 used to validate the thermal model, divided into aggressor and victim blocks. The aggressor blocks contain heating elements - JJs and resistors.

The maximum increase in temperature within a D flip flop is approximately 400 mK, as shown in Fig. 6. Although this increase in temperature does not compromise the operation of the D flip flop, it does increase the heat load. This thermal model of small scale RSFQ circuits can therefore be used to analyze local hot spots within RSFQ ICs.

A portion of the AMD2901 is evaluated to validate the thermal algorithm and the block level thermal model for large scale systems. The dimensions of the structure are 380 µm x 200 µm, and the circuit contains 18 gates (155 resistively shunted Josephson junctions). The structure is divided into blocks based on the element radius r_{el} characterizing the complexity of the blocks. Element radii, 7.5 µm, 10 µm and 50 µm, are chosen to evaluate the effects of the substantial variations in block size considered in the case study. An example of a structure partitioned into blocks based on r_{el} = 7.5 µm is shown in Fig. 7. The circuit is assumed to operate at 50 GHz with a global switching coefficient of 0.5.

A comparison between the thermal model and a numerical simulator is listed in Table II. The greatest discrepancy between the average thermal model and the numerical simulation is 0.51%. Due to the averaging nature of the average thermal model, higher accuracy is produced at larger block complexities. Rather than averaging the temperature of all of the heaters within the blocks, the peak thermal model determines the temperature generated by the greatest heat producing element. The accuracy of this model therefore does not depend on the complexity of the block. The largest discrepancy between the peak thermal model and numerical simulation is 0.92%. A thermal profile depicting the average temperature for r_{el} = 7.5 µm is shown in Figure 8a. Note that for enhanced visibility the color bar in this figure is limited to between 4.2 K to 4.25 K. A thermal profile of the same structure depicting the peak temperature is portrayed in Figure 8b. The minimum and maximum temperature is shown, respectively, at the bottom and top of the color bar for both thermal profiles. The increase in average temperature for this structure is 160 mK. The increase in peak temperature for this structure is 1.66 K.

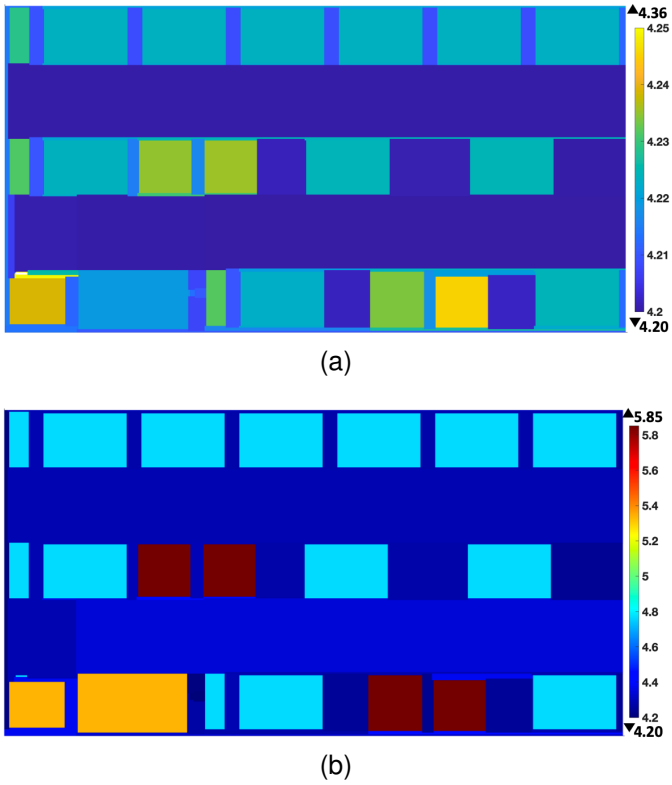

Fig. 8. Thermal profile of a portion of the RSFQ AMD2901 (r_{el} = 7.5 µm), (a) average temperature, and (b) peak temperature.

V. CONCLUSIONS

A methodology is presented in this paper for analyzing the thermal behavior of RSFQ integrated circuits, important due to the sensitivity of cryogenic RSFQ to temperature and heat load. The approach includes a compact thermal model and a multi-stage algorithm, validated against numerical simulations, to predict the thermal behavior, identify hotspots, and optimize the design of both small scale and large scale RSFQ circuits.

REFERENCES

[1] G. Krylov and E. G. Friedman, *Single Flux Quantum Integrated Circuit Design*, Springer, 2022.

[2] A. Mitrovic and E. G. Friedman, "Thermal Modeling of Rapid Single Flux Quantum Circuit Structures," *IEEE Transactions on Electron Devices*, Vol. 69, No. 5, pp. 2718-2724, May 2022.

[3] A. S. Lavine and C. Bai, "An Analysis of Heat Transfer in Josephson Junction Devices," *ASME Journal of Heat Transfer*, Vol. 113, pp. 535–543, August 1991.

[4] A. Mitrovic and E. G. Friedman, "Thermal Exploration of RSFQ Integrated Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, in press.

TABLE II
ACCURACY OF THERMAL MODEL AS COMPARED TO THE NUMERICAL SIMULATOR, COMSOL MULTIPHYSICS [9].

	Average Thermal Model				**Peak Thermal Model**			
r_{el} (μm)	$\|D\|_{ave}$ (mK)	$\|D\|_{max}$ (mK)	δ_{ave} (%)	δ_{max} (%)	$\|D\|_{ave}$ (mK)	$\|D\|_{max}$ (mK)	δ_{ave} (%)	δ_{max} (%)
50	4.50	14.33	0.11	0.34	10.85	20.15	0.24	0.47
10	4.46	20.70	0.11	0.49	14.84	32.93	0.34	0.74
7.5	5.03	21.56	0.12	0.51	14.77	39.96	0.33	0.92

[5] T. Jabbari, G. Krylov, S. Whiteley, E. Mlinar, J. Kawa, and E. G. Friedman, "Interconnect Routing for Large-Scale RSFQ Circuits," *IEEE Transactions on Applied Superconductivity*, Vol. 29, No. 5, pp. 1–5, August 2019.

[6] T. A. Ohki, J. L. Habif, M. J. Feldman, and M. F. Bocko, "Thermal Design of Superconducting Digital Circuits for Millikelvin Operation," *IEEE Transactions on Applied Superconductivity*, Vol. 13, No. 2, pp. 978–981, June 2003.

[7] S. K. Tolpygo, "Superconductor Digital Electronics: Scalability and Energy Efficiency Issues," *Low Temperature Physics*, Vol. 42, No. 5, pp. 361–379, May 2016.

[8] S. K. Tolpygo, V. Bolkhovsky, R. Rastogi, S. Zarr, A. L. Day, E. Golden, T. J. Weir, A. Wynn, and L. M. Johnson, "Advanced Fabrication Processes for Superconductor Electronics: Current Status and New Developments," *IEEE Transactions on Applied Superconductivity*, Vol. 29, No. 5, pp. 1–13, August 2019.

[9] Heat Transfer Module User's Guide, COMSOL Multiphysics® v. 5.4. COMSOL AB, Stockholm, Sweden, 2018.

[10] M. Pedram and S. Nazarian, "Thermal Modeling, Analysis, and Management in VLSI Circuits: Principles and Methods," *Proceedings of the IEEE*, Vol. 94, No. 8, pp. 1487–1501, August 2006.

[11] W. Huang, M. R. Stan, K. Skadron, K. Sankaranarayanan, S. Ghosh, and S. Velusamy, "Compact Thermal Modeling for Temperature-Aware Design," *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 878–883, June 2004.

[12] C. J. Fourie, "Extraction of DC-Biased SFQ Circuit Verilog Models," *IEEE Transactions on Applied Superconductivity*, Vol. 28, No. 6, pp. 1-11, September 2018.

[13] A. M. Kadin, *Introduction to Superconducting Circuits*, Wiley-Interscience, 1999.

[14] A. M. Kadin, C. A. Mancini, M. J. Feldman, and D. K. Brock, "Can RSFQ Logic Circuits be Scaled to Deep Submicron Junctions?," *IEEE Transactions on Applied Superconductivity*, Vol. 11, No. 1, pp. 1050–1055, March 2001.

[15] S. K. Tolpygo, V. Bolkhovsky, T. J. Weir, A. Wynn, D. E. Oates, L. M. Johnson, and M. A. Gouker, "Advanced Fabrication Processes for Superconducting Very Large-Scale Integrated Circuits," *IEEE Transactions on Applied Superconductivity*, Vol. 26, No. 3, pp. 1–10, April 2016.

[16] G. Krylov and E. G. Friedman, "Design Methodology for Distributed Large-Scale ERSFQ Bias Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 11, pp. 2438-2447, November 2020.

[17] M. Asheghi, M. N. Touzelbaev, K. E. Goodson, Y. K. Leung, and S. S. Wong, "Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates," *Journal of Heat Transfer*, Vol. 120, pp. 30–36, February 1998.

[18] J. Lee, SB Kim, A. Marconnet, M. A. A. in't Zandt, M. Asheghi, H. S. Philip Philip Wong, and K. E. Goodson, "Thermoelectric Characterization and Power Generation Using a Silicon-on-Insulator Substrate," *Journal of Microelectromechanical Systems*, Vol. 21, No. 1, pp. 4–6, February 2012.

[19] E. Pop, V. Varshney, and A. K. Roy, "Thermal Properties of Graphene: Fundamentals and Applications," *MRS Bulletin*, Vol. 37, No. 12, pp. 1273-1281, November 2012.

[20] R. Bairamkulov, T. Jabbari, and E. G. Friedman, "QuCTS—Single-Flux Quantum Clock Tree Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 41, No. 10, pp. 3346-3358, October 2022.

[21] R. Bairamkulov and E. G. Friedman, *Graphs in VLSI*, Springer, 2023.

[22] N. Zhuldassov, R. Bairamkulov, and E. G. Friedman, "Thermal Optimization of Hybrid Cryogenic Computing Systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 31, no. 9, pp. 1339-1346, September 2023.

[23] S. S. Meher, C. Kanungo, A. Shukla and A. Inamdar, "Parametric Approach for Routing Power Nets and Passive Transmission Lines as Part of Digital Cells," *IEEE Transactions on Applied Superconductivity*, Vol. 29, No. 5, pp. 1–7, August 2019.