Delay Generation Based on Differential Sawtooth Waveforms for 3-D Heterogeneous Integration

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***Abstract*—Emerging technologies in the semiconductor industry, such as three-dimensional integration and sub-10 nm technology nodes, have revolutionized the next generation of microelectronic systems. Deeply scaled systems demand both coarse and precise compact delay elements for applications such as time-to-digital conversion, digital timers, and phase compensation. A sawtooth waveform-based delay generation technique for periodic clock signals is proposed here to produce large, high resolution delays. The technique uses a differential sawtooth waveform to extract delay information from the input signal.**

I. Introduction

Classical delay generation approaches have consisted of cascaded delay elements, producing a desired output from dozens of tap points. These techniques rely on the inherent propagation delay of inverters, where each stage can be sized to deliver a specific delay [1], [2]. By chaining multiple inverters, a cumulative delay is achieved. This technique provides a highly scalable and modular approach to delay generation. The near universal applicability of cascaded inverters is noteworthy, as the approach is suitable for almost any technology. The increasing speed of deeply scaled technologies, however, makes large (or coarse) delay lines composed of cascaded inverters impractical in terms of physical area and power dissipation.

Alternatively, digitally controlled delay lines based on NAND gates offer programmable delay intervals [2]. This method utilizes the logical behavior of a NAND gate to create a variable delay. Using thermometer-based encoding [2], control circuitry dynamically and finely tunes the delay of these structures. The digital controllability supports applications demanding dynamic adjustments to delay intervals, such as digital delay locked loops (DLL) [3]. This approach, however, raises similar concerns (area and power) as cascaded inverters.

A delay generation technique where large delay ranges are achieved without requiring multiple delay elements is the focus of this paper. The sawtooth waveform-based delay element proposed here exploits certain waveform characteristics to achieve precise delay intervals. By generating a sawtooth waveform and extracting the relevant crossing points, a controlled delay is realized. A single ended sawtooth-based delay line is proposed in [4], where two single ended sawtooth waveforms provide delay information. To improve reliability and compatibility for heterogeneous three-dimensional (3-D) integration, a delay generator is proposed here that uses differential sawtooth waveforms to perform phase detection and delay generation for a DLL [5].

A DLL based on the proposed approach is explored, specifically targeting the synchronization of 3-D interfaces [6]. Phase compensation circuitry is an effective tool to address timing variations between tiers (planes). The large number of interfaces between tiers in 3-D integration, such as the example shown in Fig. 1, necessitates timing solutions that can be scattered across the system to address sensitive clock paths between tiers. To achieve precise timing across a heterogeneous 3-D system, it is crucial to enable compact, reliable, and low complexity circuits that can maintain fast locking times.

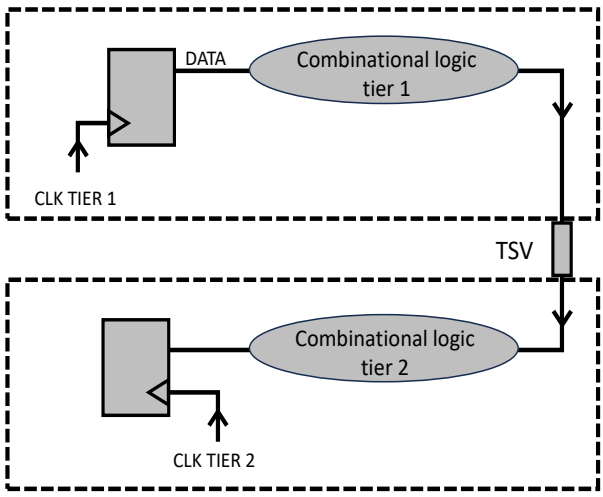

Fig. 1: Synchronization of a 3-D interface.

The rest of this paper is organized as follows: The general principle of sawtooth delay generation is described in Section II. A delay locked loop that utilizes the proposed delay generation technique in a 3-D clock tree is described in Section III. Simulation results are discussed in Section IV. Some

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conclusions are drawn in Section V.

II. Sawtooth delay generation

A sawtooth delay generator is based on the timing relationship between a periodic input square signal (such as a clock signal), a differential pair of sawtooth-shaped waveforms produced by the periodic signal, and a reference voltage. As illustrated in Fig. 2, four crossing points between the reference voltage and the sawtooth waveform occur within one period. To produce a delay relative to the input signal, the proposed circuit generates an output signal at one of these four crossings. Assuming that the output is generated when the sawtooth waveforms cross the reference voltage on the rising edge, selecting $V^+_{Sawtooth}$ generates a delay between $t = 0$ and $t = T_{period}/2$, where T_{period} is the period of the input signal. Selecting $V^-_{Sawtooth}$ generates a delay between $t = T_{period}/2$ and $t = T_{period}$, thereby achieving a full period delay range. To maintain the period of the input signal, the delay generator extracts the pulse width from the same set of signals. From Fig. 2, points 1 and 3 are always half a period apart. Similarly, points 2 and 4 are also half a period apart. The crossing points on the falling edge of the opposite sawtooth waveform can therefore be used to extract the timing information for a pulse width with a 50% duty cycle.

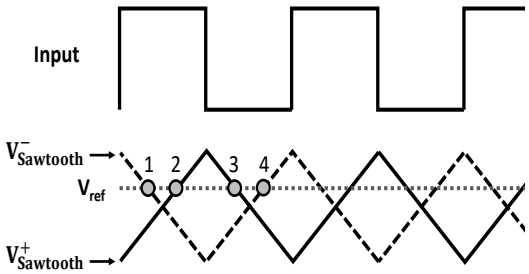

Fig. 2: Four sets of crossing points for V_{ref}. Points 1 and 3 and points 2 and 4 are always half a period apart. A digital control signal determines which pair of crossing points is used.

To generate a sawtooth waveform, a differential integrator is used [7]. The waveforms are produced by charging and discharging two capacitors, C_1 and C_2. The sawtooth generator is depicted in Fig. 3. Note that if charging and discharging one of the capacitors is stopped, a reference voltage can be maintained. In the circuit depicted in Fig. 3, C_2 maintains the reference voltage after some delay T_{delay}. The reference voltage is guaranteed to be within the voltage swing of the sawtooth waveform. By setting the reference voltage in this manner, the pulse width delay can no longer be extracted from the same set of sawtooth waveforms.

III. Sawtooth-Based Delay Locked Loop

To evaluate the efficiency of the proposed delay generation technique, a DLL utilizes the proposed sawtooth delay generator as both a phase detector and a delay generator. Delay locked loops are attractive tools for 3-D synchronization

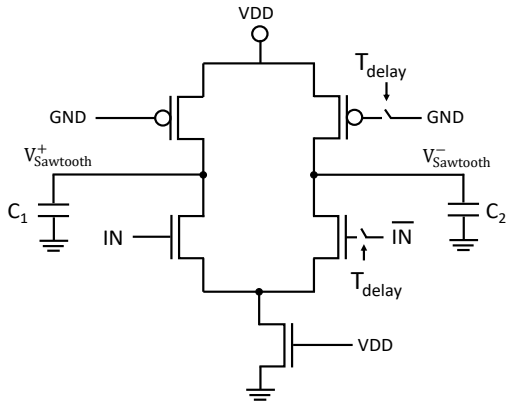

Fig. 3: Integrator sawtooth generator with differential output. At T_{delay}, capacitor C_2 is no longer charged or discharged by the integrator, maintaining the reference voltage.

given the ability to dynamically synchronize clock signals on separate tiers [8]–[10].

A DLL within a 3-D environment is shown in Fig. 4. The DLL receives a clock signal from two separate tiers and outputs a clock signal at the root of one of the clock trees. The DLL shown in Fig. 4 synchronizes signals at the clock sink level to maintain accurate point-to-point synchronization.

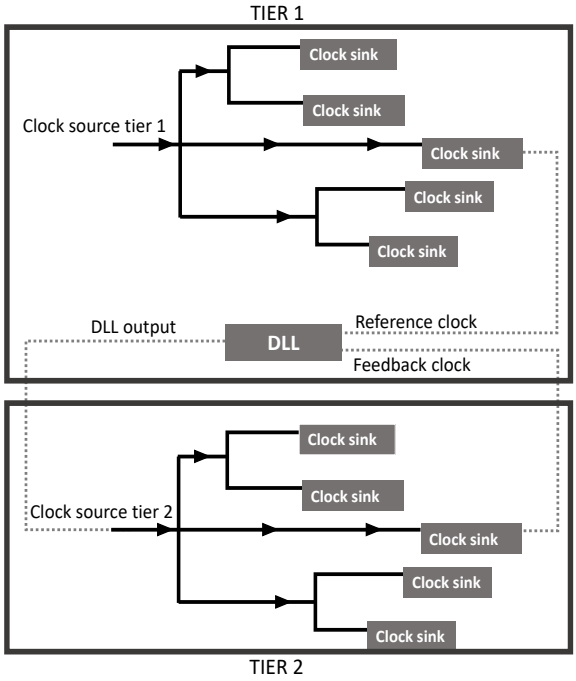

Fig. 4: 3-D clock tree with a DLL synchronizing the clock sinks.

The remainder of this section describes the sawtooth DLL. The locking stage, where the DLL determines the appropriate delay, is described in Section III-A. The circuit components of the sawtooth DLL are described in Section III-B.

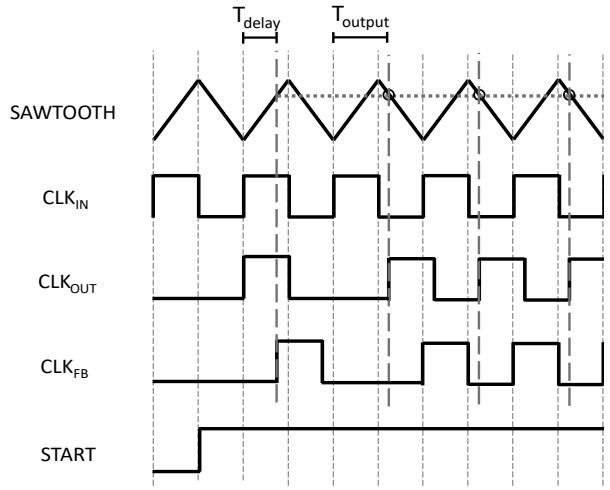

Fig. 5: Sawtooth DLL waveforms depicting the ideal timing relationship between the reference clock signal, DLL output, and feedback clock signal.

A. Sawtooth DLL locking delay stage

A timeline of the DLL locking stage is shown in Fig. 5, where a reference clock signal with a 50% duty cycle and period T_{period} with an associated sawtooth waveform are assumed. The waveform rises when the clock signal is high and falls when the clock signal is low, as depicted in the first two waveforms shown in Fig. 5. After the START signal goes high, the circuit sources a pulse from the reference clock signal which propagates through the clock tree. Once the clock signal arrives at the input of the feedback network, the signal is delayed by propagation delay T_{delay} of the clock tree. This signal is represented in Fig. 4 as the feedback clock. The circuit maintains the voltage level of the sawtooth waveform V_{offset} at the rising edge of the feedback signal. The delay inserted by the DLL into the clock path occurs when the sawtooth waveform crosses V_{offset} in the opposite direction. This event is indicated as T_{output}. This relationship is described by the following expressions,

$$\begin{aligned} T_{output} &= T_{delay} + 2(T_{period}/2 - T_{delay}) \\ &= T_{period} - T_{delay},\ for\ T_{delay} < T_{period}/2, \end{aligned} \quad (1)$$

$$\begin{aligned} T_{output} &= T_{delay} + 2(T_{period} - T_{delay}) \\ &= 2T_{period} - T_{delay},\ for\ T_{delay} > T_{period}/2. \end{aligned} \quad (2)$$

After the output signal propagates through the clock tree, the feedback signal is delayed by T_{delay}. The feedback is delayed, with respect to the input, by either T_{period} or $2T_{period}$, depending upon the value of T_{delay}.

B. Sawtooth DLL circuit components

To perform the operation described in Section III-A, the sawtooth DLL must generate a sawtooth shaped waveform, maintain the voltage offset, and delay the reference signal by T_{output}. The circuit components used to realize these functions are described in this section.

1) Sawtooth generation: Two pairs of sawtooth waveforms are generated by the DLL. The first waveform aligns the rising edge, while the second waveform aligns the falling edge. The pulse generation stages detect when the sawtooth waveform crosses V_{offset}, generating a pulse to change the output state. The output generation stage changes the output clock waveform based on the timing characteristics of the previous stages. The signal that controls charging and discharging C_1 switches from CLK_{IN} to $\overline{\text{CLK}_{\text{IN}}}$. This switch maintains the same timing relationship between the sawtooth waveform and V_{offset}, as shown in Fig. 5. The switch causes a voltage overshoot in C_1 but returns to the average value of the voltage after a few cycles. The integrator is shown in Fig. 6a, and the relevant waveforms are shown in Fig. 6b. Note that STOP_{INT} transitions high at the rising edge of the first CLK_{FB} pulse, and the multiplexer switches the input of C_1. The integrator generator responsible for aligning the falling edge has a similar architecture where STOP_{INT} transitions high at the falling edge of the first CLK_{FB} pulse.

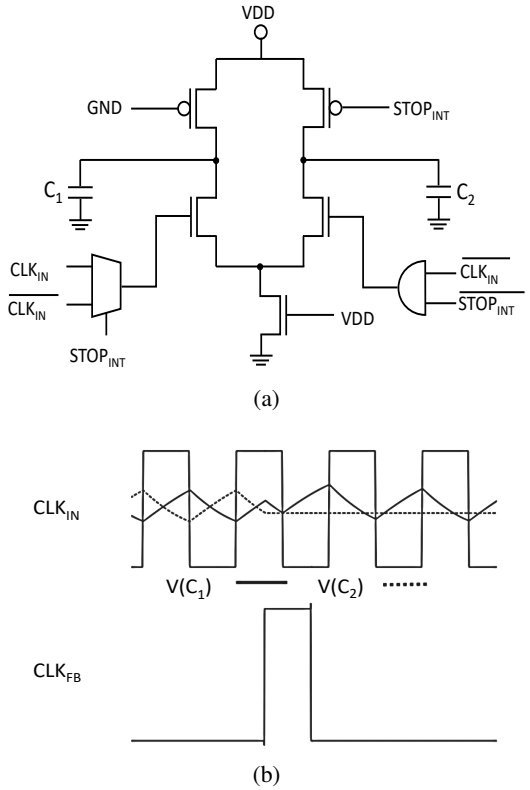

Fig. 6: Integrator stage, (a) integrator circuit, and (b) sawtooth waveform with relationship to CLK_{IN} and CLK_{FB}.

2) Pulse and output generation: The DLL generates a delayed version of the input clock based on the timing information provided by the sawtooth waveform. The pulse generation stage is composed of a pulse generator and a level detector, which is achieved by a differential amplifier with C_1

and C_2 at the input. The pulse generator is composed of an inverter chain and a NAND gate. The pulse generator provides a pulse with sufficient hold time for the toggle flip flop. The toggle flip flop is the output generator, switching between high and low depending upon whether the flip flop receives a pulse from the rising edge detector or from the falling edge detector. These components are illustrated in Fig. 7.

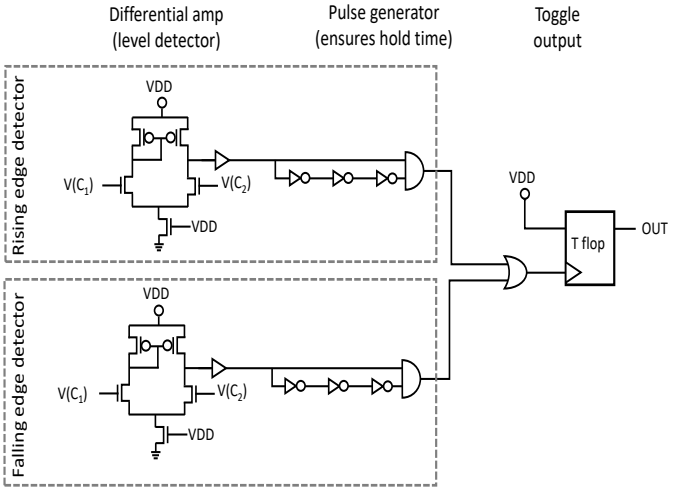

Fig. 7: Level detectors for rising and falling edges, pulse generators, and toggle output stage.

IV. Performance

The sawtooth DLL is evaluated in the 7 nm predictive technology model [11]. The reduction in skew for different T_{delay} is shown in Fig. 8. The DLL successfully attenuates the skew between the feedback and reference across a range of delay from 0 ps to 950 ps. Note two exceptions: at 0 ps (*i.e.*, when T_{delay} is a multiple of T_{period}) and at 450 ps (*i.e.*, when T_{delay} is a multiple of $T_{period}/2$). This failure in attenuating the skew arises from the sawtooth waveforms crossing V_{offset} near the peak of the waveform. These peaks occur at T_{period} (for the 0 ps case) and at $T_{period}/2$ (for the 450 ps case). In these cases, an external control unit must determine whether the sawtooth DLL applies no delay or inverts the reference clock signal, depending upon which peak is closer to V_{offset}.

The differential nature of this approach offers additional benefits such as robustness to temperature corners. The delay generation is evaluated at -50°C, 27°C, and 125°C. As shown in Fig. 9a, the extreme temperature corners affect the amplitude of the sawtooth waveforms; however, the timing relationship between V_{offset} and the sawtooth waveforms is maintained despite the wide range in temperature. The feedback signal CLK_{FB} for the three cases is shown in Fig. 9b. Any difference at the output due to the temperature corners is minimal (a maximum difference of 1.3%). The circuit exhibits an average power dissipation of 510 μW at -50°C, 613 μW at 27°C, and 991 μW at 125°C.

Due to leakage current from the capacitors, the skew between the input clock signal and the feedback clock signal accumulates. The amount of accumulated skew depends upon the type of capacitor. The relationship between the skew accumulation and leakage current is shown in Fig. 10. High-K trench capacitors exhibit lower leakage current, below 10 nA [12], while a TSV with a 3-D metal-insulator-metal capacitor can exhibit a leakage current above 10 nA [13].

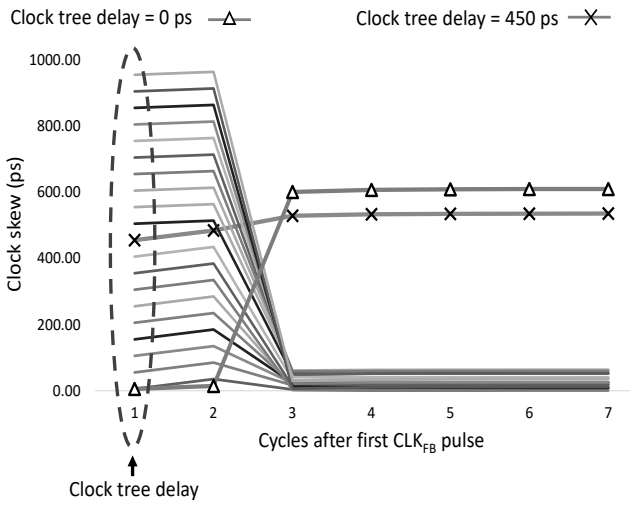

Fig. 8: Attenuation of clock skew due to inital T_{delay}.

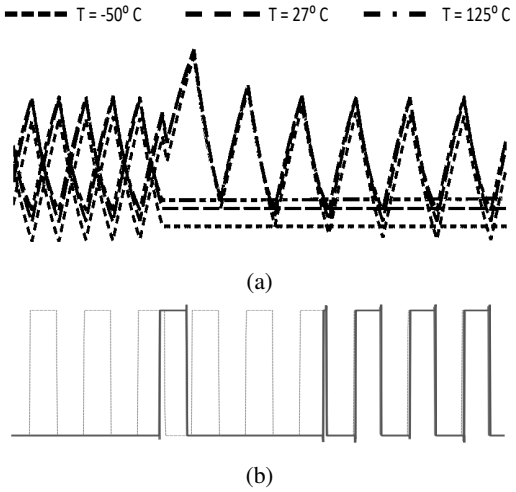

Fig. 9: Performance of the sawtooth DLL at the extreme temperature corners.

V. Conclusions

A sawtooth based technique is proposed in this paper for accurate delay generation. The technique is verified by a delay locked loop that performs periodic synchronization between clock sinks at different tiers of a 3-D system. The differential sawtooth waveforms provide robustness against extreme temperature corners, a major concern in 3-D systems. The effectiveness of this approach is dependent on the leakage current of the capacitors that generate the sawtooth waveforms.

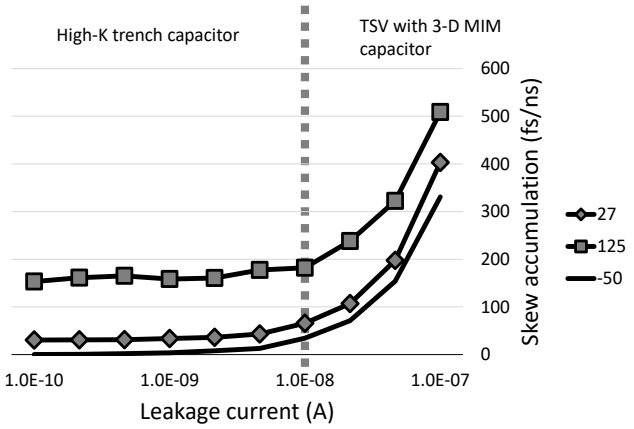

Fig. 10: Effect of leakage current on skew accumulation

This dependence on leakage current is accentuated in a DLL as the reference voltage is maintained by one of the capacitors used to generate the sawtooth waveforms.

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