Partitioning SFQ Circuits for Current Recycling with Driver-Receiver Pair Insertion

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***Abstract*—Large scale single flux quantum systems often require substantial bias currents, which can strain the power delivery system and potentially lead to system failure. To address this issue, current recycling is employed as a method to reduce bias currents by dividing similar circuits into multiple partitions. Each block is allocated a separate ground plane and biased in series with the ground of another block connected to the bias current supply of the next block. To facilitate the transfer of clock or data signals between these blocks, which are isolated by different ground planes, driver-receiver pairs (DRPs) are utilized. The concept of current recycling is extended here to heterogeneous circuits, where circuit blocks have different bias currents. In systems with small bias imbalances, dummy Josephson transmission lines can be used, while resistive trees are effective for systems with significant bias imbalances. To address the challenges of large bias imbalances caused by DRP insertion, a partitioning algorithm tailored for heterogeneous circuits is proposed. This algorithm combines the Kernighan–Lin and Fiduccia-Mattheyses methods to minimize the number of DRPs. The effectiveness of the heterogeneous partitioning algorithm is demonstrated on several ISCAS'89 benchmark circuits. By integrating resistive tree and DRP insertion, the approach achieves an average reduction of 29.7% in bias current, a 31% reduction in DRPs, and a 40.9% reduction in the number of Josephson junctions.**

***Index Terms*—Current recycling, serial biasing, driver-receiver pair, resistive tree, heterogeneous circuit**

I. Introduction

A major challenge in single flux quantum (SFQ) circuits is the need for large bias currents, which can strain the current distribution system and potentially cause system failure [1]. To mitigate this issue, serial biasing of SFQ circuits has been proposed [2]–[4], offering a method to reduce the overall current demand of SFQ systems. In serial biasing, similar circuits are divided into multiple blocks through a process called partitioning, where each block is placed on a separate ground plane, as depicted in Fig. 1. These blocks, referred to here as partitions, are placed on different ground planes. A driver-receiver pair (DRP) facilitates signal transfer between partitioned blocks on isolated ground planes [5]. The DRP uses inductive coupling to ensure that no physical electrical connection exists between the driver and receiver, preserving the isolation of the ground planes due to the difference in ground voltage [3].

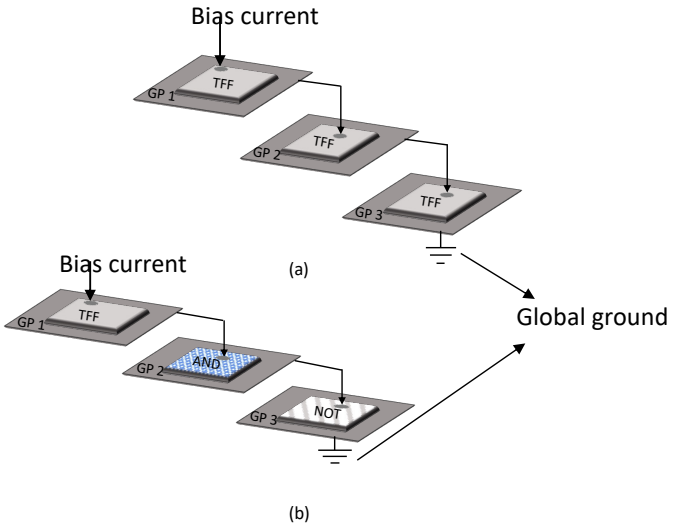

Fig. 1: Serially biased circuits, (a) homogeneous circuits, and (b) heterogeneous circuits

Serial biasing has previously been applied to circuits with similar bias current (I_b) requirements (homogeneous circuits), as exemplified by serially biased Josephson transmission lines (JTL) [6], [7] and serially biased toggle flip flops [8]. The bias current of each block is similar to avoid overbiasing or underbiasing a circuit block placed on a different ground plane. In [9]–[11], this approach is extended to heterogeneous circuits, which consist of different logic gates with varying current requirements. Serial biasing in heterogeneous circuits introduces several challenges, such as unequal bias currents, described as a bias imbalance, which is the difference between the maximum and minimum bias current required by a partitioned block. A major challenge is partitioning the ground plane in a heterogeneous system to ensure that the bias current required by each partition is similar, as illustrated in Fig. 1. While efficient biasing techniques are addressed in [9], [10], issues related to DRP area overhead, clock distribution, and bias current balancing after DRP insertion remain prominent. In this paper, an algorithm for partitioning heterogeneous circuits after DRP insertion while applying a bias balancing

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technique based on a resistive tree is proposed.

The structure of the paper is as follows: a brief description of serial biasing is discussed in Section II. Partitioning constraints are explored in Section III. A partitioning algorithm for heterogeneous circuits after DRP insertion using resistive tree bias balancing is presented in Section IV. Some conclusions are drawn in Section V.

II. Serial Biasing in Heterogeneous Circuits

A brief overview of different types of heterogeneous circuits and bias current distribution methods is provided in Section II-A. The overhead of serial biasing in heterogeneous circuits after DRP insertion is discussed in Section II-B.

A. Overview of heterogeneous circuits

Several bias balancing techniques are proposed [10] to prevent overbiasing and underbiasing in partitioned blocks to support heterogeneous current recycling. In serial biasing of heterogeneous circuits, the circuit is initially partitioned into distinct blocks. After partitioning, multiple inter-partition transfers, which are signals between adjacent blocks, are necessary. Ground plane partitioning for current recycling is discussed in [9], [12], where the number of inter-partition edges and bias imbalances is estimated prior to inserting the DRPs.

The number of signals transferred across an adjacent partition is non-uniform across a system. After DRP insertion, the bias imbalance between the partitions significantly increases. This imbalance is further aggravated by the differences between the driver and receiver circuits, each requiring different bias currents. Dummy JTLs are inserted to absorb excess bias current on each isolated ground plane. Assuming the 10 kA/cm² MIT Lincoln Lab SFQ5EEE fabrication process, the maximum critical current (I_c) for a Josephson junction (JJ) is 500 μA [13]. A two junction JTL can absorb a maximum bias current of 700 μA, which is 70% of I_c [13], [14]. The larger the bias imbalance, the more balancing JTLs are required, increasing the overhead to achieve current recycling. To eliminate the need for dummy JTLs to reduce this overhead, a resistive tree bias balancing method is adopted.

Heterogeneous circuits are classified into two categories based on whether the bias margins overlap or do not overlap. Circuits with a small bias imbalance fall under the overlap bias margin classification, where the operating margins of the bias current of different partitioned blocks share a common range, as shown in Fig. 2a. In contrast, no common range occurs in the operating margin of the bias current in the non-overlap bias margin category [10] and often in circuits with a large bias imbalance. Different techniques are used to balance the bias current in these two circuit classifications. Those circuits within the overlap bias margin can operate without additional balancing techniques but need to tolerate low bias margins. To enhance this margin, JTLs are inserted within the partitioned blocks with a bias current lower than the maximum current supplied to the blocks [10]. The JTL circuits consume the excess bias current supplied to each circuit block. For those circuits classified under the non-overlap bias margin, a resistive tree is used to balance the bias current. The resistive tree provides additional bias current to the individual partitioned blocks, arranged in ascending order of bias current requirement, as depicted in Fig. 2b.

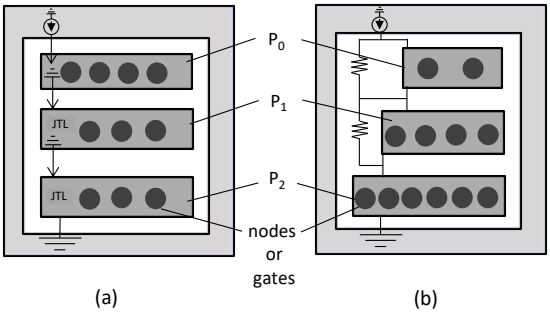

Fig. 2: Serially biased partitioned circuit blocks (P_n) on isolated ground planes illustrate the current distribution process, (a) overlap bias current classification with dummy JTLs, and (b) non-overlap bias current classification with a resistive tree

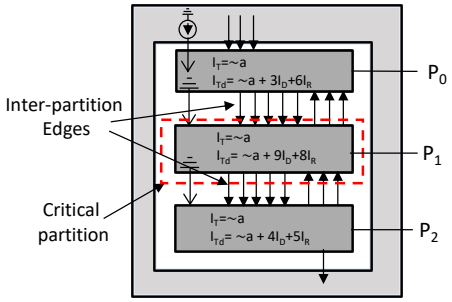

Fig. 3: Inter-partition edges illustrating the critical partitions

B. Overhead of heterogeneous circuits with JTL padding after inserting DRPs

In serial biasing of heterogeneous systems, a graph G = (N, E) is formed, where N is the set of vertices representing the nodes (logic gates and splitters), and E is the set of edges representing the wires connecting the nodes. The graph is initially partitioned into K distinct parts, where K denotes the number of partitions. Multiple inter-partition edges between nodes across adjacent partitions are necessary. These inter-partition edges transfer signals that ensure effective communication between the nodes in each partition. The number of inter-partition edges entering and exiting each partition varies, producing a larger bias imbalance after DRP insertion. The total bias current required by the nodes and DRPs within each partition is

$$I_{\mathrm{Td}} = I_T + n_d(I_D) + n_r(I_R), \tag{1}$$

where I_T, I_D, and I_R represent, respectively, the total bias current of all of the nodes in a partition before DRP insertion, the bias current of the drivers, and the bias current of the receivers, while n_d and n_r represent, respectively, the number of drivers and receivers. As depicted in Fig. 3, P_1 contains nodes with

TABLE I: Bias imbalance in modified ISCAS'89 benchmark circuits before and after DRP insertion in systems with a different number of partitions. The number of partitions is denoted by K, and the inter-partition wires are edges.

BC	I_b (mA)	K=2					K=3					K=4				
		Edges	Before		After		Edges	Before		After		Edges	Before		After	
			B_{imb} (%)	I_{bmax} (mA)	B_{imb} (%)	I_{bmax} (mA)		B_{imb} (%)	I_{bmax} (mA)	B_{imb} (%)	I_{bmax} (mA)		B_{imb} (%)	I_{bmax} (mA)	B_{imb} (%)	I_{bmax} (mA)
s27	16.9	13	0.33	8.6	3.5	16.3	17	1.19	6	32.11	14.9	35	3.12	6.4	37.4	18.1
s382	337	294	0.02	152	0.12	247	496	0.21	101	43.52	253	705	1.01	78.5	50.1	232.3
s420	349	267	0.01	175	0.59	266	523	0.23	104	40.05	271	719	0.26	89.2	48.2	249
s641	412	372	0.03	206	0.19	347	682	0.10	164	38.3	394	942	0.23	104	49	327
s1423	868	912	0.01	434	0.7	722	1644	0.08	265	47.44	768	2293	0.03	219	62.84	711

inter-partition edges from two adjacent partitions. n_d and n_r are larger in P_1, as noted by the I_{Td} equations included in Fig. 3. Eight edges from the adjacent partitions flow into P_1, and nine edges flow from P_1 to the adjacent partitions. The bias current required by P_1 is therefore significant, causing a large imbalance in bias current between the adjacent partitions after inserting DRPs. This phenomenon makes P_1 critical, hence called the critical partition. Since only one adjacent partition exist in P_0 and P_2, these partitions are considered non-critical. After DRP insertion, the imbalance in bias current between the partitions increases, requiring the insertion of additional JTLs. Despite operating within the overlap bias margin, the issue of large bias imbalances can persist. Bias current imbalances in modified SFQ benchmark circuits with a varying number of partitions are listed in Table I. The bias current imbalance, denoted as B_{imb}, before DRP insertion is notably lower than after DRP insertion in those cases where K exceeds two. The maximum bias current I_{bmax} supplied to the system is also greater after inserting DRPs. This situation causes a large imbalance in P_1 after DRP insertion.

III. Partitioning constraints

As discussed in Sections I and II, similar bias current is required in both homogeneous and heterogeneous circuits with an overlap bias margin. Partitioning heterogeneous circuits using a resistive tree requires unequal bias current. Therefore, constraints to optimally partition heterogeneous circuits with a significant bias imbalance are explored. These partitioning constraints are described as follows: the ascending order constraint is discussed in Section III-A, the inter-partition interconnect constraint is presented in Section III-B, and the critical partition constraint is explored in Section III-C.

A. Ascending order of bias current

In heterogeneous current recycling, where the bias current is unequal with a large imbalance, a resistive tree is used. The partitions are arranged in ascending order of bias current to ensure that the partition with the largest bias current is connected to the global ground, as depicted in Fig. 4 where P_i represents the partition. The ascending order of bias current ensures a balanced current distribution. This constraint also reduces the number of inter-partition edges by placing more nodes in the larger partition which, in turn, reduces the number of DRPs.

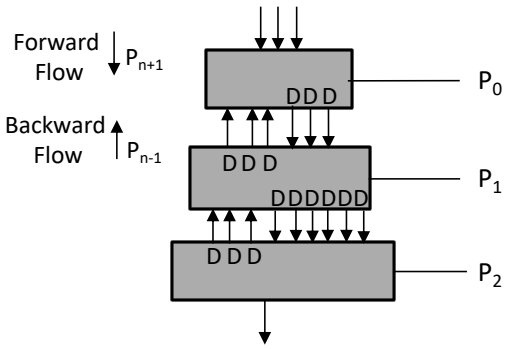

Fig. 4: Forward and backward edges between partitions using the resistive tree current distribution method. The direction of flow determines where the driver is placed since the driver requires four JJs and the receiver requires two JJs. The driver is placed, respectively, at the origin of the forward and backward edges.

B. Inter-partition interconnect

The number of inter-partition edges is a major constraint when partitioning different nodes. For example, after the initial placement of nodes, if a node in P_0 is connected to a node in P_2 rather than through P_1, as illustrated in Fig. 4, both nodes can be placed within the same partition to avoid unnecessary inter-partition edges. This constraint minimizes the number of inter-partition edges and, consequently, the number of DRPs. The constraint relies on gain g_i, the change in the number of inter-partitions when a node is moved from one partition to another partition. This constraint is incorporated into the partitioning algorithm as

$$g_i = \sum_{n_j \in \text{Adj}(n_i)} \left(1 - 2 \cdot \delta(p_i, p_j)\right), \tag{2}$$

$$\delta(p_i, p_j) = \begin{cases} 1, & \text{if } p_i = p_j \\ 0, & \text{if } p_i \neq p_j, \end{cases} \tag{3}$$

where g_i represents the gain of node n_i, indicating the change in inter-partition edges if n_i is moved to another partition. p_i and p_j denote, respectively, the partition of nodes n_i and n_j, with n_j being a neighboring partition to n_i. Adj(n_i) refers to the set of neighboring nodes connected to n_i.

C. Critical partition

The partition between the first and final partitions is critical, as described in Section II-B for K>2. The final two partitions

Algorithm 1: Enhanced Graph Partitioning with K Partitions

Input: Graph $G = (N, E)$, K, $MinL_{IB}$
Result: Best inter-partition edges $\{P_0, P_2, \ldots, P_{K-1}\}$ with ascending order of I_b, $n_i \in P_k$, and number of forward and backward edges per partition.

Initialization:
$\text{Best}_{\text{score}} \leftarrow \infty$, $\text{Best}_{\text{imb}} \leftarrow \infty$, $\text{S} \leftarrow 100$, $\text{MinL}_{\text{IB}} \leftarrow 40$;
for *seed* $= 1, \ldots, S$ **do**
  RNG.init(seed);
  Shuffle N;
  for *each* $n_i \in N$ **do**
    $n_i \leftarrow P_{(i \mod K)}$;
  end
  Sort partitions $\{P_0, P_1, \ldots, P_{K-1}\}$ by $\sum_{n_i \in P_k} \text{Bias}(n_i)$ (ascending);
  Reassign partitions;
  Compute gains g_i;
  while *partitioning improves* **do**
    for $p = 0, \ldots, K-1$ **do**
      $n_{\text{max\_gain}} = \arg\max_{n_i \in (N_p \setminus \text{locked})} g_i$;
      if $n_{max\_gain} = \emptyset$ **then**
        break;
      end
      Move $n_{\text{max\_gain}}$ to partition $P_{(p+1) \mod K}$;
      Lock $n_{\text{max\_gain}}$ or treat as relaxed;
      Recompute g_i;
    end
  end
  Compute B_{imb};
  if $B_{imb} < MinL_{IB}$ **then**
    move n_i between P_{K-2} and P_{K-1};
  end
  Redo B_{imb};
  if *adjusted* $B_{imb} \geq MinL_{IB}$ **then**
  end
  Compute $E_{p_i \neq p_j}$;
  $E_{p_i \neq p_j} = \sum \delta(p_i \neq p_j)$ for $(i, j) \in E$ and $|i - j| > 1$;
  if $E_{p_i \neq p_j} < Best_{score}$ *and* $B_{imb} \geq L_{IBmin}$ **then**
    Update $\text{Best}_{\text{score}}$ and Best_{imb};
    Store as the best;
  end
end

are the most crucial due to the large number of inter-partition edges since these partitions exhibit the greatest bias current and number of nodes due to arranging the bias current in ascending order. Between the final two partitions, a large bias imbalance must be managed. The bias imbalance between the critical and non-critical partitions must be sufficiently large to ensure that the ascending order constraint is maintained after DRP insertion. This large imbalance is necessary only in the final two partitions, where the penultimate partition is critical, and the final partition is not, as illustrated in Fig. 4. The imbalance between these final two partitions is enforced with $B_{imb} < L_{IBmin}$, where L_{IBmin} represents the minimum bias imbalance between the final two partitions, and B_{imb} is

$$B_{imb} = \frac{\text{Bias}(P_{K-2}) - \text{Bias}(P_{K-1})}{\text{Bias}(P_{K-1})} \tag{4}$$

IV. Partitioning algorithm in heterogeneous circuits

The partitioning algorithm for heterogeneous circuits utilizes a combination of the Kernighan–Lin (KL) partitioning algorithm and Fiduccia-Mattheyses (FM) partitioning algorithm [16]–[18]. The KL algorithm is used for the initial partitioning step, allowing for K parts, while the FM algorithm determines the gain to enhance the efficiency of the inter-partition edges. The algorithms are implemented in Python 3. Modified ISCAS'89 benchmark circuits contain several logic gates, splitters, inverters, and connections between the gates and splitters. The algorithm parses the benchmark circuits to differentiate nodes from edges and forms a graph $G = (N, E)$, where the nodes represent logic gates and splitters, and the edges represent each connecting wire. Based on the critical partition constraint discussed in Section III-C, the bias imbalance between the final two partitions can be adjusted by the minimum bias imbalance, denoted by L_{IBmin}. The distribution of nodes is

$$N_1 \cup N_2 \cup \cdots \cup N_K = N \quad \text{and} \quad N_i \cap N_j = \emptyset \quad \forall i \neq j, \tag{5}$$

the combination of all nodes in all partitions is equal to the total nodes in the graph, and no single node should be present in more than one partition.

The algorithm partitions the nodes in the graph into K parts based on the bias currents and creates an adjacency list (neighboring nodes) from the edges. These partitions are arranged in ascending order of bias current. For each node, the gain is determined, and the node is moved between partitions to minimize the number of inter-partition wires. The node is locked within the partition with the highest gain. The optimal solution is the partition with the fewest inter-partition edges after a specified number of iterations, denoted as S in Algorithm I. The algorithm also determines the forward flow (edges from P_i to P_{i+1}) and backward flow (edges from P_i to P_{i-1}) of the inter-partition wires for each partitioned graph, which is of primary importance due to the difference in bias current between the driver and receiver.

The optimal number of inter-partition edges along with the number of external inputs and outputs of each benchmark circuit determine the number of DRPs to be inserted into a system. Since the driver and receiver of the DRP exhibit different bias current demands, and the direction of the inter-partitioned wires is known, the DRP bias current for each partition can be estimated from the following expression,

$$\text{IDR}_{P_i} = (nF_i + nB_{i+1} + nO_i)I_D + (nB_i + nF_{i-1} + nI_i)I_R, \tag{6}$$

where nF_i is the number of forward edges. nB_i is the number of backward edges. nO_i and nI_i are, respectively, the number

TABLE II: Partitioning after DRP insertion on SFQ modified ISCAS'89 benchmark circuits [15], K=4

BC	Similar I_B				Resistive Tree (unequal I_B)				
	Edges	I_{bmax} (mA)	JJ Overhead		Edges	I_{bmax} (mA)	JJ Overhead	Reduction in DRP %	Reduction in JJ overhead %
			DRP	JTL			**DRP**		
s382	705	232.3	4308	236	514	227	3084	37.16	47.34
s420	719	249	4452	244	560	256	3360	28.39	39.76
s641	942	327	5790	328	737	350	4422	27.82	38.35
s1423	2293	711	13758	784	1756	798	10536	30.58	38.00

of outputs and inputs in partition P_i. The number of forward and backward edges in each partition supports an accurate estimate of the total bias current and bias imbalance between adjacent partitions.

As listed in Table II, the number of edges in the resistive tree partition is reduced due to the relaxed constraint of equal bias current. This relaxation allows for additional nodes in larger partitions, reducing the total number of DRPs. Since the resistive tree distributes sufficient current to each block during the current recycling process, the need for dummy JTLs is eliminated, lowering the number of JJs. The number of inter-partition edges is also reduced during the resistive tree partitioning process. The average reduction in bias current when partitioning with equal bias current constraints after DRP insertion is higher by 2.9%. Considering the average reduction in the number of inter-partition edges is 31% and JJ overhead is 40.9%, the resistive tree partition method outperforms equal bias current partitioning of heterogeneous circuits after DRP insertion.

V. Conclusions

A partitioning scheme is proposed for efficient current recycling in heterogeneous SFQ circuits. This approach uses a resistive tree to address the significant bias imbalance that arises after DRP insertion. To effectively assign the gates to different partitions using a resistive tree, a partitioning algorithm is introduced. The algorithm mitigates the effects of the critical partitions, which contribute to substantial bias imbalances due to inter-partition connections between adjacent blocks. To resolve this issue, the partitioning algorithm incorporates a critical partition constraint that ensures a minimum bias imbalance between the final two partitions. Specific constraints are applied to support the ascending bias current required by the resistive tree bias balancing method, eliminating the need for inserting dummy JTLs. This current biasing technique efficiently recycles current throughout the SFQ system using a resistive tree while minimizing the number of DRPs by reducing inter-partition connections.

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