AN ENVIRONMENT SENSITIVE CIRCUIT DESIGN TECHNIQUE FOR MODELING VLSI INTERCONNECT IMPEDANCES

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Abstract

A circuit design technique is described that permits accurate modeling of interconnect load impedances by specifically considering the circuit's environment. Appropriate interconnect models are selected on a node-by-node basis as a function of the relative magnitude of the individual device and interconnect resistive and capacitive components at each given node so as to maintain a given level of accuracy while optimizing computational efficiency. This technique has been baselined around the Hughes Aircraft 1.25 μm CMOS/SOS VHSIC technology and is currently being automated for structured VLSI design applications.

I. Introduction

High performance VLSI circuit design is typically highly iterative in nature and requires extensive detailed circuit analysis. This analysis must consider the extreme range of environmental conditions that the circuit is specified to operate within. Over these wide range of conditions, from best case to worst case, the device output impedance will vary appreciably with respect to its interconnect load impedance. Therefore, the lumped interconnect impedance network used to model the resistive and capacitive interconnect impedance should be chosen so as to maintain simulated performance accuracy and save circuit area while conserving CPU compute efficiency. This paper describes a circuit impedance relationship that permits one to select an optimally modeled lumped interconnect impedance network as a function of its circuit environment.

II. Circuit Analysis

It is common practice within the industry to use a lumped one-section ladder network to model distributed RC transistor interconnect load impedances. This lumped network guarantees an upper bound (i.e., worst case) time delay for critical path timing analysis and a minimum number of nodes for CPU computational efficiency. However, this upper bound can lead to appreciable circuit overdesign which increases with the relative magnitude of the interconnect delay between register elements in a data path. Thus, a more accurate representation of the interconnect delay is useful when designing higher performance circuits. The design technique described within this paper is directly oriented to high speed and high precision VLSI circuit design.

A. Definition of Symbols

W_p: PMOS transistor width (micrometers)

R_W: Lumped wire resistance (ohms)

C_W: Lumped wire capacitance (femtofarads)

r_t: Lower bound transistor output impedanc

$$\left[\frac{1}{\text{max drain conductance}} \right] \text{ (ohms)}$$

C_t: Lumped transistor input capacitance (femtofarads)

V_{in}: MOS transistor input voltage (volts)

V_{tp}: PMOS transistor threshold voltage, negative for enhancement devices (vol

V_{dsp}, V_{dsn}: PMOS and NMOS transistor sourc drain voltages, respectively (volts)

V_{DD}: Power supply voltage (volts)

α: Relative Modulation Factor between r_t a W_p (dimensionless)

β_p: PMOS transistor gain factor $\left[\frac{\text{farads}}{\text{volt-secor}} \right.$

$C_T = \frac{C_t}{C_W}$, ratio of the transistor input capacitance to the lumped wire capacitance

$R_T = \frac{r_t}{R_W}$, ratio of the transistor output resistance to the lumped wire resistance

B. Calculation of Device Output Impedance

The output impedance of a driver is a compl lationship among several factors such as vice's process parameters, the shape of the transient waveform, the output resistiv capacitive loading, the circuit environ conditions, and the layout design style. r_t bounds are used in this design tec since they are more sensitive to capac interconnect impedances and therefore re greater accuracy of the distributed interc impedance models.

The drain current equations of a typical ra buffer represented in Figure 1 which corre to a minimum PMOS output impedance are de below [1]:

$$I_{dsp} = -\beta_p[(V_{in} - V_{DD} - V_{tp})(V_{dsp}) - \tfrac{1}{2}V_{dsp}^2] \quad \left.\begin{array}{l} V_0 \le V_{in} - V_{tp} \\ 0 \le V_{in} \le V_{tn} \end{array}\right. \qquad (1)$$

$$I_{dsn} = 0 \quad \left.\begin{array}{l} |V_{tp}| \le V_0 \le V_{DD} \end{array}\right. \qquad (2)$$

where,

$$\beta_p = \frac{W_p}{L_p}\,\mu_p C_{ox} \qquad (3)$$

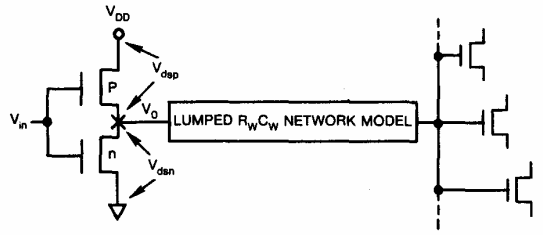

Figure 1: CMOS Ratioed Buffer Driving Interconnect and Device Loads

The above equations define the drain current of a PMOS transistor when operating in the linear mode and the drain current of an NMOS transistor when operating in the cutoff mode. Since the PMOS and NMOS devices are assumed to be geometrically ratioed, the drain-to-source current is equivalent for both the P-channel and N-channel devices when operating in the same I-V region. As the input voltage V_{in} and the drain voltage V_{dsp} approach zero, the PMOS lower bound output impedance will approach r_t as described in equations (4) and (5) below.

$$(r_t)^{-1} = \lim_{V_{in},V_{dsp}\to 0} \frac{dI_{dsp}}{dV_{dsp}} = \beta_p(V_{DD} + V_{tp}) \qquad (4)$$

Therefore,

$$r_t = \frac{1}{\beta_p(V_{DD} + V_{tp})} \qquad (5)$$

The tranconductance of a device, $(r_t)^{-1}$, is linearly dependent upon its width as described by equations (3) and (5). The larger the device width, the greater its transconductance. This linear relationship has been extensively studied in terms of its technology dependence and can be described in a useful, intuitive way as shown in equation (6). Thus, for a given value of α, process, and bias conditions, r_t can be determined directly from Wp.

$$r_t = \frac{1}{\beta_p(V_{DD}+V_{tp})} = \alpha\,\frac{1}{\beta_p V_{DD}}$$

$$r_t = \alpha\,\frac{1}{W_p}\,\frac{L_p}{\mu_p C_{ox}}\,\frac{1}{V_{DD}}$$

where,

$$\alpha = \frac{V_{DD}}{V_{DD} + V_{tp}}$$ and $\beta_p V_{DD}$ is described in [2].

Thus, α is always larger than one for a typ enhancement PMOS device since V_{tp} is nega Equation (6) can be characterized in terms o 1.25 µm CMOS/SOS technology for a given ci environment. This example assumes nominal cess parameters, 85°C, 5 volt power supply no total dose radiation. Thus, one can dete the device output impedance directly from a device geometric width under a given set o vironmental conditions. This is exemplifi equation (8) below and the inverse relatio between r_t and W_p is graphically depict Figure 2.

$$r_t = \alpha\,\frac{(18.7 \times 10^3)}{W_p}$$

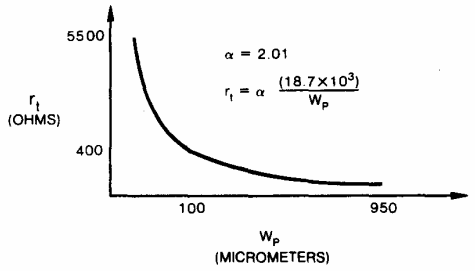

Figure 2: Buffer Output Resistance as a Fun of P-Channel Geometric Width

The Relative Modulation Factor α is sensiti the circuit environment as depicted in Ta since both V_{DD} and V_{tp} can change. V depicted in Table 1 as an implicit functi temperature, process parameters, and radia This table has been calibrated for our 1. CMOS/SOS VHSIC technology. Values of r_t been determined as described by Sakurai [3] the added sophistication of considering th fects of varying circuit environmental condi on the value of α. Thus, for a given value an estimate of the output resistance of a ra buffer can be made and this value can be us optimally model that output node's interco impedance.

V_{DD}(V)	TEMP (°C)	PROCESS PARAMETERS	TOTAL DOSE RADIATION (Rad-Si)	α
4.5	27	BEST	NO	1.50
4.5	85	NOMINAL	NO	2.23
4.5	125	WORST	NO	2.92
4.5	125	WORST	3×10^5	3.31
5.0	27	BEST	NO	1.34
5.0	85	NOMINAL	NO	2.01
5.0	125	WORST	NO	2.61
5.0	125	WORST	3×10^5	2.92
5.5	27	BEST	NO	1.22
5.5	85	NOMINAL	NO	1.83
5.5	125	WORST	NO	2.37
5.5	125	WORST	3×10^5	2.61

Table 1: Values of the Relative Modulation Factor α as a Function of Circuit Environment

C. Selection of Optimal Interconnect Impedance Model

For each cell type in a given cell library, the input capacitive load and the output drive resistance described in terms of P-channel device width is defined in a look-up table, exemplified by Table 2. From these values and a node's extracted resistive and capacitive interconnect impedances, the ratios R_T and C_T can be computed. R_T and C_T are ratios which represent the relative magnitude of the transistor impedance, r_t and C_t, to its interconnect impedance, R_W and C_W, as described in equations (9) and (10). A second

$$R_T = \frac{r_t}{R_W} \tag{9}$$

$$C_T = \frac{C_t}{C_W} \tag{10}$$

CELL TYPE	C_t (fF)						W_p (MICROMETERS)		
INVA	22						6.8		
ANDA	28	28					14.2		
DFF	57	38					17	17	
ADD2	264	87	88	84	85		17	17	
⋮									

Table 2: Cell Library Look-up Table Defining Input Capacitance and P-Channel Device Width for Each Cell Type

look-up table, shown in Table 3, is then used to select an optimum lumped network model, examples of which are given in Figure 3, for each net under study. Table 3 is constructed based on the relative error of the signal transition time between a one-section ladder network and a one-section π network [4] for various values of R_T and C_T.

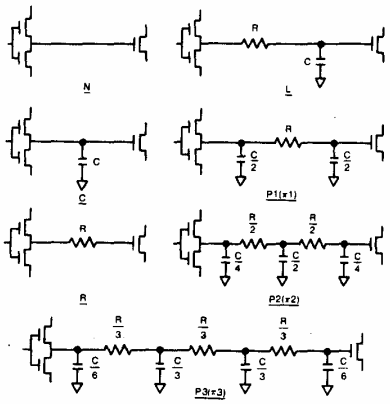

Figure 3: Lumped Circuit Models Used to Ap mate Distributed RC Interconnect Impedances

Table 3 assumes that an L network is chose a one-section π network when the relative transition error is less than 10%. Wh relative error is between 10% and 35%, section π network is chosen while a two-s π network is chosen for larger errors. Tl favorable compromise position between c accuracy and computational efficiency is tained.

C_T \ R_T	0	0.1	0.2	0.3	0.75	1.5	2	5	20	100
0.1	π3	π3	π3	π2	π1	π1	L	C	C	
0.2	π3	π2	π2	π1	π1	π1	L	C	C	
0.5	π2	π2	π1	π1	L	L	L	C	C	
1	π1	π1	π1	π1	L	L	L	C	C	
2	π1	π1	π1	L	L	L	L	C	C	
3	π1	L	L	L	L	L	L	C	C	
5	L	L	L	L	L	L	L	C	C	
20	R	R	R	R	R	R	R	C	C	
100	R	R	R	R	R	R	R	C	N	

Table 3: Lumped Interconnect Circuit Models I up Table Approximating Distributed RC Intercor Impedance as a Function of R_T and C_T

The choice of error breakpoint is both techn and design style dependent and can be varie different design constraints. The relative describes the percentage improvement in acc that one can achieve when using a more acc interconnect impedance model. A π netwo used instead of a T network since it util fewer nodes and is therefore more computation efficient since the computational efficienc SPICE is directly dependent upon the size of nodal matrix. For values of R_T and C_T gr er than 5, relative errors between L, R, C, a networks less than 10% dictate the selection simple R, C, or N network model. For large ues of R_T, the interconnect resistance i negligible consequence and the interconnect m can be represented as a simple capacitor.

large values of C_T, the interconnect model can be represented as a simple resistor. For large values of both R_T and C_T, no RC interconnect impedance model is necessary and this is symbolically represented as an N network model. Thus, the user defined factor combined with the two technology dependent look-up tables, Tables 2 and 3, define an appropriate RC network for modeling a wire's distributed interconnect impedance which accurately represents the distributed RC load for specific R_T and C_T ratios.

III. Conclusion

This paper describes an algorithm for 1) determining a device's output impedance from a technology dependent gain relationship as a function of its circuit environment and 2) choosing an optimal RC network which accurately models a wire's interconnect impedance based on technology specific look-up tables. Each node's device input capacitance and output resistance is compared to its resistive and capacitive interconnect impedances respectively, in terms of the ratios C_T and R_T. Together, they define both a sufficiently accurate and CPU efficient model of a node's interconnect impedance. The technology specific information described within this paper has been baselined around our 1.25 μm CMOS/SOS VHSIC nology.

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