SOS/CMOS Technology for Space Applications

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1) Introduction

Silicon-on-Sapphire (SOS) CMOS technology is known to be the most mature of the dielectric isolated technologies and to have several important semiconductor traits; high speed, low power, density (due to its immunity to latch-up), and of great significance to space applications, high tolerance to radiation. These characteristics are important for a large variety of systems, many of which are key Hughes, DoD, and DoE products and applications. Therefore, Hughes, in an effort to satisfy these business requirements, has been developing a family of CMOS/SOS technologies. The focus of this paper is to report on the recent results, current status, and future plans for these Hughes Aircraft SOS/CMOS technologies.

In the following section, the baseline 1.25 μm CMOS/SOS technology will be described in terms of its performance characteristics, space applications, and business development. In section 3, more aggressive extensions of this standard technology to submicrometer and analog technologies and their applications will be discussed. Finally, some conclusions will be provided in section 4.

2) Baseline 1.25 μm SOS III Digital Process

The 1.25 μm polycide single level metal (SLM) CMOS/SOS technology (described internally as SOS III) was originally developed and improved under VHSIC Φ1 and VHSIC Yield Enhancement contracts. It was further developed by the United States Army Strategic Defense Command (USASDC) to demonstrate performance at the much higher radiation levels required by SDI. This environment requires circuit performance under total dose, transient, survivability, neutron, and single event upset, much of which is necessary when operating in space environments. SOS was chosen since it is one of the only available technologies expected to reach the highest radiation goals established by the SDIO community. Classified radiation results from this program were presented at GOMAC in 1987 and an unclassified summary is described in [1].

As a result of these government programs and considerable internal investment by Hughes, a cost effective, high performance, low power, and radiation tolerant technology has been developed. This process is an all ion implanted, all dry etched polycide gate process where the polycide is formed using polysilicon and tantalum silicide. The technology is formed by the etching of completely isolated silicon islands on a 0.5 μm silicon-on-sapphire epitaxial layer. This SOS III technology has recently been extended to a polysilicon gate double level metal (DLM) process and is termed internally as SOS III-D.

SOS III has shown itself to be of high reliability and is fully space qualified. Accelerated burn-in of SOS III parts has verified that reliability is well above levels required for space applications [< 10 FITS (failures per 10^9 device hours)]. SOS III-D data is currently being produced and is expected to mirror or exceed the very low failure rate exhibited by SOS III.

The standard 1.25 μm SOS III technology has been used to develop many different circuit types for a variety of space applications. Recent examples of SOS III delivered production space programs is the recently completed seven chipset for HS601, a general purpose commercial satellite product, and a four chipset, currently in production for UHF (a Navy communications satellite system). SOS III has also been used to develop different product types such as a programmable IIR digital filter [2] (see Figure 1), an analog multiplexor, and a variety of other common functional part types.

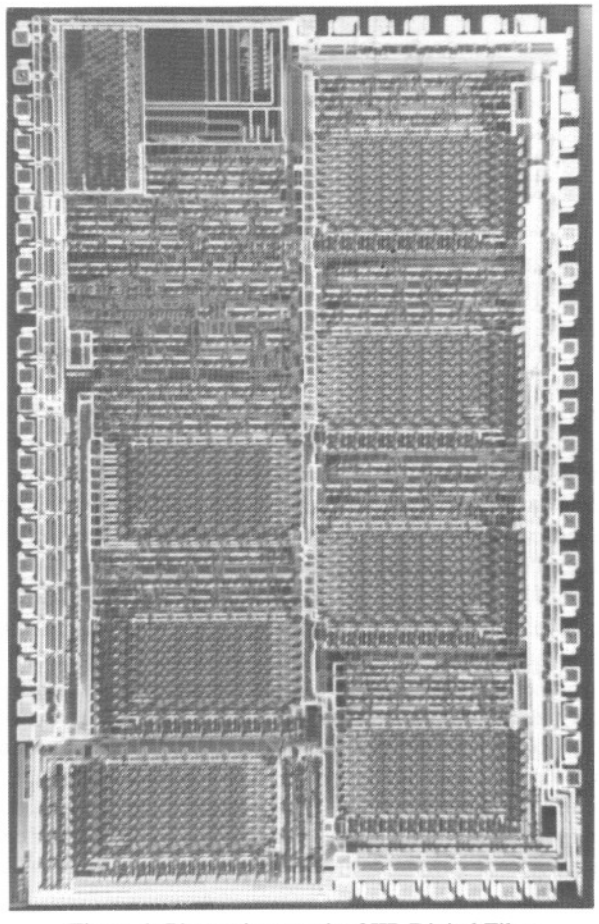

Figure 1: Photomicrograph of IIR Digital Filter

Aggressive performance (in terms of speed and power dissipation) is a common goal for many government programs. The standard SLM SOS III technology was used to develop a high speed Add & Multiply circuit [3] in which clock rates of (a tester limited) 150 MHz. at 5 volts were reached while exhibiting a power dissipation characteristic of 0.58 μwatts/gate/MHz. at 3.3 volts (where one gate is composed of four CMOS transistors). Low power dissipation is an important peformance trait of this technology. SOS III circuits have been experimentally shown to operate at power supply voltages as low as 2.7 volts. Normalized power dissipation in units of μwatts/gate/MHz. as a function of supply voltage for the baseline 1.25 μm CMOS/SOS technology is shown in Figure 2. This feature of the SOS technology makes such circuits ideal for battery operated systems.

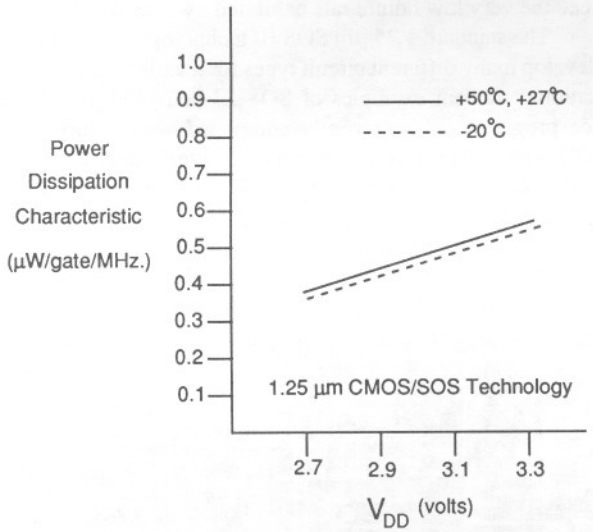

Figure 2: Experimentally Derived Power Dissipation Characteristic versus Supply Voltage for SOS III

In order to broaden the use of this capability, two approaches have been taken. The first is the development of a general IC design system in which the entire spectrum of the design process, from register transfer level description to pattern generation is automated, supporting a variety of design methodologies such as standard cell, cell generation, structured custom, and full custom. Some of the details of the design system, its flow and methologies, are described in [4,5].

The second approach for broadening the use of SOS III is the development of a dual alternate source relationship with Marconi Electronic Devices Ltd. in the United Kingdom. A generic set of 1.25 μm design rules has been developed among the recognized SOS foundries [i.e., Hughes, Marconi, Harris (formerly RCA), and Rockwell] in order to provide multi-vendor capability for high performance, radiation hard CMOS/SOS circuits. The generic 1.25 μm design rule set have already been incorporated into a double level metal cell library for standard cell and structured custom designs of digital radiation hard VLSI circuits.

Specifically, Hughes and Marconi have entered into an alternate source agreement and Hughes has processed, as a test case of the generic 1.25 μm design rules, Marconi designed 16K SRAMs, exhibiting excellent yield, performance, and radiation characteristics. For example, the 16K SRAM design meets manufacturers specifications after a total dose of at least 1 Megarad (Si). Discussions are underway for Hughes to process the Marconi designed 64K SRAM and their 1750A computer chipset.

Finally, efforts are underway to provide analog and combined analog/digital capability in SOS III. An assortment of analog components, such as operational amplifiers, comparators, oscillators, and voltage references, have been made and experimentally verified, showing promising performance results. The comparators exhibit 5 mV resolution while operating at speeds greater than 20 MHz. (settling within 40 ns.) while the op amps exhibit open loop gains of greater than 100 db and bandwidths up to 8 MHz.

3) Extension of SOS to Submicron and Analog

In order to satisfy current and developing space applications requiring higher digital and analog performance levels, significant focus has been placed on developing two new aggressive CMOS/SOS technologies; an 0.8 μm lithographically defined polysilicon gate SLM technology (termed SOS IV) and a deep submicrometer (DSM) E-beam defined salicide gate SLM technology (termed SOS V). The range of effective channel lengths in the SOS V technology is between 0.25 μm and 0.5 μm and is clearly targeted for extremely aggressive performance goals.

SOS IV is being used to develop near term marketable product types which extend the performance of SOS III while maintaining its high yields. Recently, SOS V was used to demonstrate a high speed 4 bit A/D converter [6]. Focused-ion-beam (FIB) threshold implants were used to set the threshold voltages of individual MOSFET's in the comparators, greatly simplifying their design. A/D conversion rates exceeding 2 Gigasamples per second (GSPS) and dissipating 100 milliwatts (excluding output buffers) were achieved. Some circuits, produced with 0.25 μm channel lengths, operated at a tester limited 2.6 GSPS. A photomicrograph of the circuit is shown in Figure 3. These devices have been functionally demostrated at total dose radiation levels up to 3 Megarads (Si) with degradations of 2 to 3 db in signal to noise ratio at a sampling frequency of 800 MHz. Detailed characterization is in progress. In addition to the significant capital, process development, and circuit design costs required to develop a capability of this nature, significant investment has been made in the supporting test technology required to evaluate these high speed low noise circuits.

In an effort to exploit the speed and complexity offered by this 0.25 to 0.5 μm technology, Hughes, working under contract with NOSC, is using the 4 bit A/D as a building block for a Σ-Δ A/D converter [6,7] intending on providing 16 bit accuracy at speeds of 100 MSPS. Key building blocks have been designed and results are expected by late 1990.

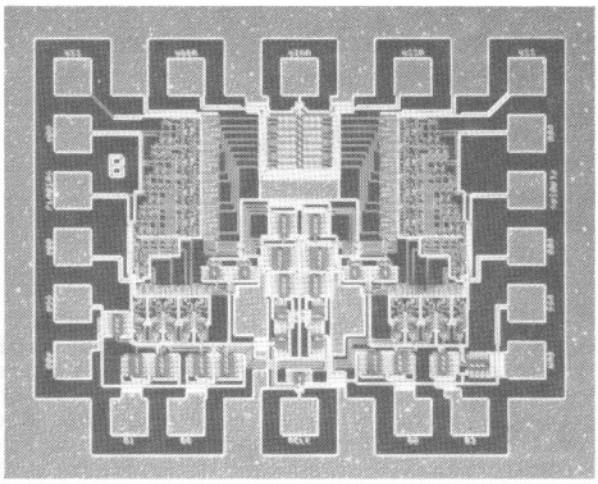

Figure 3: Photomicrograph of 4 Bit A/D Converter

At deep submicrometer dimensions, hot electron effects become a primary mechanism for degrading device reliability required by space applications. Thus, a lightly doped drain requiring a spacer technology and salicide gate forms a key element in the SOS V process. An alternate approach which is being investigated is to operate the transistors in a fully depleted mode. This provides more uniform electric fields, thereby minimizing hot electron effects. SOS films down to 0.1 μm thickness are being developed.

4) Conclusions

Hughes Aircraft has been supplying advanced space applications with chip types over many years and programs. Performance levels, such as clock rates greater than 150 MHz., and power dissipation levels less than 0.6 μwatts/gate/MHz., radiation levels much greater than 1 megarad, and excellent yields have been achieved with the 1.25 μm SOS III digital technology. Multi-vendor generic design rules have been developed among the various SOS foundries for improved supply of SOS parts and a dual alternate source agreement has been developed between Hughes and Marconi. Finally, the Hughes CMOS/SOS technology is being supported for future space systems, evidenced by the significant investment by both Hughes and the U. S. government in further developing CMOS/SOS technologies at the circuit, device, process, and test levels for both the 0.8 μm and sub 0.5 μm SOS technologies.

Acknowledgments

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References

[1] G. A. Antcliffe, K. G. Aubuchon, H. M. Gerard, G. H. Hershman, D. A. Kosty, W. Kephart, and R. Tso, "Radiation Hard Digital and Analog VLSI Circuits for SDI Applications," *Proceedings of Government Microcircuits Applications Conference*, pp. 411-414, October 1987.

[2] Hughes Technology Center - Part #4125 data sheet for Programmable IIR Digital Filter Chip.

[3] W. L. Marking, S. R. Powell, R. R. Siviy, W. S. Kephart, and E. G. Friedman, "A 150-MHz 1.25 μm CMOS/SOS DSP Integrated Circuit," *Proceedings of IEEE SOS/SOI Technology Conference*, pp. 105-106, October 1989.

[4] E. G. Friedman, S. Powell, and G. Yacoub, "A CMOS/SOS VLSI Design System," *Journal of Semi-Custom ICs*, Vol. 2, No. 4, pp. 5-11, June 1985.

[5] S. Powell and B. Barouch, "MAP:A Parameterizable Module Generator Development System Oriented to IC Design," *Proceedings of the Custom Integrated Circuits Conference*, pp. 5-8, May 1987.

[6] R. H. Walden, A. E. Schmitz, A. R. Kramer, L. E. Larson, and J. Pasiecznik, "A Deep-Submicrometer Analog-to-Digital Converter Using Focused-Ion-Beam Implants," *IEEE Journal of Solid-State Circuits*, Vol. SC-25, No. 2, pp. 562-571, April 1990.

[7] R. H. Walden, T. Cataltepe, and G. C. Temes, "Architectures for High-Order Multibit ΣΔ Modulators," *Proceedings of International Symposium on Circuits and Systems*, pp. 895-898, May 1990.