A COMPARATIVE STUDY OF THE BEHAVIOR OF NMOS AND CMOS DIGITAL CIRCUITS UNDER SUBSTRATE NOISE

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Abstract— **A comparative study of the behavior of NMOS and CMOS digital circuits in terms of the ability to tolerate substrate noise is presented in this paper. Theoretical and simulation results are confirmed by experimental data gathered from the analysis of NMOS and CMOS test chips. It is shown that while the noise sensitivity of NMOS digital circuits is influenced by a variety of factors, the primary phenomenon responsible for the noise integrity of the CMOS digital circuits is latch-up.**

I. Introduction

Substrate noise is a deleterious phenomenon particularly important in systems-on-a-chip (SOCs) mixed-signal integrated circuits which are composed of a variety of possible on-chip circuit blocks such as analog, digital, high voltage, high power, or RF. The noise immunity of digital circuits in a mixed-signal environment has been investigated in [1–4]. In this paper, a comparative study of the noise immunity of NMOS and CMOS digital circuits in a mixed-signal smart-power environment is presented in Section II. Some conclusions are drawn in Section III.

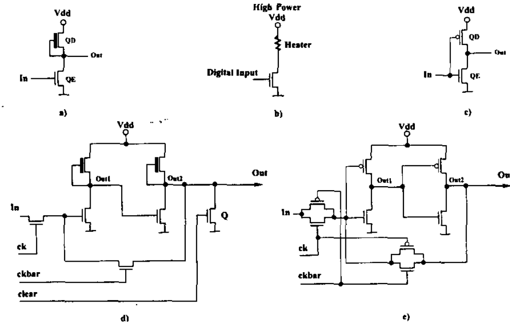

Fig. 1. NMOS and CMOS test circuits: a) an NMOS inverter, b) NMOS and CMOS power driver, c) a CMOS inverter, d) an NMOS static slave latch, and e) a CMOS static latch.

II. Substrate noise in NMOS and CMOS digital circuits

A mixed-signal smart-power application is used [1, 5] to evaluate and compare the influence of substrate noise on NMOS and CMOS digital circuits. The NMOS and CMOS test circuits are shown in Fig. 1. Note that the power driver is similar in both technologies. The circuit configuration of the NMOS and CMOS static latches are also similar to eliminate certain circuit variables from the comparative analysis.

NMOS and CMOS test circuits have been designed and fabricated in high voltage non-epitaxial NMOS and epitaxial N-well CMOS processes, respectively. Chip microphotographs of representative NMOS and CMOS test circuits are shown in Figs. 2 and 3, respectively. Both circuits have a similar floorplan to ensure an accurate comparison, as shown in Fig. 4. Note that in the NMOS and CMOS test circuits, the 64 (NMOS) and 48 (CMOS) individually selectable power drivers are grouped into eight and six groups, respectively. Each group of eight drivers, affects the 32 respectively 20 registers placed along the upper side of the chip. Test chips with different floorplans have also been designed, fabricated, and tested [1, 2, 4], such as the CMOS test circuit shown in Fig. 5 which is used to probe the individual substrate noise waveforms.

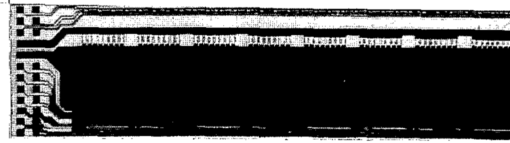

Fig. 2. Microphotograph of NMOS test circuit

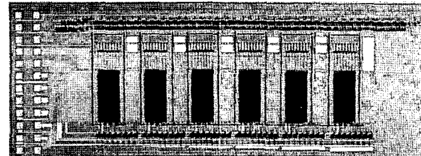

Fig. 3. Microphotograph of CMOS test circuit

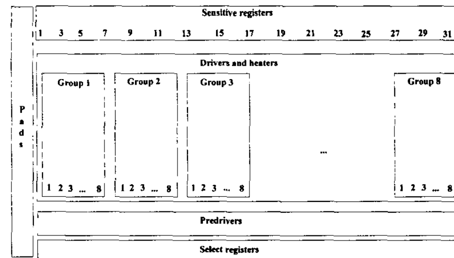

Fig. 4. Floorplan of both of the NMOS and CMOS test circuits

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The magnitude of the substrate noise together with related nonuniformities within the substrate are the two primary factors that influence the noise behavior of digital circuits [1, 2]. The noise behavior of NMOS digital circuits can be greatly improved by considering a large variety of technological, circuit, and physical design issues [1–4, 6–12]. These issues include the technology, the substrate doping and thickness, the distance between the noise source and the noise receptor, the placement of substrate contacts, guard rings and wells, a backplane substrate contact, circuit switching speed and transition times, the routing of the power lines, inductive effects, circuit placement and orientation, power driver supply voltage, the switched current of the power driver, the duration of the noise pulse, the number of drivers that are active, clock and signal conditioning of the digital circuits, the chip temperature, the transistor sizes, and the common or separated grounds between the analog and digital blocks. The minimum necessary noise level to latch a parasitic transition for a nonuniform substrate noise distribution is ≈ 1.7 volts for a 5 volt NMOS digital circuit [2, 5].

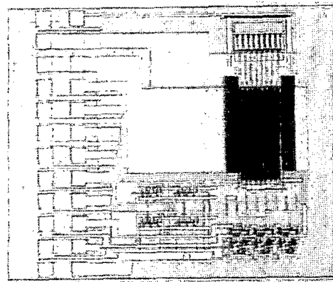

Fig. 5. Microphotograph of a CMOS test circuit used to probe the substrate noise waveforms

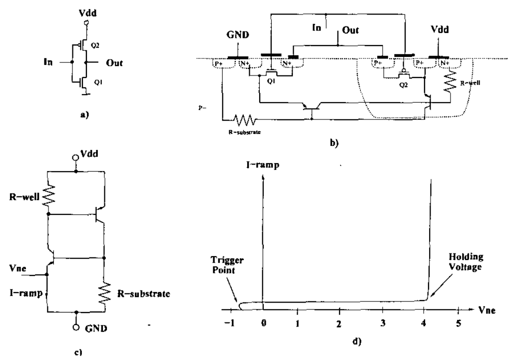

Fig. 6. The latch-up phenomenon: a) a CMOS inverter, b) cross-section of a CMOS inverter, c) the SCR parasitic circuit schematic, d) $I - V$ characteristics of the parasitic circuit.

A similar analysis as performed for the NMOS test circuits [1, 2, 4] is applied to the CMOS test circuits with the addition of the latch-up phenomenon [13–16]. The primary characteristics of the latch-up phenomenon such as the SCR parasitic structure and the $I - V$ characteristic of the parasitic circuit are shown in Fig. 6.

The NMOS and CMOS test circuits have been designed to evaluate a set of similar variables [1, 2, 4]. In addition, two similar subsets of CMOS test circuits have been fabricated to evaluate the effects of the tub isolation of the power drivers on the generation, transmission, and reception of the substrate noise.

The experimental data characterizing the CMOS circuits exhibit a different behavior as compared to the NMOS circuits. The test circuits featuring non-isolated power drivers are shown to be prone to substrate noise induced latch-up and metastability. Other secondary dependencies such as turn on/off characteristics, power supply, pulse width, number of active drivers, process related issues, substrate contacts, and stored data are also noted for all the test circuits, featuring either isolated or non-isolated power drivers. These dependencies are discussed next as part of several major categories.

a) Latch-up

The latch-up behavior of the circuits with non-isolated power drivers as a function of supply voltage of the power drivers when all six groups of power drivers are active for a $2\,\mu s$ pulse is listed in Table I. When latch-up occurs, irreversible damage to the circuit is prevented by limiting the current generated by the logic power supply. As with the NMOS circuits, the pulse width and the number of active groups that are on affect the noise behavior. Therefore, latch-up is shown to not occur when only one group is active for a $2\,\mu s$ pulse at 38 volts, or when eight groups are active at 38 volts where the turn-on/turn-off time of each of the groups is distributed in time over a $2\,\mu s$ period.

TABLE I

LATCH-UP BEHAVIOR OF CMOS TEST CIRCUITS WITH NON-ISOLATED POWER DRIVERS AS A FUNCTION OF THE POWER SUPPLY VOLTAGE

Power supply (V)	38	34	30	26	22	20	18
Latch-up	Yes	Yes	Yes	Yes	Yes	Yes	No

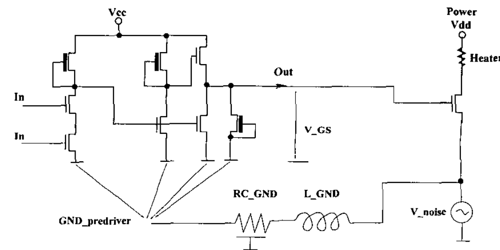

Fig. 7. The positive feedback loop responsible for the output oscillation

b) Metastability

Metastability is observed when the duration and/or amplitude of the substrate noise pulse is not sufficient to maintain but is sufficient to trigger the latch-up process [13, 17–21]. The metastable state (the output oscillation) is maintained by a positive feedback loop among the predriver, power driver, and the substrate and/or ground lines [4], as shown in Fig. 7 for the NMOS circuits. This positive feedback loop is responsible for developing an oscillatory substrate noise waveform [4] as shown in Fig. 8.

c) Turn on/off characteristics

Test data also show that the noise generated as the power drivers turn-off is more likely to induce noise

glitching than the noise generated as the power drivers turn-on. This behavior can be explained by noting that in order for the two events to be similar from a noise point of view, the turn-on edge must be sufficiently sharp, and the power supply of the predrivers must be significant in order to produce a large voltage swing on the gate of the power drivers. Test data show that it is sufficient to skew the turn-off time of the active power drivers to reduce the influence of the substrate noise.

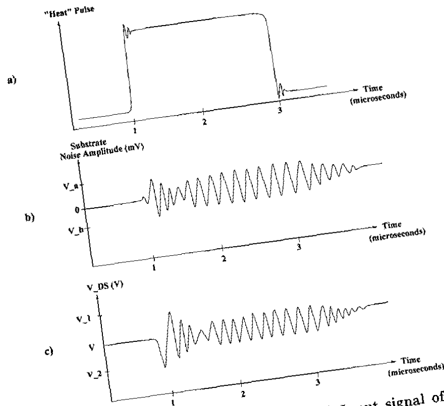

Fig. 8. Characteristic noise waveforms a) Input signal of the power transistor b) Substrate bias oscillation c) V_{DS} across the power transistor

d) Process related issues

Experimental CMOS data show that, in general, for the isolated power drivers, the aforementioned test conditions do not affect the registers. However, a difference is observed depending on the HV-well (high-voltage well) and V_T doping concentrations. For increased doping levels, the registers in the vicinity of the active power drivers can be randomly affected from one pulse to another pulse. This phenomenon can be explained by noting the differences between the noise transmission process in a non-epitaxial technology as compared to an epitaxial technology [2, 3, 6, 12], primarily due to the low resistivity bulk in an epi technology [3]. Three-dimensional noise distributions as described in [3] are shown in Figs. 9 and 10 for a non-epi and epi technology, respectively. For high dopings in these regions, local non-epitaxial areas are created by making the doping level within the epitaxial layer closer to the doping level within the bulk. Another aspect that contributes to this behavior is the V_T decrease of the transistors as the V_T doping levels increase. Test data show that the placement of the substrate contacts with respect to the sensitive registers and power drivers [3] can affect the integrity of the stored data.

e) Data dependency

In the same context, the registers are observed to be affected primarily when the stored data is at logic high. This behavior can be explained by considering two aspects: 1) the transmission path of a parasitic *"high"* logic level (see Fig. 1) for $D_{in} = 1$ (from one inverter directly to another inverter) and for $D_{in} = 0$ (through a transmission gate), and 2) the noise, generated as the power drivers turn-off, which has been shown to be more likely to affect the registers, primarily affects the *"high"* logic data signal stored in a register.

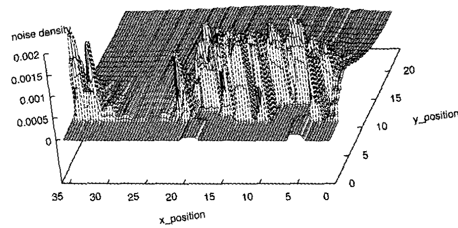

Fig. 9. A substrate noise distribution for a non-epi technology

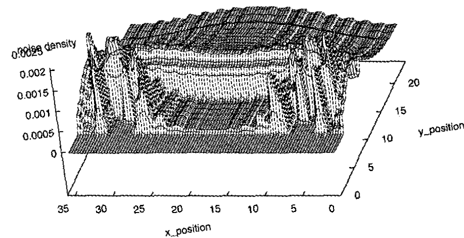

Fig. 10. A substrate noise distribution for an epi technology

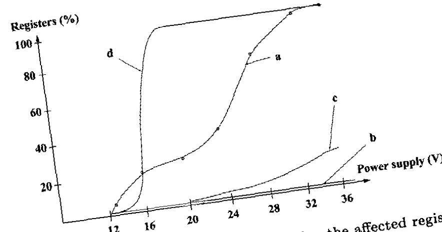

Fig. 11. Experimental data characterizing the affected registers as a function of the supply voltage of the power drivers: a) NMOS circuits, b) CMOS isolated power drivers, c) CMOS isolated power drivers (high dopings), d) CMOS non-isolated power drivers (latch-up and metastability)

Latch-up is shown to be the most important way in which the integrity of the stored data in the registers is influenced. Therefore, the dependence of the affected registers as a function of the power supply voltage of the power drivers for isolated and non-isolated power drivers is shown in Fig. 11. For comparison, a similar dependency for NMOS circuits is also shown, where the affected registers are averaged over the four clocking regimes as described in [1]. The four curves are normalized with respect to the number of affected registers. Note that for curve d), once latch-up is induced, all of the registers are considered to be affected. Curve c) includes other dependencies as previously explained.

All of these dependencies have technological, circuit, and physical design components. While the technological and physical design aspects are fairly well understood, the circuit component needs further investigation. Therefore, to better characterize the circuit aspects of this behavior, simulations have been performed using Cadence Spectre under ideal conditions where no parasitic latch-up structure is considered, emulating similar conditions as for the NMOS circuits [2, 4]. The simulation set-up is shown in Fig 12. Note that similar to an NMOS latch [2], independent noise sources to simulate any desired noise configuration have been provided for each of the four transistors. As for an NMOS latch, an open loop latch is analyzed. Since a transmission gate is used in the feedback loop, the output voltage is transmitted over the feedback connection without any voltage drop. Each of the four noise sources may have any value between +5 and -5 volts. The simulation results demonstrate that a parasitic transition is latched for both high and low logic inputs and for substrate noise amplitudes greater than approximately +3 and -3 volts, respectively. If such a large substrate noise level is present, it is highly likely that latch-up will occur before a parasitic transition is induced.

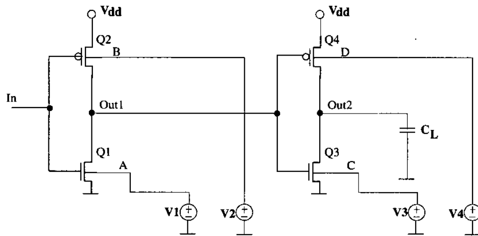

Fig. 12. The simulation set-up

These results confirm the experimental data. The +/- 3 volts noise threshold has not been obtained for the isolated power drivers; therefore, no parasitic transition has been observed independent of the test conditions. For the non-isolated power drivers, a noise level smaller than the +/- 3 volts has been shown to induce latch-up and metastability. Again, no parasitic transition has been observed, since, as expected, the substrate noise level necessary to induce latch-up is smaller than the +/- 3 volt threshold, the voltage level necessary to induce a parasitic transition.

III. Conclusions

Important differences in the behavior of NMOS and CMOS digital circuits with respect to tolerating substrate noise have been experimentally determined. The differences in the experimental data are explained using extensive simulation and analysis. The substrate noise threshold voltage required to induce a parasitic transition has been determined. It is experimentally shown that for CMOS circuits the substrate noise triggers latch-up and metastability before inducing a parasitic transition. For a latch-up aware technology with proper circuit design and physical layout, it is demonstrated that the behavior of CMOS digital circuits is much more tolerant to substrate noise than the counterpart NMOS circuits.

References

[1] R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Noise Immunity of Digital Circuits in Mixed-Signal Smart Power Systems," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 314–317, February 1999.

[2] R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "The Behavior of Digital Circuits under Substrate Noise in a Mixed-Signal Smart-Power Environment," *Proceedings of the IEEE International Symposium on Power Semiconductor Devices and ICs*, pp. 253–256, May 1999.

[3] R. M. Secareanu, S. Warner, S. Seabridge, C. Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Substrate Noise Distribution and Placement of Substrate Contacts to Alleviate Substrate Noise in Epi and Non-Epi Technologies," *Proceedings of the IEEE Annual EDS/CAS Activities in Western New York Conference*, pp. 15–16, November 1999.

[4] R. M. Secareanu, S. Warner, S. Seabridge, C. Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Physical Design to Improve the Noise Immunity of Digital Circuits in a Mixed-Signal Smart-Power System," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 4.277–4.280, May 2000.

[5] E. Peeters and S. Verdonckt-Vandebroek, "Thermal Ink Jet Technology," *IEEE Circuits and Devices Magazine*, Vol. 13, No. 4, pp. 19–23, July 1997.

[6] D. K. Su and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 4, pp. 420–430, April 1993.

[7] X. Aragones and A. Rubio, "Analysis and Modelling of Parasitic Substrate Coupling in CMOS Circuits," *IEE Proceedings–Circuits, Devices and Systems*, Vol. 142, No. 5, pp. 307–312, October 1995.

[8] S. Masui, "Simulation of Substrate Coupling in Mixed-Signal MOS Circuits," *Proceedings of the IEEE International Symposium on VLSI Circuits*, pp. 42–43, June 1992.

[9] T. Blalack and B. A. Wooley, "Experimental Results and Modeling of Noise Coupling in a Lightly Doped Substrate," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 623–626, December 1996.

[10] K. M. Fukuda and M. Hotta, "Voltage-Comparator-Based Measurement of Equivalently Sampled Substrate Noise Waveforms in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 5, pp. 726–731, May 1996.

[11] B. R. Stanisic, N. K. Verghese, and D. J. Allstot, "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power Distribution Synthesis," *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 3, pp. 226–238, March 1994.

[12] X. Aragones and A. Rubio, "Experimental Comparison of Substrate Noise Coupling Using Different Wafer Types," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 10, pp. 1405–1409, Oct. 1999.

[13] B. L. Gregory and B. D. Shafer, "Latch-up in CMOS Integrated Circuits," *IEEE Transactions on Nuclear Science*, Vol. NS-20, No. 6, pp. 293–299, December 1973.

[14] R. R. Troutman, "Latchup in CMOS Technologies," *IEEE Circuits and Devices Magazine*, Vol. 3, No. 3, pp. 15–21, May 1987.

[15] R. R. Troutman, "Recent Developments in CMOS Latchup," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 296–299, December 1984.

[16] R. R. Troutman and H. P. Zappe, "Power-up Triggering Conditions for Latch-up in Bulk CMOS," *Proceedings of the IEEE Symposium on VLSI Technology*, pp. 52–53, September 1982.

[17] M. R. Pinto and R. W. Dutton, "Accurate Trigger Condition Analysis for CMOS Latch-up," *IEEE Electron Device Letters*, Vol. 6, No. 2, pp. 100–102, February 1985.

[18] S. Odanata, M. Wakabayashi, and T. Ohzone, "The Dynamics of Latch-up Turn-on Behaviour in Scaled CMOS," *IEEE Transactions on Electron Devices*, Vol. 32, No. 7, pp. 1334–1340, July 1985.

[19] R. E. Bank, W. M. Coughran, and K. R. Smith, "Transient Simulation of Silicon Devices and Circuits," *IEEE Transactions on Electron Devices*, Vol. 32, No. 10, pp. 1992–2007, October 1985.

[20] W. M. Coughran, M. R. Pinto, and R. K. Smith, "Computation of Steady-State CMOS Latch-up Characteristics," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 7, No. 2, pp. 307–323, February 1988.

[21] A. Ochoa, W. Dawes, and D. B. Estreich, "Latch-up Control in CMOS Integrated Circuits," *IEEE Transactions on Nuclear Science*, Vol. 26, No. 6, pp. 5065–5068, December 1979.