A 250 MHZ DELTA-SIGMA MODULATOR FOR LOW COST ULTRASOUND/SONAR BEAMFORMING APPLICATIONS

Boaz Shem-Tov[1], Mücahit Kozak[2], and Eby G. Friedman[2]

[1]Department of Electrical and Computer Engineering
ORT-Braude College
Karmiel, Israel 21982-0078

[2]Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627-0231

ABSTRACT

Single-bit Delta-Sigma (ΔΣ) modulation reduces the complexity of receive beamformers in ultrasound and sonar imaging applications. These applications, however, require a sampling rate in excess of 220 MHz due to the high bandwidth of the echo signals. In this paper, the design and implementation of a 250 MHz second-order single-bit ΔΣ modulator suitable for ultrasound/sonar applications is presented. The circuit is realized in a 0.18 μm P-well CMOS technology and dissipates 20 mW average power when clocked at 250 MHz. The area of the circuit is 0.24 mm^2. Post-layout simulations show that the modulator achieves 48 dB maximum SNR and 50 dB dynamic range for a 5 MHz input signal bandwidth.

1. INTRODUCTION

Ultrasound/Sonar imaging devices use beamforming techniques to reconstruct an image of the interrogated medium. A simplified block diagram of a medical ultrasound imaging system is depicted in Figure 1, which includes a transducer array, transmit and receive beamforming blocks, a signal and image processor, and a display device. The primary task of the system is to form beams on both transmit and receive at a significantly fast rate to enable real-time imaging.

In real-time phased array systems, due to limited sound velocity, transmit beamformers employ a fixed focused beam at each scan angle, whereas receive beamformers dynamically focus the array to the successive focal points to obtain nearly uniform resolution throughout the field of interest [1]. Dynamic receive focusing is illustrated in Figure 2 where the pulse echo signals are combined together with a spherical timing relationship to compensate different round-trip signal times at each channel array.

Realizing a dynamic receive focusing requires multi-bit (typically, 8-bit) A/D converters at each array channel, dramatically increasing the cost, area, and power consumption. The use of single-bit ΔΣ modulators, rather than multi-bit A/D converters, can greatly reduce the electronics inside a beamformer [1], [2]. In recent years, receive beamforming using single-bit ΔΣ modulation has received significant attention. In [2]-[5], system level architectures are proposed, analyzed, and simulated for single-bit ΔΣ beamformers. From a practical point of view, however, the application of ΔΣ modulators in ultrasound and sonar beamformers is challenging due to a high sampling rate (in excess of 220 MHz). In this paper, the design and implementation of a second-order single-bit ΔΣ modulator that can be clocked at 250 MHz is addressed.

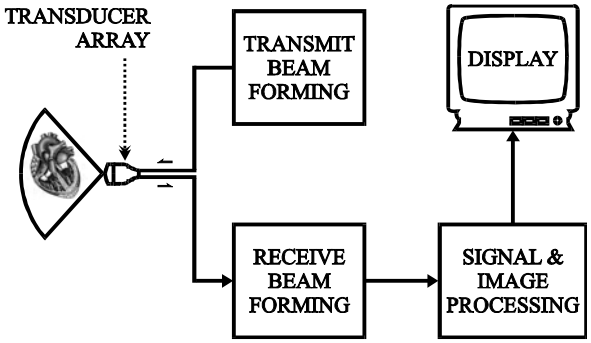

Figure 1. Block diagram of a medical ultrasound imager

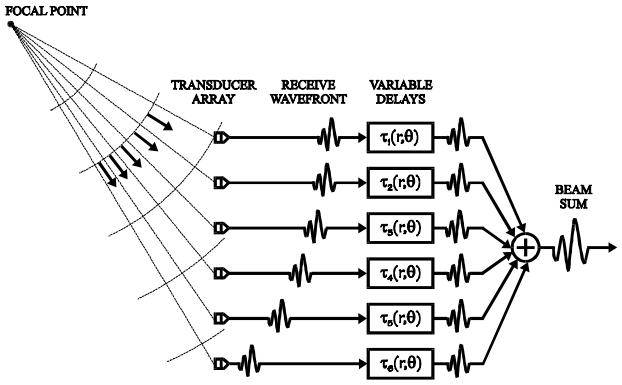

Figure 2. Dynamic receive focusing

This paper is organized as follows. In Section 2, the system architecture for ΔΣ beamformers is presented. The design and implementation of a second-order ΔΣ modulator is explained in Section 3. Post-layout simulation results are presented in Section 4, followed by some conclusions in Section 5.

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2. SYSTEM ARCHITECTURE

A block diagram for a phased array ΔΣ beamformer is illustrated in Figure 3, where Nyquist-rate multi-bit A/D converters are replaced with single-bit ΔΣ modulators at each array channel [2]. The single-bit output from each ΔΣ modulator undergoes dynamic focusing before summing. A decimation filter is used to filter out the high frequency quantization noise caused by the ΔΣ modulators, producing a high-resolution beam sum.

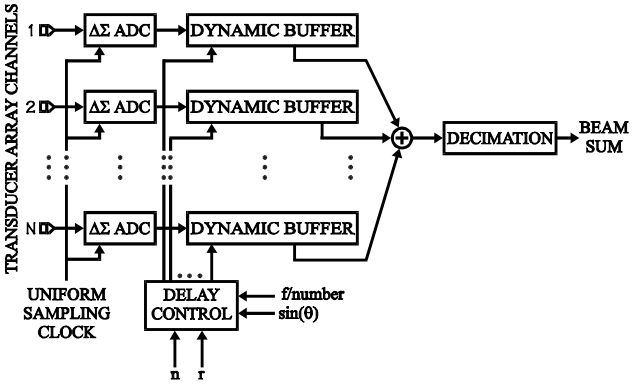
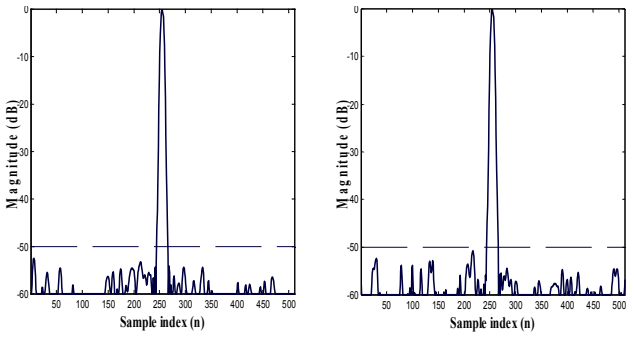


Figure 3. Block diagram of the ΔΣ beamformer



(a) **(b)**

Figure 4. Envelope of the beam sum, (a) 8-bit Nyquist-rate A/D, (b) 1-bit second-order ΔΣ modulator

A single-bit ΔΣ beamformer has numerous advantages over a conventional multi-bit beamformer: (i) the required analog hardware is greatly reduced due to the simpler implementation of a ΔΣ modulator, (ii) single-bit ΔΣ outputs reduce the word length of the dynamic focusing hardware, and (iii) the high sample rate from the ΔΣ modulators results in greater delay accuracy in dynamic focusing. Despite these advantages, previous simulation results [2]-[5] have, however, shown that a clock frequency in excess of 222 MHz is required from the ΔΣ modulators when deployed in ultrasound and sonar applications.

Simulation results for a 16-channel phased array beamformer that utilizes 8-bit A/D converters and single-bit second-order modulators are shown in Figures 4(a) and (b), respectively. In these figures, a 3.5 MHz RF Gaussian pulse with a 5 MHz low-pass bandwidth is noise added (up to -50 dB relative to its maximum amplitude). The RF pulse is then quantized using ideal 8-bit A/D converters and single-bit second-order ΔΣ modulators (see Figure 5) operating at 222 MHz, followed by dynamic focusing. As shown in Figure 4, the beam sums produced by the systems are indistinguishable.

3. DESIGN AND IMPLEMENTATION OF THE DELTA-SIGMA MODULATOR

A block diagram of the second-order ΔΣ modulator used in this study is shown in Figure 5. The modulator includes two delaying integrators with a gain of 0.5, a comparator, and two summing junctions. As compared to a conventional second-order structure, this modulator is preferred due to the reduced signal swing requirement at the output of the integrators [6]. The ΔΣ modulator is targeted to obtain 8 bits of equivalent resolution for a 5 MHz input signal bandwidth with a 250 MHz sampling frequency (*i.e.*, OSR=25).

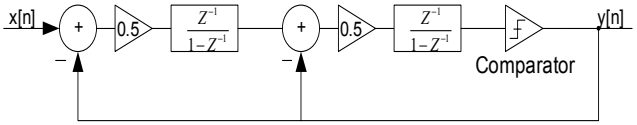


Figure 5. A second-order ΔΣ modulator

The implementation of ΔΣ modulators is achieved with either switched capacitor or continuous-time circuits. In general, continuos-time ΔΣ modulators provide good wide-band noise performance, but are sensitive to 1/f noise in the amplifiers. Additionally, continuous-time integrators are highly sensitive to clock jitter error, and require highly linear resistances that are normally not available in standard digital CMOS technologies. Due to these limitations, a switched capacitor technique is preferable. A switched capacitor implementation of the ΔΣ modulator shown in Figure 5 is illustrated in Figure 6. A fully differential topology is used to reduce the common mode noise, charge injection, and harmonic distortion.

The switched capacitor implementation uses two non-overlapping clocks ($\theta 1$ and $\theta 2$) along with the slightly delayed versions ($\theta 1d$ and $\theta 2d$). The operation of the first integrator is as follows. At phase 1, the input and feedback signals are sampled in the sampling and feedback capacitors, respectively. At phase 2, the charge in the sampling and feedback capacitors is transferred to the integrating capacitor. Since the output of the first integrator is the input to the second integrator, this clocking scheme is reversed for the second integrator. To reduce signal dependent charge injection, switches $\theta 1d$ and $\theta 2d$ open slightly earlier than $\theta 1$ and $\theta 2$ [6]. Sufficiently large sampling and integrating capacitors are used so that the maximum achievable Signal-to-Noise ratio (SNR) and dynamic range is not limited by kT/C noise. Referring to Figure 6, the sampling and integrating capacitors are 500 fF and 1 pF, respectively. The resulting noise floor at the output is therefore limited by the quantization noise introduced by the ΔΣ modulator, and not by kT/C noise.

The circuit is implemented in a 0.18 μm P-well standard digital CMOS process and operates with a 1.8 volt single power supply. Seven external signals (input signal, VDD, GND, master clock, Vref+, Vref-, and Reset) are required to operate the circuit. All of the internal bias voltages and clocks are generated on-chip.

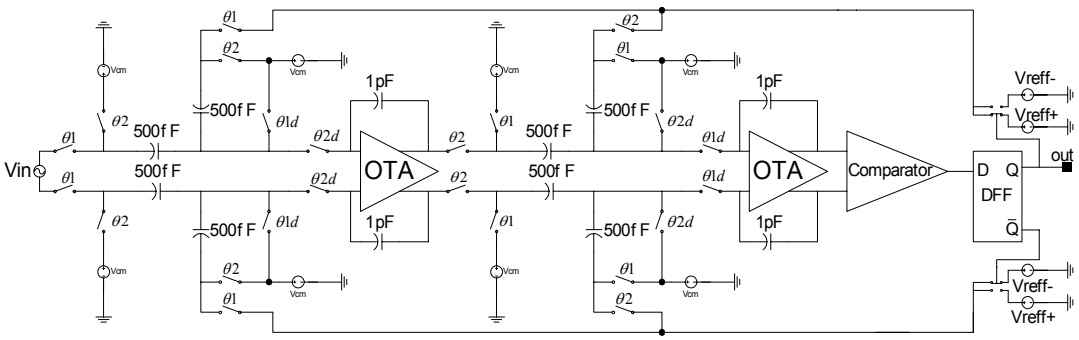


Figure 6. Switched capacitor implementation of the ΔΣ modulator

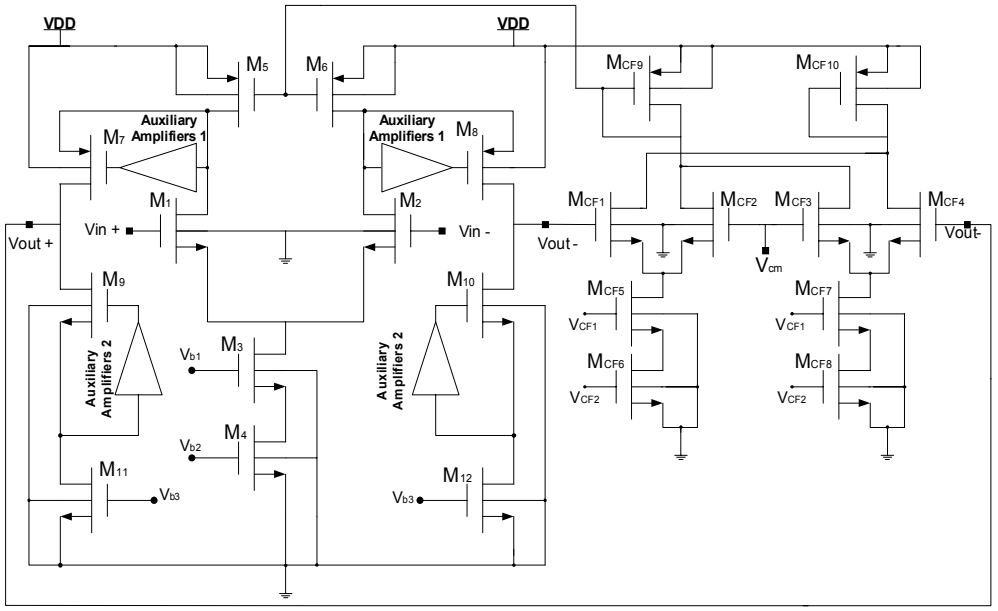


Figure 7. Circuit schematic of the OTA

The Operational Transconductance Amplifiers (OTA) used in the implementation are realized using a fully-differential folded-cascode topology with gain boosting amplifiers as shown in Figure 7. The gain boosting amplifiers are designed using a single-ended folded-cascode topology. A continuous-time common-mode feedback circuit is utilized to define the output common level (in this paper, 900 mV), due to the superior speed. Due to the fast settling requirement (less than 2 ns), the quiescent current in the OTA is chosen as 1.5 mA. The simulated open-loop DC gain of the amplifier is 90 dB.

A clocked comparator based on a regenerative latch as shown in Figure 8 is used in the ΔΣ modulator as a single-bit quantizer. The regenerative latch (cross-coupled inverters) is composed of M_{Cm3}, M_{Cm4}, M_{Cm11}, and M_{Cm12}. When the clock is high, the PMOS transistors in the regenerative latch are isolated from the NMOS transistors. The output of the comparator is therefore always low in this case. When the clock makes a transition from high to low, the regenerative action of the latch forces the output to settle to a state determined by the inputs of the comparator. The comparator is followed by inverters, which are used to recover the full signal level.

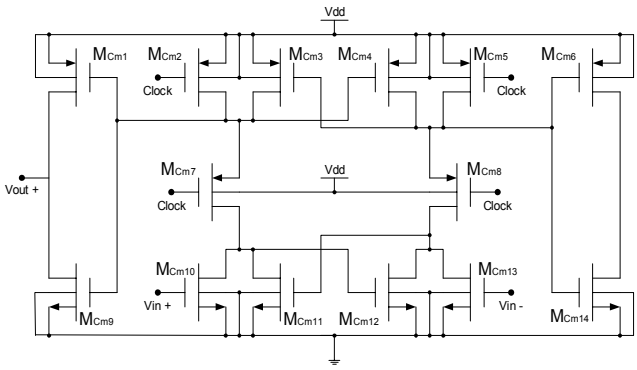


Figure 8. Circuit schematic of the comparator

The layout of the ΔΣ modulator based on a 0.18 μm P-well standard digital CMOS process with two polysilicon and three metal layers is shown in Figure 9. The circuit measures 0.22 mm^2, excluding the input/output pads. The capacitors are realized using one polysilicon layer and one metal layer. Approximately 75% of the circuit area is consumed by capacitors.

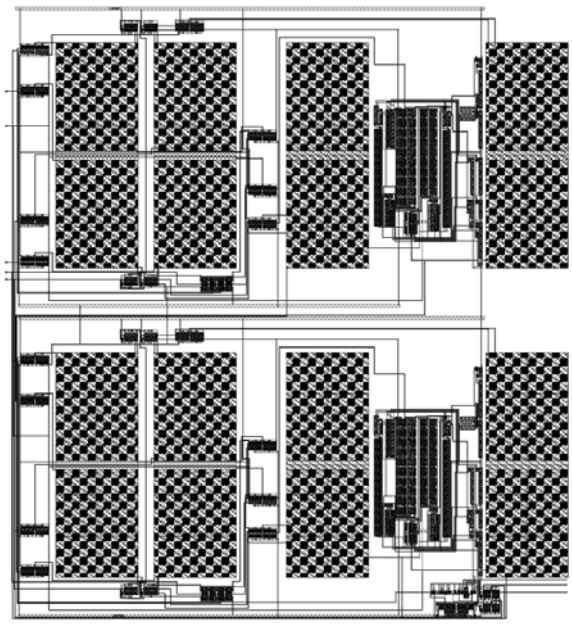


Figure 9. Layout of the ΔΣ modulator

4. POST LAYOUT SIMULATIONS

In this section, post-layout (after parasitic extraction) simulation results are presented. The power spectral density (PSD) of the output of the ΔΣ modulator for a -2 dBFS (dB Full Scale) input amplitude is depicted in Figure 10. The input is a 1 MHz sinusoidal signal, and the sampling frequency is set to 250 MHz. The simulated SNR is 47 dB for a 5 MHz input signal bandwidth (*i.e.*, OSR=25).

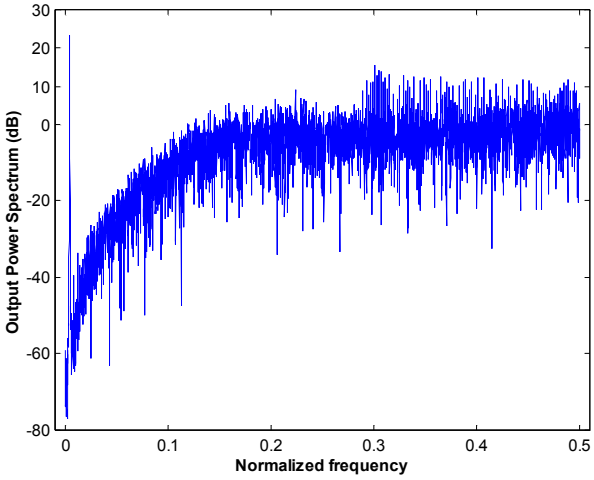


Figure 10. PSD of the output of the ΔΣ modulator

The SNR versus input amplitude obtained from several post-layout simulations is shown in Figure 11. The maximum SNR and dynamic range are 48 dB and 50 dB, respectively. These results reveal that the ΔΣ modulator attains 8 bits of equivalent resolution for a 5 MHz input signal bandwidth at an OSR=25, and hence can be used in ultrasound and sonar applications.

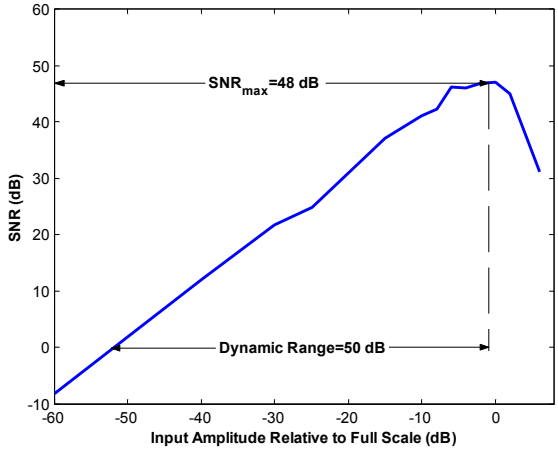


Figure 11. SNR versus input amplitude

5. CONCLUSIONS

A 250 MHz second-order single-bit ΔΣ modulator suitable for ultrasound and sonar beamforming applications is presented. The circuit is implemented in a 0.18 μm P-well standard digital CMOS process. Post-layout simulations demonstrate that the modulator achieves 48 dB maximum SNR and 50 dB dynamic range for a 5 MHz input signal bandwidth, where the sampling frequency is 250 MHz frequency (*i.e.*, OSR=25). The average power consumption and area are 20 mW (with a single power supply of 1.8 volt) and 0.24 mm^2, respectively. The circuit satisfies the specifications of ultrasound and sonar applications.

6. REFERENCES

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