BUFFER SIZING FOR DELAY UNCERTAINTY INDUCED BY PROCESS VARIATIONS

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ABSTRACT

Controlling the delay of a signal in the presence of various noise sources, process parameter variations, and environmental effects represents a fundamental problem in the design of high performance synchronous circuits. The effects of device parameter variations on the signal propagation delay of a CMOS buffer are described in this paper. It is shown that delay uncertainty is introduced due to variations in the current flow through a buffer. In addition, the variations in the parasitic resistance and capacitance of an interconnect line also affect the buffer delay. A design methodology that reduces the delay uncertainty of signals propagating along buffer-driven interconnect lines is presented. The proposed methodology increases the current flow sourced by a buffer to reduce the sensitivity of the delay on device and interconnect parameter variations.

1. INTRODUCTION

The rapid scaling of on-chip feature size has produced phenomenal advances in circuit density, chip functionality, and operational clock frequency [1, 2]. This development has also resulted in increased sensitivity of the circuit characteristics on parameter variations. Imperfections in the manufacturing process and environmental effects degrade the quality of signals within a circuit and affect the signal propagation delay. Deviations of a signal from the target delay can cause the loss of critical data, thereby causing a system to malfunction. These deviations of the signal propagation delay from a target value are described as *delay uncertainty*.

Delay uncertainty can be critical for the operation of high speed synchronous circuits. The continuous quest for higher circuit performance has pushed clock frequencies deep into the gigahertz frequencies range, reducing the period of the clock signal well below a nanosecond. Uncertainty in the propagation delay of the clock signal can cause violations of the set-up and hold timing constraints at the data path registers. In addition, delay uncertainty of the data signals can also cause violations of these constraints. To prevent these violations, either the tight timing constraints should be relaxed, or the uncertainty in the signal delay should be reduced. Relaxing the timing constraints, especially at the most critical paths of a circuit, increases the clock period and reduces the circuit performance. Alternatively, reducing delay uncertainty can prevent the violations of the timing constraints, thereby improving the robustness of a circuit and enhancing the circuit performance. In order to develop design methodologies that reduce delay uncertainty, the effects that cause uncertainty in the signal propagation delay should be investigated.

Delay uncertainty is introduced by a number of factors that affect the signal propagation, examples of which include process and environmental parameter variations [3, 4] and interconnect noise [5]. Effects such as the non-uniformity of the gate oxide thickness and imperfections in polysilicon etching [6] can cause variations of the current flow within a transistor, thereby introducing delay uncertainty. The geometrical characteristics of interconnect lines are also affected by imperfections in the photolithography, planarization and metal etching processes [4]. Environmentally induced parameter variations caused by changes in the ambient temperature [7] and external radiation [8] also introduce delay uncertainty.

In this paper, the delay uncertainty of a signal propagating along a CMOS buffer due to process, environmental, and system parameter variations is investigated. It is shown that increasing the buffer size reduces the uncertainty in the signal delay due to parameter variations in both the buffer and the interconnect. The variations in the delay of a CMOS inverter due to device parameter variations are discussed in Section 2. The effect of buffer size on the delay uncertainty introduced by interconnect parameter variations

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is described in Section 3. Finally, some conclusions are presented in Section 4.

2. DELAY UNCERTAINTY DUE TO DEVICE PARAMETER VARIATIONS

The signal propagation delay of a logic gate depends upon the gate size and the magnitude of the current flowing within the gate. Variations of the device parameters can cause the magnitude of the current flow to change, introducing delay uncertainty. Therefore, reducing the effect of the device parameters on the current flow can reduce delay uncertainty. In particular, the delay uncertainty of the active components of the most critical data paths and interconnect lines within a circuit should be reduced to prevent tight timing constraints from being violated.

In the case of a CMOS inverter, a first order relationship between the signal propagation delay and the current through an inverter is presented in [9] as

$$t_D = \left(\frac{1}{2} - \frac{1 - v_T}{1 + \alpha}\right) t_T + \frac{C_L V_{DD}}{2 I_{D0}}, \tag{1}$$

where

$$v_T = \frac{V_{TH}}{V_{DD}}, \tag{2}$$

and t_D is the signal propagation delay, α is the velocity saturation index described in [9], t_T is the transition time of the signal at the input of the inverter, V_{DD} is the supply voltage, and C_L is the capacitive load at the output of a CMOS inverter. V_{TH} is the threshold voltage of the active transistor during a signal transition and I_{D0} is the drain current flowing through that transistor (defined at $V_{GS} = V_{DS} = V_{DD}$). I_{D0} is often used as an index of the current drive of a MOSFET transistor and depends upon the transistor size,

$$I_{D0} = \frac{W}{L_{eff}} P_{dev}, \tag{3}$$

where W and L_{eff} represent the width and the effective channel length of a transistor, respectively, and P_{dev} represents the effect of the device parameters on the current flow.

According to MOSFET transistor models first proposed by Shockley in [10] and Sakurai and Newton in [9], the primary factors that affect the drain current within a transistor are the carrier mobility (μ_o), the gate oxide capacitance (C_{ox}), the threshold voltage (V_{TH}), and the power supply voltage (V_{DD}). The dependence of these factors on process, environmental, and system parameters is shown in Fig. 1. These parameters are temperature ($Temp$), gate oxide thickness (t_{ox}), substrate doping density (N_A), and power supply voltage (V_{DD}). A variation of these parameters causes a change in the magnitude of the current flow within a transistor and, eventually, uncertainty in the propagation delay.

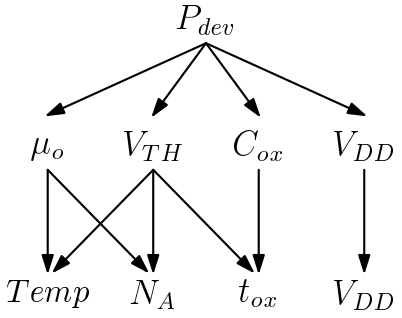


Figure 1: Dependence of device parameters on process, environmental, and system parameters.

In order to evaluate the effect of the variation of the device parameters on the inverter propagation delay, I_{D0} is substituted from (3) into (1), yielding

$$t_D = \left(\frac{1}{2} - \frac{1 - v_T}{1 + \alpha}\right) t_T + \frac{C_L V_{DD}}{2 \frac{W}{L_{eff}} P_{dev}}. \tag{4}$$

Differentiating (4) with respect to P_{dev},

$$\frac{\partial t_D}{\partial P_{dev}} = -\frac{C_L V_{DD}}{2 \frac{W}{L_{eff}} P_{dev}^2} \quad . \tag{5}$$

As shown in (5), the sensitivity of inverter delay on variations of the device parameters $\frac{\partial t_D}{\partial P_{dev}}$ is inversely proportional to the inverter size. The delay uncertainty due to variations in the drain current can therefore be reduced by increasing the size of the inverter. In addition, as shown in (4), the propagation delay of an inverter also decreases with increasing inverter size. The reduction in delay is shown in Fig. 2 where the inverter size is increased by up to five times. The inverter delay is calculated analytically from (1) and simulated using Spectre® simulator[1] [11]. The differ-

[1] Spectre® is a registered trademark of Cadence Design Systems Incorporated.

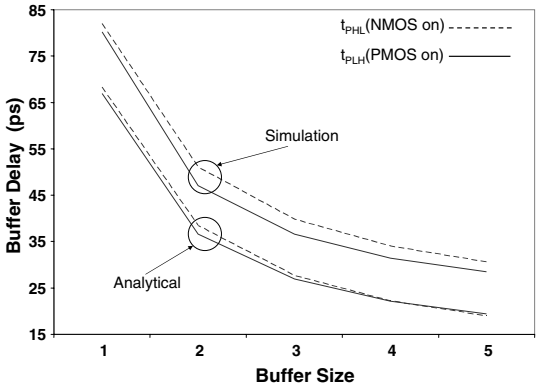


Figure 2: Reduction in delay with increasing inverter size.

ence between the calculated and simulated delay values is caused by considering in (5) only the I_{D0} of the active transistor during a signal transition. The short-circuit current flowing through the inactive transistor is ignored and therefore the calculated delay is smaller. The delay reduction, however, is similar in both the calculated and the simulated propagation delay, as shown in Fig. 2.

The effect of device parameter variations on the inverter propagation delay is shown in Fig. 3. Note that the variation of different device parameters has a different effect on the delay uncertainty. Increasing the buffer size reduces the delay sensitivity on the variation of the device parameters, as described by (5). As shown in Fig. 3, the variation of the power supply voltage (V_{dd}) is the dominant effect that introduces delay uncertainty, followed by variations in the gate oxide thickness (t_{ox}) and temperature ($temp$). In addition to these parameters, the variation of the channel doping concentration (N_A) by $\pm 5\%$ has also been investigated, however the introduced delay uncertainty is shown to be negligible. It is shown in Fig. 3 that the delay uncertainty caused by different parameter variations is inversely proportional to inverter size.

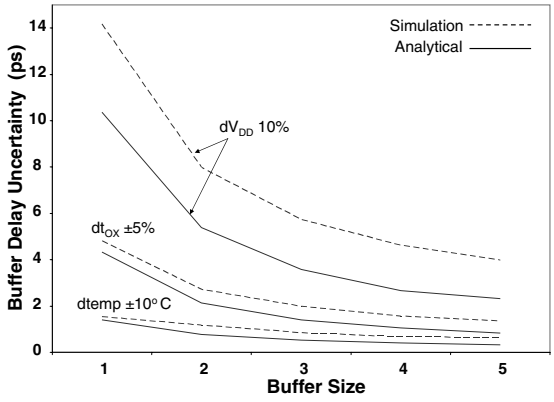


Figure 3: Reduction in delay uncertainty due to device parameter variations with increasing buffer size.

As shown in (1), the propagation delay of a signal transition also depends upon the transition time t_T of the input signal. The effect of a variation in t_T on the delay uncertainty is illustrated in Fig. 4, where the delay uncertainty due to a variation of V_{dd} of 10% is shown for a variation of t_T between 30 ps and 80 ps. Increasing the input signal transition time increases the delay uncertainty; however, the effect of increasing the inverter size is dominant, and the overall delay uncertainty is decreased. Similar delay uncertainty trends are shown in Figs. 5(a) and 5(b) for a $\pm 5\%$ variation in t_{ox} and a $\pm 10^o\ C$ variation in temperature, respectively.

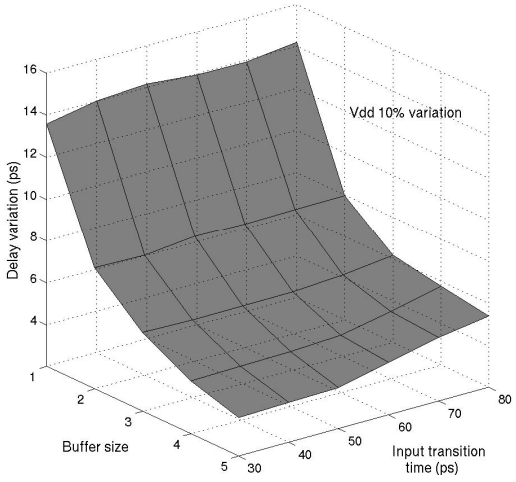
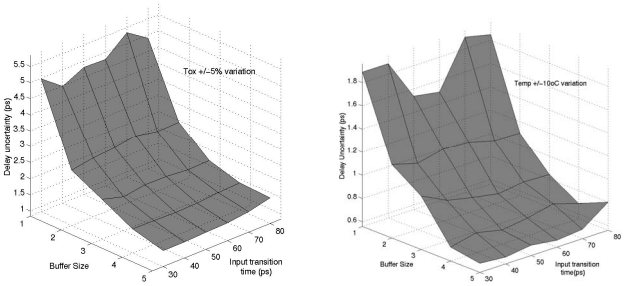


Figure 4: Delay uncertainty due to 10% V_{dd} variation for different input transition time.



(a) Delay uncertainty due to $\pm 5\%$ t_{ox} variation for different input transition time.

(b) Delay uncertainty due to $\pm 10^o C$ variation in temperature for different input transition time.

Figure 5: Effect of input signal transition time t_T on delay uncertainty.

3. DELAY UNCERTAINTY DUE TO INTERCONNECT PARAMETER VARIATIONS

In addition to the parameters of active devices, manufacturing process variations affect also the geometrical characteristics of on-chip interconnect lines. Fluctuations in the metal etching process can cause variations in the wire width and spacing among adjacent metal lines. Furthermore, imperfections in the chemical-mechanical planarization process introduce variations in the metal thickness of an interconnect line and in the dielectric thickness between metal layers. These effects create variations in the parasitic resistance and capacitance of a metal line, therefore affecting the effective load of a buffer.

In order to evaluate the effect of load variations on buffer delay, the interconnect line structure shown in Fig. 6 is simulated using Spectre®. In particular, the effect on buffer

delay caused by $\pm 10\%$ variation in the line resistance and capacitance is investigated. The following three scenarios are considered, depending on the part of the line affected by parameter variations:

i. $\pm 10\%$ variation in line resistance and capacitance at the first half of the line closer to driving buffer.

ii. $\pm 10\%$ variation in line resistance and capacitance at the second half of the line away from the buffer.

iii. $\pm 10\%$ variation in line resistance and capacitance at the entire line length.

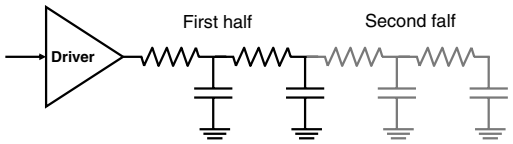


Figure 6: Circuit model to evaluate the effect of line parameter variations on buffer delay

The uncertainty in the buffer delay for these three cases is illustrated in Fig. 7, where the buffer size is increased by up to five times. It is shown that for each case the delay uncertainty is reduced with increasing buffer size. Note in Fig. 7 that the uncertainty in buffer delay is less when the line parameters are affected at the second half of a line. This reduction in delay uncertainty is caused by the shielding effect of the first half of the line that isolates the buffer output from the parameter variations at the second half.

4. CONCLUSIONS

The effects of device parameter variations on the delay uncertainty of a signal propagating through a CMOS buffer are investigated. It is demonstrated that delay uncertainty is inversely proportional to the transistor current. Increasing the inverter size, therefore, reduces the delay uncertainty caused by device parameter variations. In addition, the delay uncertainty due to interconnect parameter variations is examined. It is shown that variations in line parameter in the proximity of a driving buffer have a greater effect on buffer delay. Increasing the buffer size alleviates these effects and reduces delay uncertainty.

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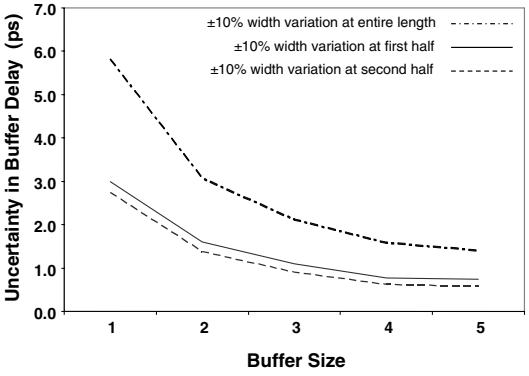

Figure 7: Reduction in delay uncertainty due to interconnect parameter variations with increased buffer size

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