A BULK-DRIVEN CMOS OTA WITH 68 dB DC GAIN

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ABSTRACT

An ultra-low voltage rail-to-rail operational transconductance amplifier (OTA) based on a standard digital 0.18 μm CMOS process is described in this paper. Techniques for designing a 0.8 volt fully differential OTA are discussed including bias and reference current generator circuits. To achieve rail-to-rail operation, complementary input differential pairs are used, where the bulk-driven technique is applied to reduce the threshold limitation of the MOSFET transistors. The OTA gain is increased by using auxiliary gain boosting amplifiers. This additional circuitry enables the OTA to operate at 0.8 volts, achieving an open loop gain of 68 dB while consuming 94 μW. The DC gain of the amplifier is the highest gain achieved to date in bulk-driven amplifiers.

1. INTRODUCTION

The reduction in the minimum dimensions in VLSI technologies along with the trend of using small portable devices necessitates reduced power supply voltages. In order to facilitate submicrometer high density systems on a single integrated circuit (IC), voltage levels must be lowered to ensure reliability. Threshold voltages of future CMOS technologies may not decrease much below what is available today, making it difficult to design analog circuits with lower supply voltages.

In analog circuit design, the threshold voltage of a transistor should be lowered in proportion to the reduction in the supply voltage to appropriately bias the device. This characteristic makes standard low voltage analog circuits incompatible with CMOS technology trends. To combat this conflict without requiring the development of expensive CMOS technologies with lower threshold voltages, novel circuit design techniques must be developed that are compatible with future CMOS technologies.

A promising approach in low voltage analog circuits is the so-called "bulk-driven" MOSFET method. In this method, the gate-to-source voltage is set to a value sufficient to form an inversion layer, and an input signal is applied to the bulk terminal. In this manner, the threshold voltage of a MOSFET can be reduced or even removed from the signal path.

The concept of a bulk-driven MOS transistor was first proposed by Guzinski *et al.* in 1987 [1] as active components in an OTA differential input stage. Later, in 1991, the concept was used in the practical realization of a software-programmable CMOS telephone circuit [2]. However, not until 1998 [3] did the method draw significant attention as a viable low-voltage analog design technique. Specifically, in [3], a 1 volt Op Amp was designed in a standard CMOS digital process utilizing the depletion characteristics of bulk-driven transistors.

One important drawback of the bulk-driven method, however, is that the body transconductance g_{mb} is approximately five times smaller than the gate transconductance g_m. Thus, when the input differential pair of an amplifier is composed of bulk-driven transistors, the resulting DC gain is relatively low. This behavior is the primary reason for the low gain (around 45 dB) in previously reported bulk-driven amplifiers [3], [4].

In this paper, a 0.8 volt fully differential folded-cascode OTA is presented. Both PMOS and NMOS bulk-driven input differential pairs are used to achieve full rail-to-rail operation. A continuous-time common mode feedback circuit is adopted in order to suppress variations in the output common mode. Four common-source gain boosting amplifiers are used to increase the gain to the target level of 68 dB (the DC gain was around 48 dB before gain boosting). This gain is the highest gain achieved to date in bulk-driven amplifiers. A bias circuitry which generates the required bias voltages for the amplifier core along with a low sensitive reference current generator circuit are also presented

This paper is organized as follows. The design of the amplifier core is presented in Section 2. In Section 3, the bias circuit and reference current generator are described. In Section 4, the circuit layout is presented. In section 5, the performance of the amplifier is summarized and some conclusions are offered in Section 6.

2. THE AMPLIFIER CORE

The amplifier core of an OTA is illustrated in Figure 1. This circuit is based on a fully differential topology with two complementary input pairs. The output branch consists of common gate amplifiers with cascode current loads to increase the gain. A common mode feedback circuit is used with four auxiliary common source amplifiers. The operation of the OTA is explained in greater detail below.

2.1 Rail-to-Rail Operation

Rail-to-rail operation is achieved using a pair of PMOS (M_5 and M_6) and NMOS (M_{33} and M_{34}) transistors at the input stage. This

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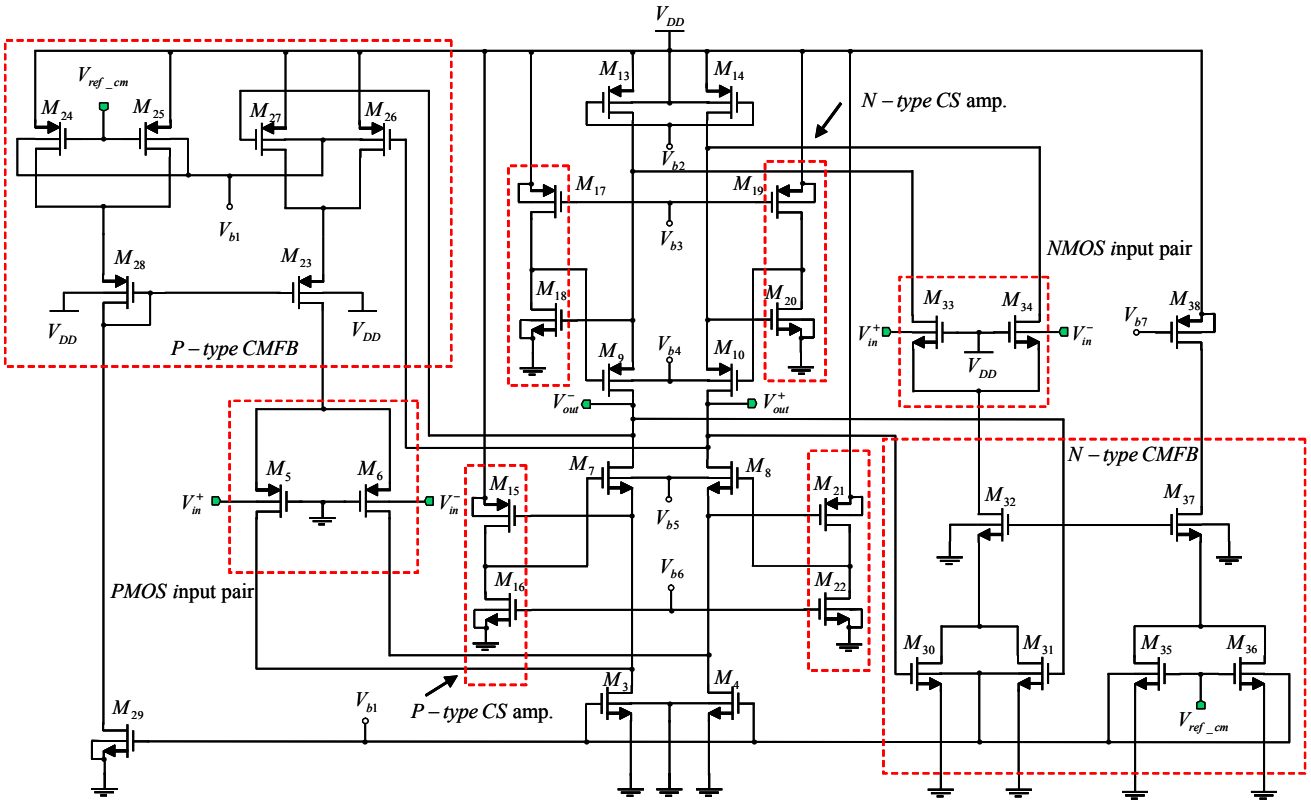

Figure 1. The amplifier core of an OTA

strategy supports rail-to-rail (0 volt to 0.8 volt) operation of the amplifier, thus the input common mode range (ICMR) is extended to the largest possible range. This increased range is achieved since when the input common mode voltage is low, the P-type pair is on and the N-type pair is off (when the input common mode is high, the P-type pair is off and the N-type pair is on). In the middle range, however, both pairs are on, providing a higher overall gain.

2.2 The Output Branch

The output branch of the OTA consists of two symmetric common gate (CG) amplifiers (M_7 and M_8). Both amplifiers have cascode current loads (M_9 and M_{13} and M_{10} and M_{14}) to increase the gain. The bias current is provided to M_7 and M_8 by the current sources M_3 and M_4, respectively, which also operate as current loads for the P-type input pair (M_5 and M_6). Note that a complementary structure is also implemented for the N-type input pair. Transistors M_{13} and M_{14} act as current sources for the N-type input pair.

2.3 Auxiliary CS Amplifiers

Auxiliary common source (CS) amplifiers (M_{15}, M_{16}, M_{21}, and M_{22}, and M_{17}, M_{18}, M_{19}, and M_{20} shown in Figure 1) provide a target open loop gain of at least 60 dB. In this way, stacking multiple transistors in the output branch is avoided, providing more overdrive voltage to maintain the transistors in the saturation region, while simultaneously increasing the voltage gain. The output of the CS amplifier is connected to the gate of the CG amplifier so as to maintain an almost constant source voltage. This source node is fed back as the input voltage to the CS amplifier. In this way, the local feedback action reduces the variations in the bias current when the source voltage of the CG amplifier changes, thereby increasing the output resistance.

2.4 Common Mode Feedback (CMFB)

The CMFB circuit (M_{24}, M_{25}, M_{26}, and M_{27} and M_{30}, M_{31}, M_{35}, and M_{36} shown in Figure 1) is used to suppress the variations in the output common mode, particularly in applications with feedback. These variations occur due to mismatches among the transistors. These mismatches cause a difference between the DC operating voltages in the outputs (V_{out}^+ and V_{out}^-). Furthermore, by forcing the output common mode to a specific level (normally halfway between V_{DD} and ground), the range of the input common mode is increased.

The CMFB circuit was first proposed in [5]. In this configuration, transistors M_{24}, M_{25}, M_{26}, and M_{27} operate in the linear region, acting as voltage controlled resistors. When the DC operating point at the output differs from the target common mode voltage, a change in the tail current of the input pair occurs, resulting in an increment or decrement in the bias currents. This

effect restores the DC operating point to the desired voltage level.

3. BIAS CIRCUIT AND REFERENCE CURRENT GENERATOR

In order to ensure that the transistors operate in the saturation region (or in the linear region for some of the transistors in the CMFB circuit), fixed bias voltages are applied either to the gate or body of the transistors. The bias voltage generator circuit is shown in Figure 2.

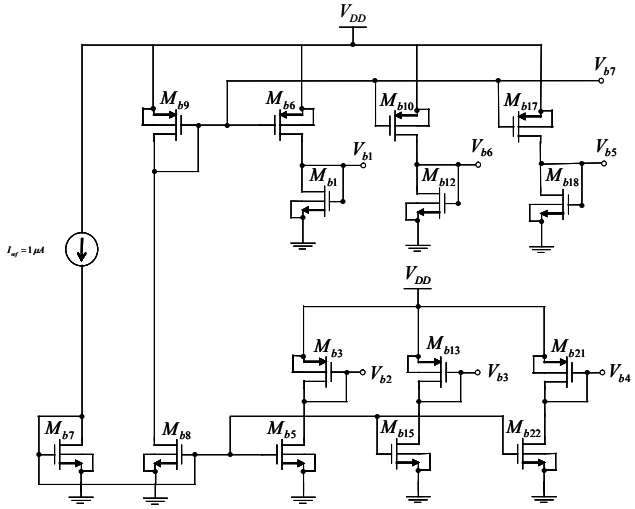

Figure 2. Bias voltage generator circuit

Due to limited voltage headroom, simple voltage dividers are used to generate the bias voltages (V_{b1}-V_{b7} in Figure 1). Transistors M_{b6}, M_{b10}, and M_{b17} act as current mirrors for the transistor M_{b9}, providing the appropriate currents to generate voltages V_{b1}, V_{b5}, and V_{b6}. A complementary structure is also applied to generate voltages V_{b2}, V_{b3}, and V_{b4}. Transistor M_{b8} is the current mirror of M_{b7}, which is biased with a constant current source I_{ref} (1 μA).

A low-sensitivity reference current generator circuit is illustrated in Figure 3. Because the gate and source of M_{c4} and M_{c2} are common for both transistors, and the aspect ratios are equal, $I_{Dc4} = I_{Dc2}$ (neglecting channel length modulation). Furthermore, note that $V_{GSc3} = V_{GSc1} + I_{Dc1}R_{Sc1}$. Thus,

$$\sqrt{\frac{2 \cdot I_{Dc2}}{\mu_n \cdot C_{ox} \cdot (W/L)_{Mc3}}} = \sqrt{\frac{2 \cdot I_{Dc2}}{\mu_n \cdot C_{ox} \cdot K \cdot (W/L)_{Mc3}}} + I_{Dc2} \cdot R_{Sc1}\,, \qquad (1)$$

where K is the ratio between the aspect ratios of M_{c1} and M_{c3}. Rearranging this expression,

$$I_{Dc2} = \frac{2}{\mu_n \cdot C_{ox} \cdot (W/L)_{c3}} \cdot \frac{1}{R^2} \cdot \left(1 - \frac{1}{\sqrt{K}}\right)^2. \qquad (2)$$

In the target circuit, $K = 1.6$ and $R = 5$ KΩ, therefore $I_{Dc2} = 4$ μA. As expected, the current is independent of the supply voltage (to a first order approximation). Transistor M_{c5} mirrors this current to generate a stable 1 μA reference current, which is used in the bias circuit as shown in Figure 2.

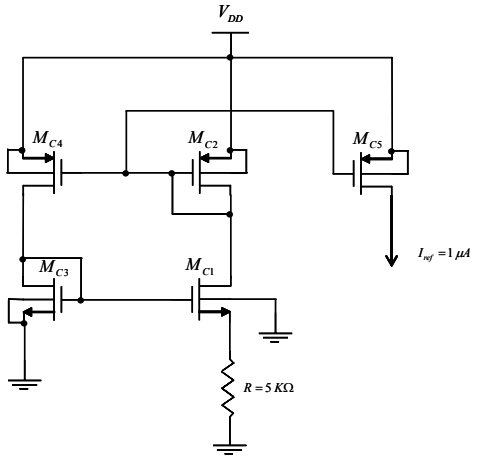

Figure 3. Low sensitivity reference current generator

The aspect ratios of each of the transistors used in the OTA core (Figure 1), the bias circuit (Figure 2) and the reference current generator (Figure 3) are listed in Tables 1, 2, and 3, respectively.

Table 1. Aspect ratios of the transistors used in the amplifier core

Transistor	Width	Length	Ratio
M_3, M_4, M_{29}	5.40 μm	360 nm	15.0
M_5, M_6	16.20 μm	360 nm	45.0
M_7, M_8	2.52 μm	360 nm	7.0
M_9, M_{10}	10.80 μm	360 nm	30.0
M_{13}, M_{14}	21.60 μm	360 nm	60.0
M_{15}, M_{17}, M_{19}, M_{21}	5.04 μm	360 nm	14.0
M_{16}, M_{18}, M_{20}, M_{22}	1.80 μm	360 nm	5.0
M_{24}, M_{25}, M_{26}, M_{27}	20.52 μm	360 nm	57.0
M_{23}, M_{28}	11.16 μm	360 nm	31.0
M_{30}, M_3, M_{35}, M_{36}	3.42 μm	360 nm	9.5
M_3, M_{34}	1.98 μm	360 nm	5.5
M_{32}, M_{37}	2.88 μm	360 nm	8.0
M_{38}	18.36 μm	360 nm	51.0

Table 2. Aspect ratios of the transistors used in the bias circuit

Transistor	Width	Length	Ratio
M_{b1}, M_{b13}	5.04 μm	360 nm	14.0
M_{b3}	10.08 μm	360 nm	28.0
M_{b5}, M_{b22}	2.88 μm	360 nm	8.0
M_{b6}	18.00 μm	360 nm	50.0
M_{b7}	0.40 μm	360 nm	1.1
M_{b8}	0.47 μm	360 nm	1.3
M_{b9}	1.73 μm	360 nm	4.8
M_{b10}	15.12 μm	360 nm	42.0
M_{b12}	1.80 μm	360 nm	5.0
M_{b15}	5.40 μm	360 nm	15.0
M_{b17}	9.43 μm	360 nm	26.2
M_{b18}	0.27 μm	360 nm	0.7
M_{b21}	7.02 μm	360 nm	19.5

Table 3. Aspect ratios of reference current transistors

Transistor	Width	Length	Ratio
M_{c1}	5.52 µm	1380 nm	4.0
M_{c3}	3.80 µm	1520 nm	2.5
M_{c2}, M_{c4}	25.20 µm	1400 nm	18.0
M_{c5}	6.16 µm	1370 nm	4.5

4. CIRCUIT LAYOUT

The layout of the OTA including the bias circuit and current generator is illustrated in Figure 4. A 0.18 µm CMOS twin-well TSMC process is used. Because both the PMOS and NMOS transistors are body biased, a twin-well technology is required in the bulk-driven technique. The double-well only marginally complication the manufacturing process. The use of a twin-well technology, however, is not a significant limitation for the bulk-driven method, since many advanced CMOS technologies use a two well process [6]. As shown in Figure 4, interdigitization and common-centroid methods have been applied in the design of the OTA core so as to decrease mismatches among the transistors [7].

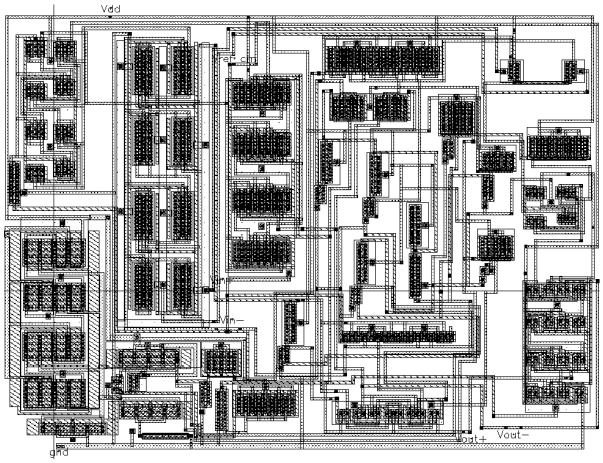

Figure 4. Physical layout of the OTA

5. OTA PERFORMANCE

The gain and phase responses of the OTA, which are obtained from post-layout simulations, are shown in Figure 5. The OTA has an open-loop DC gain of 68 dB, a phase margin of 80°, and a unity-gain bandwidth of 93 MHz, under a no load condition. For a capacitive load of 1 pF, the phase margin increases to 89° while the unity-gain frequency reduces to 8.12 MHz. The OTA operates from a 0.8 volt single power supply and consumes 94 µW. The simulated ICMR and output swing are 800 mV and 700 mV, respectively.

6. CONCLUSIONS

The design of an ultra-low voltage, high performance folded-cascode OTA circuit in a standard digital CMOS process is reported in this paper. To accommodate a low power supply voltage (0.8 volt), the bulk-driven MOSFET approach is used. The low gain disadvantage of the bulk-driven technique is circumvented by employing gain boosting amplifiers, permitting the achievement of a DC gain of 68 dB. Due to a lower body transconductance, bulk-driven amplifiers inherently exhibit relatively poor gain. The low gain is the primary reason why previously reported amplifiers [3], [4] have only exhibited a DC gain as high as 45 dB. The primary conclusion of this paper is that bulk-driven amplifiers can be modified to operate with low power supply voltages while still exhibiting performance levels that satisfy the demands of state-of-the-art mixed-signal circuits.

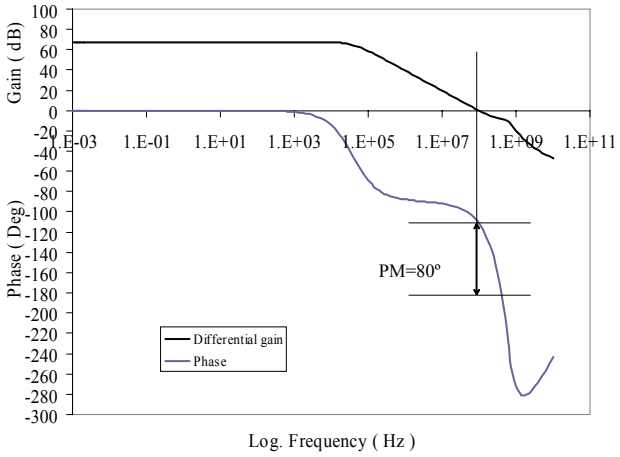

Figure 5. Simulated open loop differential gain and phase vs. log frequency

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