A HIGH-SPEED CMOS OP-AMP DESIGN TECHNIQUE USING NEGATIVE MILLER CAPACITANCE

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ABSTRACT

A method is presented in this paper for the design of high speed CMOS Operational Amplifiers (Op-Amp). The Op-Amp consists of an Operational Transconductance Amplifier (OTA) followed by an output buffer. The OTA is compensated with a *capacitor connected between the input and output of the buffer*. An Op-Amp is designed in a 0.18 μm standard digital CMOS technology and exhibits 86 dB DC gain. The unity gain frequency and phase margin are 392 MHz and 73°, respectively, for a parallel combination of 2 pF and 1 kΩ load. As compared to the conventional approach, the proposed compensation method results in a 1.5 times increase in unity gain frequency and a 35° improvement in the phase margin under the same load condition.

1. INTRODUCTION

With developments in deep submicrometer CMOS processes, the available dynamic range in Operational Amplifiers (Op-Amps) is reduced due to lower power supply voltages [1]. This loss in dynamic range tightens the noise budget. A larger load capacitor should therefore be used to reduce the circuit noise, and hence increase the Signal-to-Noise Ratio (SNR), which in turn decreases the bandwidth of the amplifier [2]. With ever increasing data rates, many mixed-signal applications, however, require fast settling Op-Amps. Op-Amp design has therefore become exceedingly difficult for broadband circuits while maintaining adequate SNR performance. Techniques for increasing the bandwidth of CMOS Op-Amps are needed to accommodate high speed operation with low noise performance.

In this paper, a high-speed CMOS Op-Amp design technique is described. The Op-Amp is comprised of an Operational Transconductance Amplifier (OTA) and a buffer, *where the OTA is compensated with a capacitor connected between the input and output of the buffer*. This arrangement simultaneously improves the unity gain frequency (the bandwidth) and phase margin of the Op-Amp. In a conventional circuit, these two parameters are inversely related to each other (*i.e.*, an increase in one parameter produces a decrease in the other parameter), imposing a tradeoff between speed and stability.

This paper is organized as follows. In Section 2, a compensation method for high speed CMOS Op-Amps is described. The design of a fully-differential Op-Amp based on this approach is explained in Section 3. Post-layout simulation results are described in Section 4. Finally, some conclusions are offered in Section 5.

2. HIGH SPEED OP-AMP DESIGN

A standard method for designing CMOS Op-Amps is to utilize an OTA followed by an output buffer [3], as shown in Figure 1. Note that all internal nodes in the OTA are low impedance nodes, except for the input and output nodes. A buffer is, therefore, used to isolate the OTA from the load. In Op-Amp applications, the load may be resistive, capacitive, or a combination, whereas OTAs typically drive relatively small capacitive loads.

Since the load is connected at the output of the Op-Amp, which is a low impedance node, the load capacitance has little effect on the phase margin of the amplifier. The OTA should, therefore, be internally compensated, otherwise the overall amplifier would exhibit poor stability. As shown in Figure 1, in conventional Op-Amps, the OTA is compensated with a capacitor C_c connected from the output of the OTA to ground [3], [4].

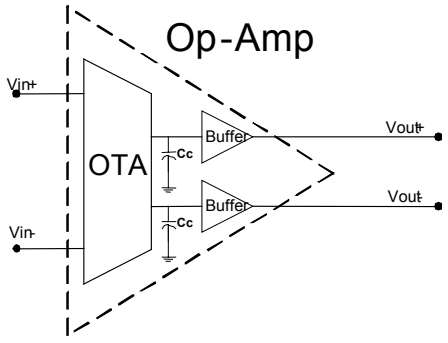

Figure 1. Conventional Op-Amp circuit structure

The high speed Op-Amp method presented in this paper is illustrated in Figure 2. Unlike a conventional circuit structure, the OTA is compensated using a Miller capacitance connected between the input and output of the buffer. Assuming that the Op-Amp drives a parallel combination of a capacitor C_L and a resistor R_L, the effective capacitance seen at the input and output of the buffer is

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$$C_{eff,in} = C_c(1-A) \text{ and } C_{eff,out} = C_L + C_c\left(1-\frac{1}{A}\right). \quad (1)$$

In (1), A represents the gain of the buffer (in this study, $A = 0.6$). Note that since the gain of the buffer is always smaller than one, the effective capacitance seen at the output of the Op-Amp is smaller than the original load capacitance. This effect pushes the first non-dominant pole (*i.e.*, the pole closest to the origin after the dominant pole) to a higher frequency. The location of the dominant pole, however, remains unaltered (to a first order approximation). This argument suggests that in the proposed compensation scheme (see Figure 2), both the unity gain frequency and phase margin are improved as compared to a conventional circuit structure. To avoid a negative effective capacitance at the output of the Op-Amp, however, the compensation capacitance must satisfy the following relation,

$$C_c < C_L\left(\frac{A}{1-A}\right). \quad (2)$$

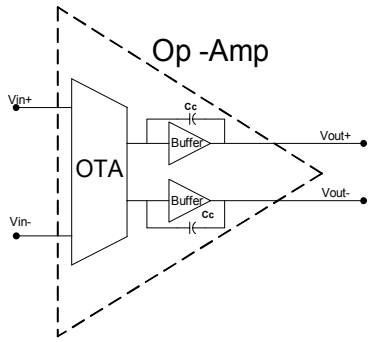

Figure 2. High speed Op-Amp circuit structure

Note that Miller capacitance compensation is extensively used in two-stage Op-Amps and other applications [2]-[5]. Generally speaking, in these applications, the Miller capacitance is connected around an amplifier with a negative high gain (*i.e.*, $A << -1$). The reason for this negative gain is to establish negative feedback. In the approach presented here, the gain of the buffer is positive (but smaller than one). As long as the gain is smaller than one, the positive feedback does not necessarily result in a completely unstable system, as shown in this paper. This paper is the first (according to the authors' best knowledge) to present the application of a negative Miller capacitance to reduce the effective load capacitance so as to achieve both a higher bandwidth and improved phase margin.

3. DESIGN AND IMPLEMENTATION

In this section, the design of a fully-differential Op-Amp is described. The Op-Amp is composed of a fully-differential folded-cascode OTA and two buffers, where the OTA is compensated using the scheme shown in Figure 2. The amplifier is designed based on a 0.18 μm standard digital CMOS process from TSMC [6], and achieves 86 dB DC gain. The unity gain frequency and phase margin of the amplifier are 392 MHz and 73°, respectively, for a parallel combination of 2 pF and 1 kΩ load. The power consumed by the Op-Amp is 12 mW with a 1.8 volt single power supply.

A schematic of the OTA core, which employs a folded-cascode topology, is illustrated in Figure 3. Referring to Figure 3, transistors M_1 and M_2 form the input differential pair. The tail current of the differential pair is provided by a cascode current sink (M_3 and M_4), which sinks a 1mA bias current. The transistor M_5 (M_6) supplies a 1.5 mA bias current for the output branch and input differential pair. As 0.5 mA current flows through transistors M_1 and M_2, the current flowing through M_7 (M_8), M_9 (M_{10}), and M_{11} (M_{12}) is 1 mA. Transistor M_7 (M_8) acts as a common gate amplifier with a cascode current load M_9 (M_{10}) and M_{11} (M_{12}).

The folded-cascode topology provides limited gain (usually, between 60 dB and 65 dB) in deep submicrometer CMOS technologies due to the low intrinsic impedances of the devices. In this paper, the DC gain of the OTA is increased using auxiliary gain boosting amplifiers with a single-ended folded-cascode topology (see Figure 4). In addition, stabilization of the output common mode level is achieved using a continuous-time Common Mode Feedback (CMFB) circuit (see Figure 5). All of the voltages required to bias the OTA core (Figure 3), auxiliary amplifiers (Figure 4), CMFB circuit (Figure 5), and buffers (Figure 6) are generated using a self-biasing circuit (see Figure 7). The remaining components of the Op-Amp are explained in greater detail in the following paragraphs.

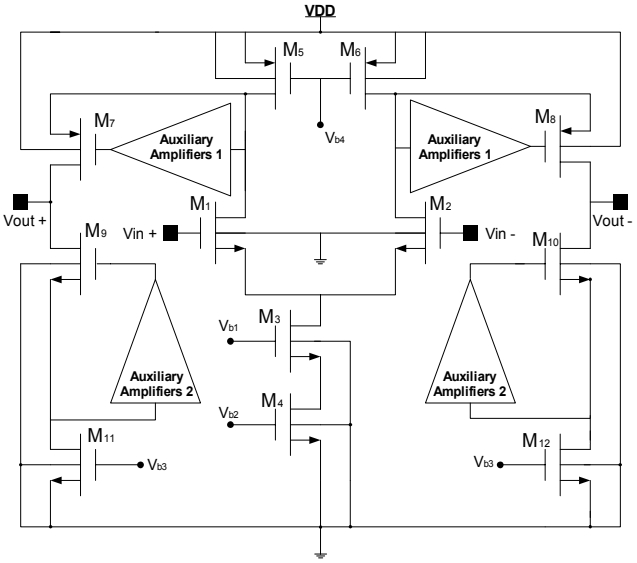

Figure 3. Schematic of the OTA core

As previously mentioned, the auxiliary amplifiers are implemented using single-ended folded-cascode gain stages as shown in Figure 4. As compared to a common source amplifier, folded-cascode gain stages provide higher DC gain. The cost for this enhancement, however, is a small increase in power consumption and area. In Auxiliary Amplifier 1 (2), the transistor M_{Au2} (M_{Au5}) is an NMOS (PMOS) input device, whereas transistor M_{Au3} (M_{Au8}) acts as the cascode PMOS (NMOS) device. Transistors M_{Au1} (M_{Au7}) and M_{Au4} (M_{Au6}) behave as a simple current source and current sink, respectively. The inputs to the Auxiliary Amplifier 1 (2) originate from the drains of M_5 (M_{11}) and M_6 (M_{12}), and the outputs are connected to the gates of M_7 (M_9) and M_8 (M_{10}) (see Figure 3).

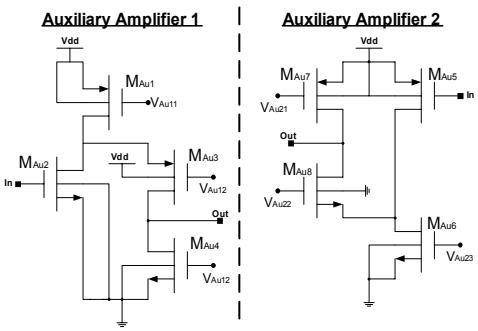

Figure 4. Schematic of the auxilary amplifiers

The continuous-time CMFB circuit shown in Figure 5 is utilized to maintain the output common voltage at the required level (900 mV), while maximizing the output swing of the OTA. The inputs to the circuit are the outputs of the OTA, V_{out+} and V_{out-}. The CMFB circuit amplifies the difference between the average of V_{out+} and V_{out-} and the desired common level V_{cm} (900 mV), and sends a feedback signal V_{B4} to set the bias voltage at the gates of M_5 and M_6 (see Figure 3). Also note that the tail current of the CMFB circuit is set at 50 μA to reduce power consumption.

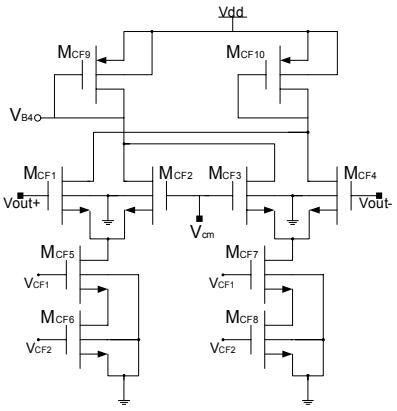

Figure 5. Common mode feedback circuit

A schematic of the buffer used in the Op-Amp is shown in Figure 6, which consists of two cascaded PMOS and NMOS source followers. The PMOS source follower is used as a level shifter to bring the outputs of the OTA to an appropriate voltage level suitable to bias the NMOS source follower. The output common mode level of the Op-Amp is the same as that of the OTA (900 mV). The DC gain of the buffer (*i.e.*, the combined gain of the PMOS and NMOS source followers) is 0.6.

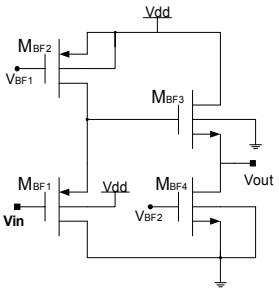

Figure 6. Schematic of the buffer

A schematic of the threshold voltage referenced self-biasing circuit is illustrated in Figure 7. The circuit is used to generate the voltages required to bias the OTA core, auxiliary amplifiers, CMFB circuit, and buffers. The transistors M_{Bias5}, M_{Bias6}, M_{Bias7}, and M_{Bias8} and the 11 kΩ resistor constitute a threshold voltage referenced current generator. Note that a start-up circuit (M_{Bias1}-M_{Bias4}) is utilized to avoid zero current flow in the current generator.

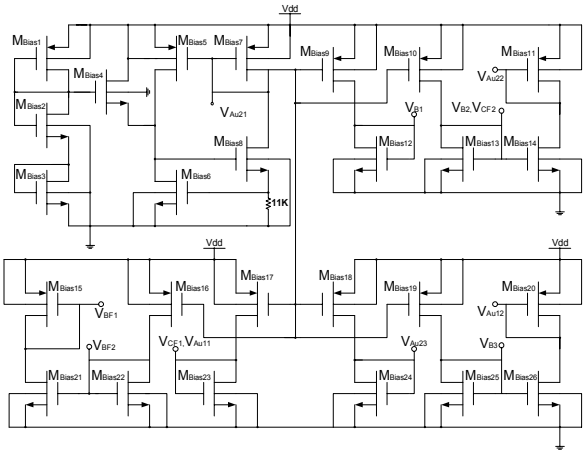

Figure 7. Schematic of the self-biasing circuit

In order to avoid the need for a twin-well process, in Figures 3 to 7, the bulk nodes of all of the PMOS and NMOS transistors are connected to the power supply and ground, respectively.

4. POST-LAYOUT SIMULATIONS

The layout of the overall Op-Amp in the TSMC P-well 0.18 μm CMOS process is shown in Figure 8, including the OTA core, CMFB circuit, buffers, auxiliary amplifiers, and the biasing circuitry. Common-centroid and inter-digitization methods are employed to reduce gradient-induced mismatches among the matched transistors. The resistor is laid out in a polysilicon layer.

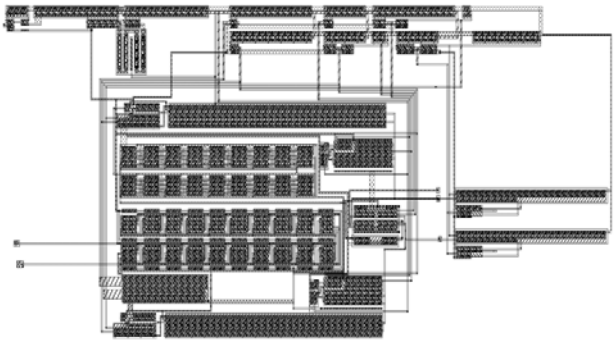

Figure 8. Layout of the Op-Amp

The gain and phase response of the amplifier obtained from the post-layout simulations is illustrated in Figure 9 for a parallel combination of 2 pF and 1 kΩ load and a compensation capacitance C_c=1.4 pF. The DC gain of the Op-Amp is 86 dB. As shown in Figure 9(a), the conventional compensation method

(see Figure 1) results in a unity gain frequency of 251 MHz and phase margin of 37° with C_c=1.4 pF.

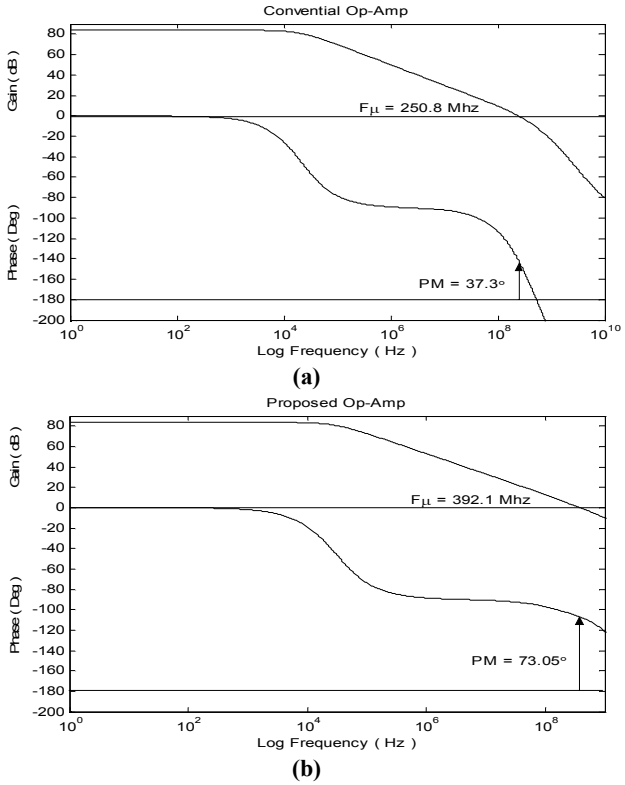

Figure 9. Open loop gain and phase response versus frequency, (a) convential Op-Amp, (b) proposed Op-Amp

The gain and phase response obtained using the proposed compensation scheme (see Figure 2) is shown in Figure 9(b) for the same load and compensation capacitance. In this method, the unity gain frequency and phase margin are 392 MHz and 73°, respectively. Note that both the bandwidth and stability of the Op-Amp are significantly improved.

As shown in Figure 9, the location of the dominant pole is close for both methods, as discussed in Section 2. This behavior demonstrates that the proposed compensation scheme shifts the first non-dominant pole to a higher frequency, while maintaining unaltered the location of the dominant pole.

The unity gain frequency (f_μ) and phase margin (P.M.) of both the conventional and proposed compensation schemes are listed in Table 1 for various loads. Note that the compensation capacitance is a constant C_c=1.4 pF in all cases. These results show that the proposed compensation scheme simultaneously results in a higher unity gain frequency and an improved phase margin under all load conditions. The improvement, however, is dependent upon the specific values of the compensation capacitance, load resistor, and load capacitance.

5. CONCLUSIONS

A method is presented to efficiently compensate buffered Op-Amps. In this approach, the OTA is compensated by connecting a capacitance between the input and output of the buffer. This configuration results in a significant improvement both in the unity gain frequency and phase margin, providing higher speed and improved stability.

A fully-differential Op-Amp is designed in a TSMC P-well 0.18 μm standard digital CMOS process using the proposed compensation scheme. The DC gain of the amplifier is 86 dB. The unity gain frequency and phase margin of the amplifier are 392 MHz and 73°, respectively, for a parallel combination of 2 pF and 1 kΩ load. The total power consumption of the Op-Amp is 12 mW with a 1.8 volt single power supply.

Table 1. Unity gain frequency (f_μ) and phase margin (P.M.) for conventional and proposed Op-Amp circuit structures

Conventional		Proposed			
f_μ	P.M.	f_μ	P.M.	R_L	C_L
224 MHz	20°	672 MHz	69°	∞	1 pF
166 MHz	14°	413 MHz	73°	∞	2 pF
138 MHz	11°	299 MHz	73°	∞	3 pF
287 MHz	49°	582 MHz	80°	1 kΩ	1 pF
251 MHz	37°	392 MHz	73°	1 kΩ	2 pF
222 MHz	31°	307 MHz	67°	1 kΩ	3 pF
298 MHz	41°	617 MHz	75°	2 kΩ	1 pF
248 MHz	30°	402 MHz	71°	2 kΩ	2 pF
215 MHz	24°	308 MHz	66°	2 kΩ	3 pF
297 MHz	37°	630 MHz	73°	3 kΩ	1 pF
242 MHz	27°	405 MHz	70°	3 kΩ	2 pF
208 MHz	22°	306 MHz	66°	3 kΩ	3 pF
138 MHz	17°	154 MHz	45°	1 kΩ	10 pF
103 MHz	9°	125 MHz	52°	10 kΩ	10 pF
274 MHz	28°	654 MHz	70°	10 kΩ	1 pF
311 MHz	71°	1.36 GHz	93°	1 kΩ	0 pF

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