Efficiency Optimization of Integrated DC-DC Buck Converters

Gregory Sizikov, Avinoam Kolodny
Electrical Engineering Department
Technion, IIT
Haifa, Israel 3200
gregory.sizikov@intel.com
kolodny@ee.technion.ac.il

Eby G. Fridman
Electrical and Computer Engineering Department
University of Rochester
Rochester, New York 14627
friedman@ece.rochester.edu

Michael Zelikson
Intel Architecture Group
Intel Corporation
Haifa, Israel 31015
michael.zelikson@intel.com

Abstract - An analytic method to evaluate frequency dependent losses in on-chip DC-DC buck converters is presented in this paper. Microprocessors or chipsets exhibit wide dynamic range of load current varying from 50mA up to 1.5 A per phase at full operation. Peak efficiency is shown to occur when the load current related losses and the inherent losses of the DC-DC converter are equal. Efficiency optimization methods are described for light and heavy load scenarios. The primary design objective is to maintain the load at the peak of the efficiency curve. A SPICE based circuit model of a DC-DC converter is applied to validate the proposed analytic methods.

Keywords: on-chip DC-DC efficiency, frequency dependent losses, air core inductor

I. INTRODUCTION

With the increasing attention to energy savings and battery life in mobile devices [1], microprocessors and chipsets integrate different functional blocks such as I/O, analog circuits, memory, and graphics on the same die. For power efficiency, each block may operate at a different DC supply voltage, resulting in multiple DC-DC power converters on the same printed circuit board, which occupy a growing fraction of the board area. Integrated on-die DC-DC converters may provide a solution for the PCB resource issue, enabling a larger number of different on-chip voltage supplies.

Power efficiency is one of the most critical parameters of on-chip DC-DC converters. These converters require inductors which cannot be efficiently implemented on die, but can be embedded inside the package. Typically, these inductors have an air-core (no ferromagnetic materials are used), and therefore exhibit a low inductance in the range of a few nH. A buck converter needs to operate at high switching frequencies (hundreds of MHz) for the inductor to be sufficiently small. Existing work on analytic modeling of integrated DC-DC converter efficiency [2-5] does not properly address the combination of high switching frequencies and air-core inductors. Consequently, a need for considering high frequency effects, such as the skin effect, arises. Since the dominant losses are related to the ripple current (in contrast to discrete component based converters), a novel procedure for light load efficiency optimization is proposed.

The process of analytic model parameter extraction is based on circuit simulation and is independent of implementation. The target converter supports 2 volts to 1 volt conversion, a filter inductor of 3 nH embedded in a package [6], and a switching frequency in the range of hundreds of MHz. The maximum load is targeted at 1.5 amperes.

This paper is organized as follows: the analytic linear loss model is presented in section 2 as well as a method for extracting the model parameters using the Ansoft field solver. Peak efficiency equilibrium of the converter losses and load related losses is shown in section 3. Switching frequency optimization is presented in section 4. Optimization of the efficiency under light load conditions by area scaling and frequency optimization is addressed in section 5. Validation of the analytic results by simulation is presented in section 6. The paper is concluded in section 7.

II. ON-CHIP DC-DC LOSS MODEL

A. *Analytic Efficiency Model*

The efficiency of a DC-DC buck converter is

$$\eta = \frac{P_{out}}{P_{loss} + P_{out}} = \frac{I_{load} V_{out}}{P_{fet} + P_{ind} + I_{load} V_{out}}. \quad (1)$$

The losses are within the power FET and inductor. The major power FET losses are $C_b V_{in}^2 f_{sw}$ switching losses within the pulse width modulator (PWM) where C_b is the effective switching capacitance and $I^2 R_{ds}$ losses due to the current in the transistors. The power dissipation in the inductor is primarily due to $I^2 R(f)$ losses. $R(f)$ is the frequency dependent inductor resistance, in which the DC component is denoted by R_i. The current in the power path of the converter is a superposition of the triangular ripple current ΔI and DC load current I_{load}. Equations (2) and (3) describe the losses in the power FET and the inductor, respectively,

Supported by Technion Advanced Circuit Research Lab (ACRC)

$$P_{fet} = \underbrace{C_b V_{in}^{\ 2} f_{sw}}_{P_{cvf}} + R_{ds}\left(I_{load}^{\ 2} + \frac{\Delta I^2}{12} \right), \tag{2}$$

$$P_{ind} = R(f)\left(I_{load}^{\ 2} + \frac{\Delta I^2}{12} \right). \tag{3}$$

Combining these two expressions in terms of load and ripple current,

$$P_{ripple} = \frac{\Delta I^2}{12}\left(R_{ds} + R(f)\right), \tag{4}$$

$$P_{load} = I_{load}^{\ 2}\left(R_i + R_{ds}\right). \tag{5}$$

The losses are composed of two parts: P_{cvf} together with P_{ripple}, which is independent of the load current, and P_{load}, which is a function of the load current. The efficiency of a DC-DC buck converter can be rewritten as

$$\eta = \frac{I_{load} V_{out}}{P_{cvf} + P_{ripple} + P_{load} + I_{load} V_{out}}. \tag{6}$$

With these expressions, the individual losses of a DC-DC converter can be investigated. The following section describes a method to obtain the analytic parameters from an initial circuit design.

B. Circuit-Level Efficiency Model

The losses are modeled using a DC-DC converter circuit, as shown in Fig. 1. The power FETs are modeled as ideal switches, resistors R_{ds}, and switching capacitance C_b. The inductor is modeled as an ideal inductor with a frequency dependent effective series resistance (ESR) $R(f)$. L_{ac} represents the high frequency limit of the inductance.

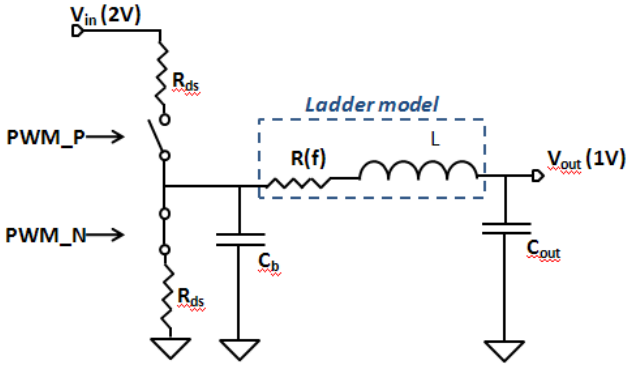

Figure 1: Frequency dependent losses model of a DC-DC converter

The output capacitor losses are neglected due to the low ESR of the capacitor (not shown in Fig. 1). Additional losses such as the power dissipated by the control compensation filter, package, leakage, and die power grid are neglected as these components are small as compared to the aforementioned losses.

C. Circuit Model Parameter Extraction

Equation (4) describes the ripple current related losses both in the driver and the inductor. Previous work ignored the skin effect in the inductor [7] or assumed a constant R_{ac} [8]. In this paper, the skin effect is modeled as a frequency dependent resistance,

$$R(f) = R_i + R_{ac}\sqrt{\frac{f}{f_0}}. \tag{7}$$

The air-core package embedded inductor structure is described in the Ansoft Q3D field solver. R_i, R_{ac}, and L_{ac} are extracted where f_o is chosen within the range of the projected switching frequency. The frequency dependent resistance of the air-core inductor is shown in Fig. 2. The resistance at 150 MHz is 150 mΩ while R_i at DC is only 25 mΩ. This dramatic difference results in the skin effect being the dominant factor in the inductor resistance. Note in Fig. 4 that using R_{ac} to describe the skin effect may not be sufficiently accurate. An RL multi-branch ladder model is therefore used [9] to capture the frequency dependence in SPICE. A fit of the analytic model, Ansoft Q3D simulation, and RL ladder models is shown in Fig. 2, where a maximum error of the model of 8% is exhibited. Note that extraction process of switching capacitance C_b is described in [9] and is based on sweeping the DC-DC converter driver circuit frequency.

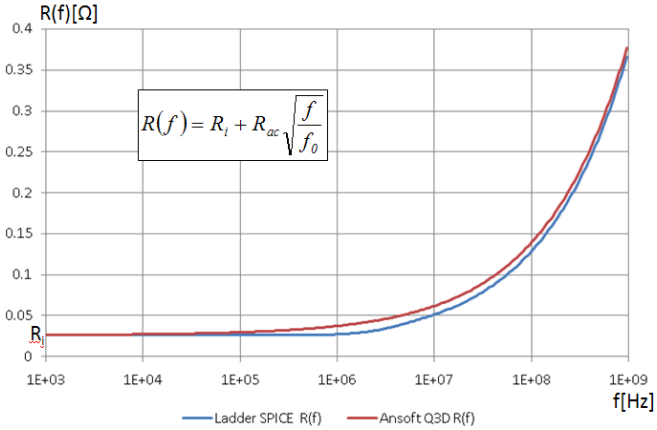

Figure 2: Frequency dependent inductor resistance model, Ansoft Q3D simulation, and SPICE ladder circuit model

III. Peak Efficiency of the DC-DC Converter

Differentiating (6) with respect to I_{load} and equating to zero produces a load current I_{load} that maximizes efficiency, see (8). Note that at the maximum efficiency, the converter inherent losses are equal to the load current related losses.

$$I_{load} = \sqrt{\frac{P_{cvf} + P_{ripple}}{R_i + R_{ds}}} \tag{8}$$

$$\underbrace{I_{load}^{\ 2} \cdot (R_i + R_{ds})}_{Output} = \underbrace{P_{cvf} + P_{ripple}}_{Inherent} \tag{9}$$

Equation (8) can be used to evaluate the optimal load current for a given integrated DC-DC converter. The integrated converter may be modified during operation to change the optimal I_{load}. The selection of the load current I_{load} at peak efficiency depends upon the load usage model and the specific power scheme.

A common practice in DC-DC converters is to use a multiphase structure where multiple identical converter blocks, *i.e.*, phases, are connected in parallel and the current is summed at the output node. The switching control signals are interleaved equally between the phases. The motivation to use multi-phase circuits is due to limitations in the passive components, and related area constraints.

The limit in the number of phases is the per phase current ripple and the requirement to produce an accurate interleaved switching frequency reference waveform. In the multi-phase case, each phase operates optimally as a single standalone converter, delivering I_{load}/n DC current to the output current summing node, where n is the number of phases. In a multi-phase structure, each phase is independent of the other phases in terms of efficiency. A multi-phase converter can be optimized for heavy loads as the peak efficiency current of a single phase is multiplied by the phase count n.

A multi phase circuit can be constrained by the maximum inductance and die area. These resources are divided among the n phases. During operation certain phases may be switched of or their area may be scaled to satisfy light load efficiency mechanisms, as described in section V.

IV. Optimization of Switching Frequency

The switching frequency can be optimized independent of the load current using only P_{cvf} and P_{ripple} (see (2), (4), and (5)). Differentiating P_{cvf} and P_{ripple} with respect to f_{sw}, marked f, and equating to zero results in

$$f^3 + f^{1/2}\frac{R_{ac}A^2}{8C_bV_{in}^2\sqrt{f_0}} = \frac{A^2(R_i+R_{ds})}{6C_bV_{in}^2}, \tag{10}$$

$$A = \frac{V_{in}}{L_{ac}}\frac{V_{out}}{V_{in}}\left(1-\frac{V_{out}}{V_{in}}\right). \tag{11}$$

Equation (10) is intractable in f. If the skin effect is neglected, $R_{ac} = 0$, making the solution of (10) the same as in [4],

$$f = \left(\frac{R_i+R_{ds}}{6}\frac{A^2}{V_{in}^2C_b}\right)^{1/3}. \tag{12}$$

If the switching frequency is high (hundreds of MHz), the power path resistance is dominated by the skin effect,

$$R_{ac}\sqrt{\frac{f}{f_0}} >> (R_{ds}+R_i). \tag{13}$$

In this case, the solution of (10) is

$$f = \left(\frac{R_{ac}A^2}{8C_bV_{in}^2\sqrt{f_0}}\right)^{2/5}. \tag{14}$$

In Fig. 3, a numerical solution of (10) is shown for an inductance of 3 nH. The asymptotes of P_{cvf} and P_{ripple} are also shown. The minimum loss is graphically found at approximately 120 MHz. The analytic solution without the skin effect in (12) results in the minimum loss occurring at 80 MHz. The skin effect dominated solution in (14) results in a 100 MHz optimal switching frequency. A solution that includes both effects is higher than each case since the ripple current is reduced to compensate both the DC and AC resistances.

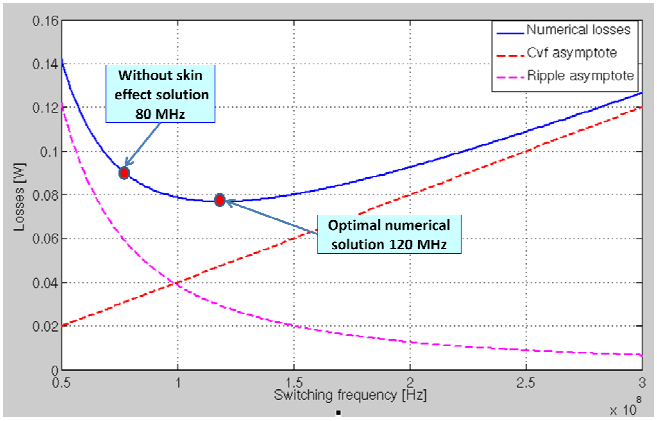

Figure 3: Frequency dependent losses vs f_{sw}

An intuitive analogy for this model is two resistors connected in parallel. The equivalent resistor is therefore always smaller than the smallest resistor. Similarly, the numerical solution is higher than each partial solution. Considering frequency dependent losses of the inductor results in a choice of optimal switching frequency that reduces losses by 15% as compared to the case where the skin effect is ignored.

V. Optimization for Light Load

One of the major drawbacks of switching DC-DC converters is inherent losses, *i.e.*, P_{cvf} and P_{ripple}, do not scale with the load current. Therefore, at light loads, the efficiency of the converter significantly drops and may fall below an acceptable range. Area scaling methods to improve the efficiency at light loads are proposed in [4] and [10]. Modern integrated circuits, such as microprocessors or chipsets, exhibit high dynamic range of the load current ranging from 50 mA to 1.5 A. Optimization for light loads is therefore critical.

A known method to increase efficiency at light loads is to scale the area of the bridge transistors. The area scaling parameter r is the ratio of the active bridge width to the total width. The optimal width for a given load current can be derived from [10] and decreases linearly with smaller load currents. Area scaling is performed by disabling portions of the power stage. In [4], the switching frequency remains constant when area scaling is performed. Based on the switching frequency optimization method illustrated in Fig. 3, the optimal switching frequency is recalculated for each r between 0 and 1. This procedure results in an increased switching frequency within a smaller area, as depicted in Fig. 4. An intuitive explanation for this surprising result is that P_{cvf} rises linearly with frequency whereas P_{ripple} decreases as $n^{1.5}$ and the losses are heavily dominated by P_{ripple}. This effect occurs despite the additional resistance due to the skin effect with rising switching frequency. The

optimal frequency increases while maintaining a balance between the two types of losses.

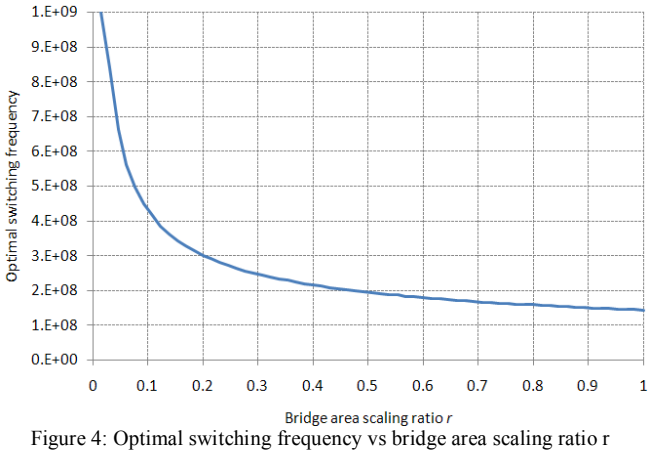

Figure 4: Optimal switching frequency vs bridge area scaling ratio r

The effect of this rise in overall efficiency is dramatic. For example, when the bridge area is scaled to one tenth of the maximum size (r = 0.1), the efficiency improves by 25% (from 60% to 85%) while the switching frequency rises from 120 MHz to 350 MHz, as shown in Figs. 4 and 5. Most of this improvement is achieved by increasing the switching frequency.

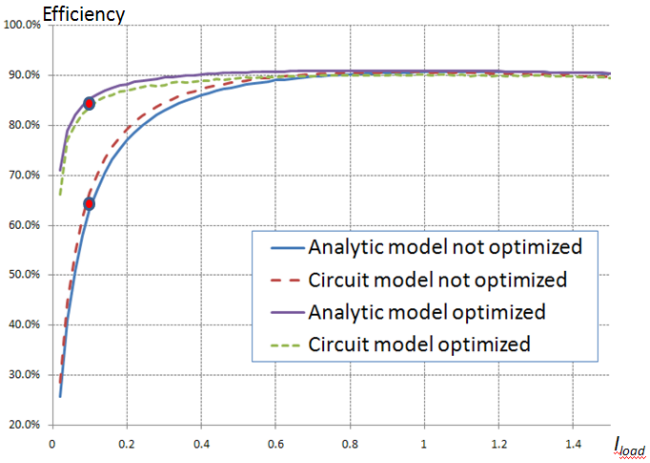

Figure 5: Optimized and non-optimized simulated vs analytic efficiency

SPICE simulations are used to characterize the DC-DC converter architecture [7] and to verify the analytic expressions. The power stage circuit is the same as shown in Fig. 2 where the parameters are based on a modern Intel process. The input voltage is 2 volts, the output voltage is 1 volt, and the inductance is 3 nH. The output capacitance is 0.4 uF. The control scheme is described by an ideal Laplace type 3 transfer function. To consider the skin effect, the output filter inductor is modeled by an *RL* ladder. Comparing the simulations with the analytic model (as described by (1)) of the efficiency η as a function of load current is shown in Fig. 5 and exhibits a maximum error of 7%. Note that the simulation data accurately match the analytic model for both the optimized and non-optimized operating modes of the buck converter.

VI. Conclusions

A frequency dependent analytic model for the power losses in an on-chip DC-DC buck converter is described. The converter employs a small air-core in-package inductor and features a high switching frequency (hundreds of MHz). Optimization of the switching frequency considers the skin effect of the inductor.

The proposed switching frequency optimization methodology is applied together with bridge width scaling for a specific load current [10] to further improve the converter efficiency. SPICE simulations are used to validate the analytic model and to extract the model parameters.

Note that in contrast to the pulse frequency modulation technique, which focuses on decreasing $C_b V_{in}^2 f_{sw}$ losses the proposed approach focuses on decreasing ripple related losses. Upcoming research will consider other types of losses that are neglected in the present work.

VII. References

[1] T. Rahal-Arabi, H. J. Park, and J. Hahn, "Power Delivery for the Next Generation Mobile Platform," *Proceedings of the IEEE Advanced Packaging and Systems Symposium*, pp. 1-4, December 2008.

[2] R. Modak and M. S. Baghini, "A Generic Analytical Model of Switching Characteristics for Efficiency Oriented Design and Optimizations of CMOS Integrated Buck Converters," *Proceedings of the IEEE International Conference on Industrial Technology*, pp. 1-6, February 2009.

[3] V. Kursun, S. G. Narendra, V. De, and E. G. Friedman, "Efficiency Analysis of a High Frequency Buck Converter for On-Chip Integration with a Dual-VDD Microprocessor," *Proceedings of the European Solid-State Circuits Conference*, pp. 743-746, September 2002.

[4] G. Schrom, *et al.*, "Optimal Design of Monolithic Integrated DC-DC Converters," *Integrated Circuit Design and Technology*, pp. 1-3, 2006.

[5] V. Kursun, V. De, E. G. Friedman, and S. G. Narendra "Monolithic Voltage Conversion in Low Voltage CMOS Technologies," *Microelectronics Journal,* Vol. 36, pp. 863-867, January 2005.

[6] P. Hazucha, *et al.*, "A 233-MHz 80%-87% Efficient Four-Phase DC-DC Converter Utilizing Air-Core Inductors on Package," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 4, pp. 838 – 845, April 2005.

[7] J. Lee, G. Hatcher, L. Vandenberghe, and C. K. Ken Yang, "Evaluation of Fully-Integrated Switching Regulators for CMOS Process Technologies," *IEEE Transactions on Very Large Scale Integrated Systems*, Vol. 15, No 9, pp. 1017 – 1027, September 2007.

[8] Y. Katayama, S. Sugahara, H. Nakazawa, and M. Edo, "High-Power-Density MHz-Switching Monolithic DC-DC Converter with Thin-Film Inductor," *Proceedings of the IEEE, Annual Power Electronics Specialists Conference,* pp. 1485 – 1490, June 2000.

[9] G. Sizikov, E. G. Friedman, A. Kolodny and M. Zelikson, "Frequency Dependent Efficiency Model of On-Chip DC-DC Buck Converters", *Proceedings of the IEEEI, 26th Convention of Electrical and Electronic Engineers in Israel,* November 2010.

[10] S. Kim and D. P. Neikirk, "Compact Equivalent Circuit Model for the Skin Effect,"*Proceedings of the IEEE International Microwave Symposium,* Vol. 3, pp. 1815-1818, June 1996.

[11] R. W. Erickson and D. Maksimovic. *Fundamentals of Power Electronics, 2nd Edition*, University of Colorado, 2001.