Estimation of On-Chip Simultaneous Switching Noise in VDSM CMOS Circuits

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Abstract— **On-chip simultaneous switching noise (SSN) has become an important issue in the design of power distribution networks in current VLSI/ULSI circuits. An analytical expression characterizing the simultaneous switching noise voltage is presented here based on a lumped RLC model. The waveform describing the SSN voltage is quite close to the waveform obtained from SPICE. The peak value of the simultaneous switching noise voltage based on this analytical expression is within 10% as compared to SPICE simulations.**

I. Introduction

The trend of next generation integrated circuit (IC) technology is towards higher speeds and densities. The total capacitive load associated with the internal circuitry is increasing in both current and next generation VLSI circuits [1], [2]. As the operating frequency increases, the average on-chip current required to charge (and discharge) these capacitances also increases, while the time during which the current being switched decreases. Therefore, a large change in the total on-chip current occurs within a short period of time.

The primary sources of the current surges are the I/O drivers and the internal logic circuitry, particularly those gates that switch close in time to the clock edges. Because of the self-inductance of the off-chip bonding wires and the on-chip parasitic inductance inherent to the power supply rails, the fast current surges result in voltage fluctuations in the power distribution network [3]. These voltage fluctuations are called simultaneous switching noise or delta-I noise.

Most existing research on simultaneous switching noise has concentrated on the transient power noise caused by the current through the inductive bonding wires at the I/O drivers [4–6]. However, simultaneous switching noise originating from the internal circuitry is becoming an important issue in the design of very deep submicrometer (VDSM) high performance microprocessors [2], [7]. This increased importance can be attributed to fast clock rates, large on-chip switching activities, and large on-chip current, all of which are increasingly common characteristics of a VDSM synchronous integrated circuit.

For example, at gigahertz operating frequencies and high integration densities, power dissipation densities are expected to approach 20 W/cm^2 [1], [8], a power density limit for an air-cooled packaged device. Such a power density is equivalent to 16.67 amperes of current for a 1.2 V power supply in a 0.1 μm CMOS technology. Assuming that the current is uniformly distributed along a 1 cm wide and 1 μm thick Al-Cu interconnect plane, the average current density is approximately 1.67 mA/μm^2. For a standard mesh structured power distribution network, the current density is even greater than 1.67 mA/μm^2. For a 1 mm long power buss line with a parasitic inductance of 2 nH/cm [9], if the edge rate of the current signal is on the order of an overly conservative nanosecond, the amplitude of the $L\,di/dt$ noise is approximately 0.35 volts. This peak noise is not insignificant in VDSM CMOS circuits.

Therefore, on-chip simultaneous switching noise has become an important issue in VDSM integrated circuits. On-chip simultaneous switching noise affects the signal delay, creating delay uncertainty since the power supply level temporally changes the local drive current [10]. Furthermore, logic malfunctions may be created and excess power may be dissipated due to faulty switching if the power supply fluctuations are sufficiently large [11], [12]. On-chip simultaneous switching noise must therefore be controlled or minimized in high performance integrated circuits.

An analytical expression characterizing the on-chip SSN voltage is presented here based on a lumped RLC model characterizing the on-chip power supply rails rather than a single inductor to model a bonding wire. The SSN voltage predicted by the analytical expression is compared to SPICE. The waveforms describing the SSN voltage are quite close to the waveforms obtained from SPICE simulations. The peak value of the SSN is within 10% of SPICE.

An analytical expression characterizing on-chip simultaneous switching noise voltage is described in Section II. A comparison of the analytical estimate with SPICE simulations is presented in Section III followed by some concluding remarks in Section IV.

II. Simultaneous Switching Noise Voltage

The power supply in high complexity CMOS circuits should provide sufficient current to support the average power and peak power demand within all parts of an integrated circuit. An inductive, capacitive, and resistive model is used in this analysis to characterize the power supply rails when a transient current is generated by simultaneous switching of on-chip registers and logic gates within a synchronous CMOS integrated circuit. The short-channel MOS transistors are modeled as nonlinear devices and characterized by the nth power law I-V model, which is more accurate than the alpha power law model in both the linear region and the saturation region [13].

A CMOS logic gate in this discussion is modeled as a CMOS inverter. The power supply rail is characterized by a lumped RLC model. The current through the PMOS transistor with a rising input signal, *i.e.*, the short-circuit current, is neglected in this discussion when determining the simultaneous switching noise voltage on a ground rail based on an assumption of a fast ramp input signal [14]. The equivalent circuit depicted in Fig. 1 is used to characterize the simultaneous switching noise voltage on the power supply rails. $L_{V_{ss}}$, $C_{V_{ss}}$, and $R_{V_{ss}}$ are the parasitic inductance, capacitance, and resistance of the ground rail, respectively. The input signal is shaped as a ramp,

$$V_{in} = \frac{t}{\tau_r} V_{dd} \quad \text{for} \quad 0 \leq t \leq \tau_r. \tag{1}$$

After the input voltage reaches V_{TN}, the NMOS transistor turns ON and begins to operate in the saturation region. It is assumed that the NMOS transistor remains in the saturation region before the input signal transition is completed.

The current through the NMOS transistor (I_N), the parasitic inductance (I_L), and the simultaneous switching noise voltage

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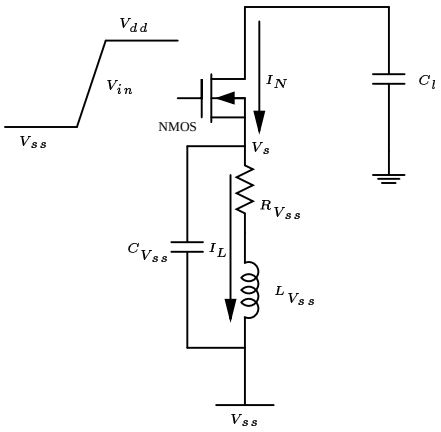

Fig. 1. Simultaneous switching noise within a ground rail.

(V_s) are given, respectively, as

$$I_N = B_n(V_{in} - V_{TN} - V_s)^n, \tag{2}$$

$$I_L = I_N - C_{V_{ss}}\frac{dV_s}{dt}, \tag{3}$$

$$V_s = R_{V_{ss}} I_L + L_{V_{ss}}\frac{dI_L}{dt}. \tag{4}$$

Assuming that the magnitude of V_s is small as compared to $V_{in} - V_{TN}$, I_N can be approximated as

$$I_N \approx B_n(V_{in} - V_{TN})^n - \frac{dI_N}{dV_{GS}}V_s. \tag{5}$$

From (5),

$$f_1 = \frac{dI_N}{dV_{GS}} = nB_n(V_{in} - V_{TN} - V_s)^{n-1}. \tag{6}$$

f_1 is a function of V_{GS} (V_{in} for the case of an inverter). In order to simplify the derivation, f_1 is approximated using V_{in} equal to $0.5\,V_{dd}$.

Combining (4), (5), and (6),

$$L_{V_{ss}}C_{V_{ss}}\frac{d^2V_s}{dt^2} + (R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_1)\frac{dV_s}{dt} + (R_{V_{ss}}f_1 + 1)V_s = R_{V_{ss}}B_n(V_{in} - V_{TN})^n + L_{V_{ss}}\frac{d}{dt}[B_n(V_{in} - V_{TN})^n]. \tag{7}$$

The first term on the left hand side of (7) is neglected since the remaining two terms on the left hand side of (7) dominate the expression.

$$(R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_1)\frac{dV_s}{dt} + (R_{V_{ss}}f_1 + 1)V_s \cong R_{V_{ss}}B_nV_{dd}^n(\frac{t}{\tau_r} - \nu_n)^n + \frac{L_{V_{ss}}B_nV_{dd}^n}{\tau_r}(\frac{t}{\tau_r} - \nu_n)^{n-1}, \tag{8}$$

where $\nu_n = \frac{V_{TN}}{V_{dd}}$. No closed form solution of this differential equation exists due to the non-integer value of n and $n-1$. In order to derive an analytical expression for the differential equation, $(\frac{t}{\tau_r} - \nu_n)^n$ and $(\frac{t}{\tau_r} - \nu_n)^{n-1}$ are approximated by a polynomial expansion to the fifth order, where the average error is less than 3%,

$$\xi^n \approx a_0 + a_1\xi + a_2\xi^2 + a_3\xi^3 + a_4\xi^4 + a_5\xi^5,$$
$$\xi^{n-1} \approx b_0 + b_1\xi + b_2\xi^2 + b_3\xi^3 + b_4\xi^4 + b_5\xi^5, \tag{9}$$

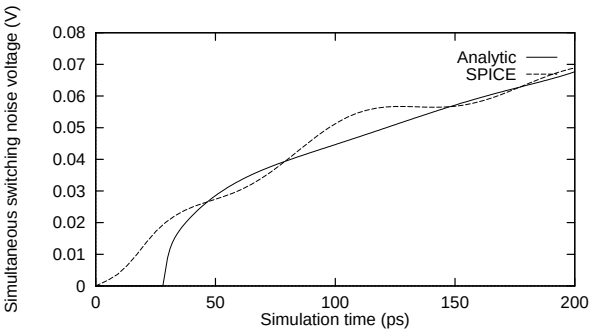

Fig. 2. Simultaneous switching noise voltage on the ground rail for a single switching logic gate with $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1$ pF, $\tau_n = 29$ ps, and $\tau_r = 200$ ps.

where $\xi = \frac{t}{\tau_r} - \nu_n$. Note that a_i and b_i for $i = 0 \ldots 5$ are independent of the input transition time τ_r. The solution of the simultaneous switching noise voltage is

$$V_s = c_0(1 - e^{-\frac{t-\tau_n}{\gamma\tau_r}}) + c_1\xi + c_2\xi^2 + c_3\xi^3 + c_4\xi^4 + c_5\xi^5, \tag{10}$$

where

$$\gamma = \frac{R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_1}{(R_{V_{ss}}f_1 + 1)\tau_r}, \tag{11}$$

$$\tau_n = \frac{V_{TN}}{V_{dd}}\tau_r = \nu_n\tau_r. \tag{12}$$

These coefficients are

$$\begin{aligned} c_0 &= A_0\gamma - A_1\gamma^2 + 2A_2\gamma^3 - 6A_3\gamma^4 + 24A_4\gamma^5 - 120A_5\gamma^6,\\ c_1 &= A_1\gamma - 2A_2\gamma^2 + 6A_3\gamma^3 - 24A_4\gamma^4 + 120A_5\gamma^5,\\ c_2 &= A_2\gamma - 3A_3\gamma^2 + 12A_4\gamma^3 - 60A_5\gamma^4,\\ c_3 &= A_3\gamma - 4A_4\gamma^2 + 20A_5\gamma^3,\\ c_4 &= A_4\gamma - 5A_5\gamma^2,\\ c_5 &= A_5\gamma. \end{aligned} \tag{13}$$

The A_i for $i = 0 \ldots 5$ are

$$A_i = \frac{R_{V_{ss}}B_nV_{dd}^n\tau_r}{R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_1}a_i + \frac{L_{V_{ss}}B_nV_{dd}^n}{R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_1}b_i, \tag{14}$$

where a_i and b_i are defined in (9). The simultaneous switching noise voltage reaches a maximum when the input voltage completes the transition, *i.e.*, $t = \tau_r$.

$$V_{s,max} = c_0(1 - e^{-\frac{\tau_r - \tau_n}{\gamma\tau_r}}) + c_1\xi_r + c_2\xi_r^2 + c_3\xi_r^3 + c_4\xi_r^4 + c_5\xi_r^5, \tag{15}$$

where $\xi_r = 1 - \nu_n$.

III. Comparison with SPICE

The simultaneous switching noise voltage on a ground rail as predicted by (10) is compared to SPICE in Fig. 2 for a single CMOS inverter with $W_n = 3.6\,\mu$m, $W_p = 7.2\,\mu$m, and $C_l = 1$ pF based on a $0.5\,\mu$m CMOS technology. The solid line represents the analytical prediction and the dashed line represents the results from SPICE simulations. During the time period from τ_n

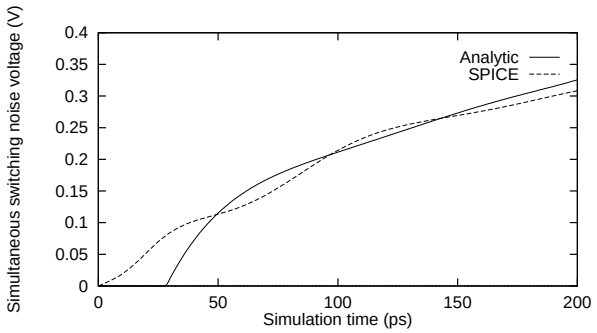

Fig. 3. Simultaneous switching noise voltage on a ground rail for five simultaneously switching logic gates with $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1$ pF, $\tau_n = 29$ ps, and $\tau_r = 200$ ps.

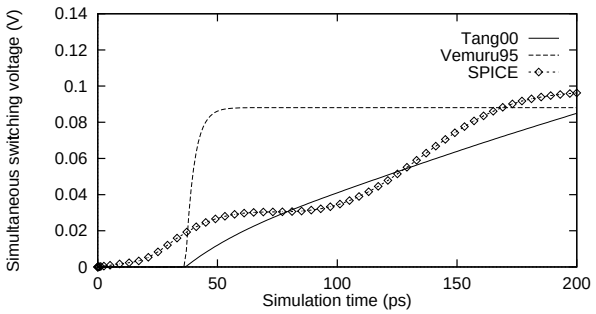

Fig. 4. The simultaneous switching voltage on a power rail with $L_{V_{dd}} = 2$ nH, $R_{V_{dd}} = 5\,\Omega$, $C_{V_{dd}} = 0.2$ pF, $\tau_p = 39$ ps, and $\tau_r = 200$ ps.

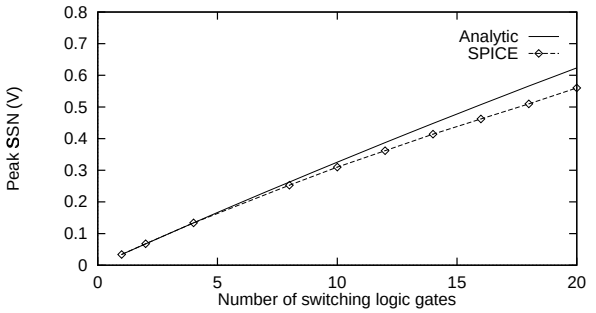

Fig. 5. The peak value of the simultaneous switching noise voltage with $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1$ pF, and $\tau_r = 200$ ps.

to τ_r, the analytical result agrees quite closely with SPICE (the error is less than 10%).

If m simultaneously switching logic gates (or inverters) are connected to the same ground rail, the total simultaneous switching noise voltage can be obtained by substituting mB_n for B_n in (11) and (14). Note that all c_i for $i = 0 \ldots 5$ are proportional to m, $\frac{1}{\tau_r}$, and B_n. Therefore, the simultaneous switching noise voltage increases with the number of simultaneous switching logic gates m, the input slew rate $\frac{1}{\tau_r}$, and the drive current of the logic gates B_n.

The analytical prediction of the simultaneous switching noise voltage for five simultaneously switching CMOS inverters with $W_n = 3.6\,\mu$m, $W_p = 7.2\,\mu$m, and $C_l = 1$ pF is compared to SPICE in Fig. 3, exhibiting less than 7% error. During the time interval from τ_n to τ_r, the analytical expression is shown to accurately model the results from SPICE simulations.

Similarly, the analytical expression for the simultaneous switching noise voltage on the power rail can be derived based on this same procedure. An estimate of the simultaneous switching noise voltage on the power rail based on the model presented in [5] is less accurate because an assumption that n is close to one ($1 \leq n \leq 1.2$) is made. This assumption is appropriate for short-channel NMOS transistors, but the value of n in a short-channel PMOS transistor is higher, typically in the range of 1.5 to 1.8 (it is 1.68 in the target $0.5\,\mu$m CMOS technology).

A comparison of the simultaneous switching noise voltage on the power rail is shown in Fig. 4. The effect of the carrier velocity saturation on a PMOS transistor is small as compared to an NMOS transistor. Therefore, a prediction based on the model presented by Vemuru in [5] cannot approximate the SSN voltage waveform shape on the power rail as shown in Fig. 4 (although the peak voltage is accurately estimated in [5]). Note that the analytical expression presented here (Tang00) accurately predicts the SSN waveform on the power rails.

The peak value of the SSN as compared to SPICE is shown in Fig. 5 with $W_n = 1.8\,\mu$m, $W_p = 3.6\,\mu$m, and $C_l = 1.0$ pF. The dashed line represents the peak value of the predicted SSN based on the analytical expression described by (15). The dotted line describes the results derived from the SPICE simulations. The accuracy of the analytical prediction is within 10% as compared to SPICE. The peak SSN voltage based on (15) is compared to SPICE for different conditions, as illustrated in Tables I and II for both the ground and V_{dd} rails, respectively, with $W_n = 1.8\,\mu$m, $W_p = 3.6\,\mu$m, and the input transition time $\tau_r = 200$ ps. Note that the maximum error of the analytical expression is within 10%.

IV. Conclusions

An analytical expression characterizing the simultaneous switching noise voltage in VDSM CMOS circuits is presented here. This expression provides a method for evaluating the simultaneous switching noise voltage at the system level. The analytically derived waveform characterizing the on-chip simultaneous switching noise voltage is quite close to SPICE. The predicted peak on-chip simultaneous switching noise voltage is within 10% as compared to SPICE.

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TABLE I

COMPARISON OF PEAK SIMULTANEOUS SWITCHING NOISE VOLTAGE ON THE V_{ss} RAIL, NUM IS THE NUMBER OF SIMULTANEOUSLY SWITCHING LOGIC GATES

Power Rail			Number of switching logic gates								
R	L	C	Peak SSN (V) (Num=5)			Peak SSN (V) (Num=10)			Peak SSN (V) (Num=15)		
(Ω)	(nH)	(pF)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)
2.0	1.0	0.1	0.0802	0.0762	5.2	0.159	0.150	6.0	0.236	0.218	8.2
		0.2	0.0802	0.0806	0.5	0.159	0.152	4.6	0.236	0.219	7.7
		0.3	0.0801	0.0790	0.3	0.159	0.151	5.3	0.235	0.217	8.2
	2.0	0.1	0.143	0.141	1.4	0.282	0.265	6.4	0.417	0.381	9.4
		0.2	0.143	0.137	4.3	0.282	0.263	7.2	0.417	0.380	9.7
		0.3	0.142	0.138	2.9	0.281	0.260	8.0	0.415	0.378	9.8
	4.0	0.1	0.267	0.256	4.3	0.522	0.490	6.5	0.760	0.697	9.0
		0.2	0.267	0.252	5.9	0.522	0.500	4.4	0.766	0.710	3.6
		0.3	0.267	0.286	6.6	0.521	0.530	1.7	0.765	0.742	3.5
5.0	1.0	0.1	0.104	0.102	1.9	0.206	0.197	4.6	0.300	0.284	5.6
		0.2	0.104	0.106	1.8	0.206	0.199	3.5	0.300	0.283	6.0
		0.3	0.104	0.104	0.0	0.206	0.198	4.0	0.300	0.282	6.3
	2.0	0.1	0.167	0.165	1.2	0.320	0.310	3.2	0.470	0.438	7.3
		0.2	0.167	0.162	3.1	0.320	0.308	3.9	0.470	0.436	7.7
		0.3	0.166	0.153	8.5	0.319	0.302	5.6	0.469	0.434	8.0
	4.0	0.1	0.288	0.278	3.6	0.560	0.526	6.4	0.810	0.750	8.0
		0.2	0.288	0.281	2.5	0.560	0.534	4.8	0.810	0.752	7.7
		0.3	0.287	0.308	6.5	0.559	0.567	0.1	0.810	0.790	2.5
Maximum error (%)			8.5			8.0			9.8		
Average error (%)			3.4			4.7			7.1		

TABLE II

COMPARISON OF PEAK SIMULTANEOUS SWITCHING NOISE VOLTAGE ON THE V_{dd} RAIL, NUM IS THE NUMBER OF SIMULTANEOUSLY SWITCHING LOGIC GATES

Power Rail			Number of switching logic gates								
R	L	C	Peak SSN (V) (Num=5)			Peak SSN (V) (Num=10)			Peak SSN (V) (Num=15)		
(Ω)	(nH)	(pF)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)	Analytic	SPICE	δ (%)
2.0	1.0	0.1	4.890	4.89	0.0	4.778	4.78	0.0	4.672	4.68	0.1
		0.2	4.890	4.89	0.0	4.778	4.79	0.1	4.670	4.68	0.1
		0.3	4.890	4.89	0.0	4.776	4.79	0.1	4.670	4.67	0.0
	2.0	0.1	4.794	4.81	0.3	4.599	4.63	0.6	4.412	4.47	1.3
		0.2	4.793	4.79	0.1	4.598	4.61	0.4	4.412	4.47	1.3
		0.3	4.794	4.79	0.1	4.600	4.61	0.1	4.410	4.46	1.3
	4.0	0.1	4.604	4.62	0.3	4.261	4.35	2.0	3.995	4.14	3.6
		0.2	4.604	4.63	0.4	4.260	4.36	2.0	3.994	4.13	3.6
		0.3	4.603	4.62	0.3	4.262	4.34	2.1	3.990	4.13	3.5
5.0	1.0	0.1	4.861	4.86	0.0	4.728	4.73	0.2	4.601	4.62	0.4
		0.2	4.860	4.86	0.0	4.726	4.73	0.2	4.600	4.62	0.4
		0.3	4.860	4.87	0.0	4.726	4.74	0.3	4.600	4.61	0.4
	2.0	0.1	4.770	4.78	0.2	4.554	4.59	0.8	4.351	4.42	1.6
		0.2	4.771	4.78	0.2	4.552	4.59	0.8	4.350	4.41	1.5
		0.3	4.770	4.76	0.2	4.552	4.58	0.8	4.350	4.42	1.6
	4.0	0.1	4.692	4.61	1.8	4.224	4.32	2.3	3.900	4.10	9.2
		0.2	4.690	4.61	1.7	4.220	4.32	2.3	3.905	4.11	9.3
		0.3	4.690	4.60	1.7	4.220	4.31	2.1	3.905	4.12	9.3
Maximum error (%)			1.8			2.3			9.3		
Average error (%)			0.4			1.0			2.8		