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Frequency Dependent Efficiency Model of On-Chip DC-DC Buck Converters

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Abstract-**An analytic method to evaluate frequency dependent losses in on-chip DC-DC buck converters is presented in this paper. These converters feature high switching losses caused by the skin effect in the package inductors. The frequency dependent air-core inductor model is shown to be critical in determining the optimal switching frequency. A general RLC parameter extraction method is also described. Considering the skin effect results in a 15% reduction in overall DC-DC converter losses. The proposed approach focuses on decreasing ripple current related losses, which are dominant in the target operating condition. Consequently, to obtain optimal efficiency, the switching frequency increases as the load current decreases. An intuitive explanation for this surprising result is that switching losses rise linearly with frequency whereas ripple losses decrease as $n^{1.5}$. A SPICE based circuit model of a DC-DC converter is applied to validate the proposed analytic method. (Abstract)**

Keywords-on chip DC-DC; frequency dependent losses buck converter efficiency; air core inductor (keywords)

I. INTRODUCTION

With the increasing attention to energy savings and battery life in mobile devices [1], microprocessors and chipsets integrate different functional blocks such as I/O, analog circuits, memory, and graphics on the same die. For power efficiency, each block may operate at a different DC supply voltage, resulting in multiple DC-DC power converters on the same printed circuit board, which occupy a growing fraction of the board area. Integrated on-die DC-DC converters may provide a solution for the PCB resource issue, enabling a larger number of different voltage supplies. Power efficiency is one of the most critical parameters of on-chip DC-DC converters. These converters require inductors which cannot be efficiently implemented on die, but can be embedded inside the package. Typically, these inductors have an air-core (no ferromagnetic materials are used), and therefore exhibit a low inductance in the range of a few nH. A buck converter needs to operate at high switching frequencies (hundreds of MHz). Existing work on analytic modeling of integrated DC-DC converter efficiency [2-5] does not properly address the combination of high switching frequencies and air-core inductor properties. Consequently, a need for considering high frequency effects, such as the skin effect, arises. Since the dominant losses are related to the ripple current (in contrast to discrete component based converters), a novel procedure for light load efficiency optimization is proposed.

The process of analytic model parameter extraction is based on simple circuit simulation and is independent of implementation details. The simulated converter supports 2 volt to 1 volt conversion, a filter inductor of 3 nH embedded in a package [6], and a switching frequency in the range of hundreds of MHz. The maximum load is targeted at 1.5 amperes.

This paper is organized as follows: A analytic linear loss model is presented in section 2 as well as a method for extracting the model parameters using SPICE simulation and a field solver. Switching frequency optimization is presented in section 3. Optimization of efficiency under light load conditions by area scaling and frequency optimization is addressed in section 4. Validation of the analytic results by simulation is also presented in section 4. The paper is concluded in section 5.

II. ON-CHIP DC-DC LOSS MODEL

A. *Analytic Efficiency Model*

The efficiency of a DC-DC converter is

$$\eta = \frac{P_{out}}{P_{loss} + P_{out}} = \frac{I_{load} V_{out}}{P_{fet} + P_{ind} + I_{load} V_{out}}. \quad (1)$$

The losses are within the power FET and inductor. The major power FET losses are $C_b V_{in}^2 f_{sw}$ switching losses within the pulse width modulator (PWM) where C_b is the effective switching capacitance and $I^2 R_{ds}$ losses due to the current in the transistors. The power dissipation in the inductor is primarily due to $I^2 R(f)$ losses. $R(f)$ is the frequency dependent inductor resistance, in which the DC component is denoted by R_i. The current in the power path

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of the converter is a superposition of the triangular ripple current ΔI and DC load current I_{load}. Equations (2) and (3) describe the losses in the power FET and the inductor, respectively,

$$P_{fet} = \underbrace{C_b V_{in}^{\ 2} f_{sw}}_{P_{cvf}} + R_{ds}\left(I_{load}^{\ 2} + \frac{\Delta I^2}{12}\right), \quad (2)$$

$$P_{ind} = R(f)\left(I_{load}^{\ 2} + \frac{\Delta I^2}{12}\right). \quad (3)$$

Combining these two expressions with respect to the load and ripple current,

$$P_{ripple} = \frac{\Delta I^2}{12}\left(R_{ds} + R(f)\right), \quad (4)$$

$$P_{load} = I_{load}^{\ 2}\left(R_i + R_{ds}\right). \quad (5)$$

The losses are composed of two parts: P_{cvf} together with P_{ripple}, which is independent of the load current and P_{load} which is a function of the load current. The efficiency of a DC-DC buck converter can be rewritten as

$$\eta = \frac{I_{load} V_{out}}{P_{cvf} + P_{ripple} + P_{load} + I_{load} V_{out}}. \quad (6)$$

With these expressions, the individual losses of a DC-DC converter can be investigated. The following section describes a method to obtain the analytic parameters from an initial circuit design.

B. Circuit-level Efficiency Model

The losses are modeled using a DC-DC converter scheme shown in Fig. 1. The power FETs are modeled as ideal switches, resistors R_{ds}, and switching capacitance C_b. The inductor is modeled as an ideal inductor with a frequency dependent effective series resistance (ESR) $R(f)$. L_{ac} represents the high frequency limit of the inductance.

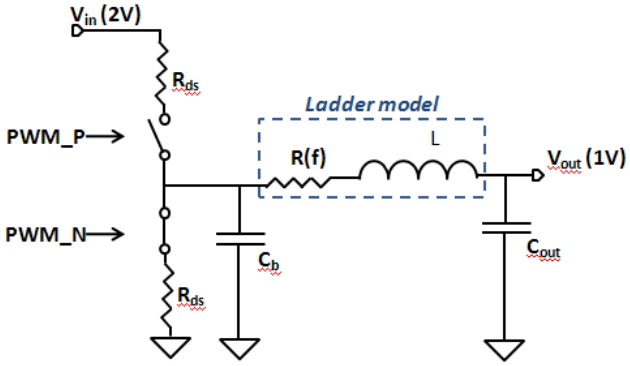

Figure 1: Frequency dependent losses model of a DC-DC converter

The output capacitor losses are neglected due to the low ESR of the capacitor (not shown in Fig. 1). Additional losses such as the power dissipated by the control compensation filter, package, inductor eddy currents, leakage, and die power grid are neglected as these components are small as compared to the aforementioned losses.

C. Circuit Model Parameter Extraction

The procedure for extracting the switching capacitance C_b assumes that the dissipated power is described by $C_b V_{in}^{\ 2} f_{sw}$ plus a constant. The simulation setup for extracting C_b, which uses a power stage, is shown in Fig 2. In this simulation, the input voltage V_{in} is constant (2 volts) and the switching frequency is swept around the projected value, 150 MHz. C_b is extracted from the slope of Fig. 3. This definition of C_b guarantees that all switching and I-V overlap losses are considered. This extraction method is independent of a power stage design. The physical properties of C_b are discussed in [3, 4].

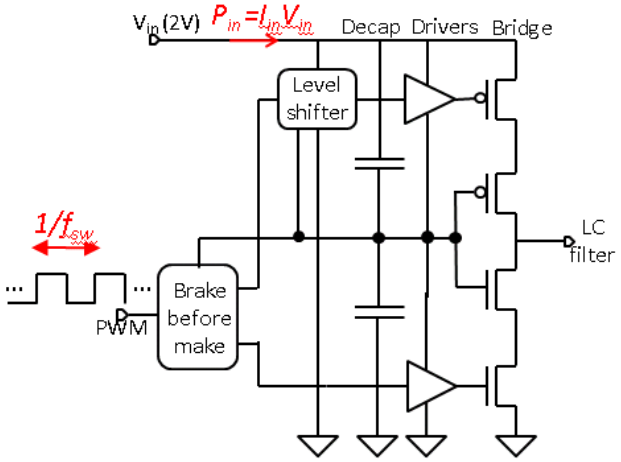

Figure 2: Simulation setup for extraction of bridge capacitance

The resistance R_{ds} of the drivers can be extracted from an I-V simulation of the bridges (the right most transistors of the power stage as shown in Fig. 2). A standard cascode topology is used [3] to avoid high voltage overstress, which is also captured in C_b and R_{ds}. The PMOS and NMOS widths are assumed to be equal.

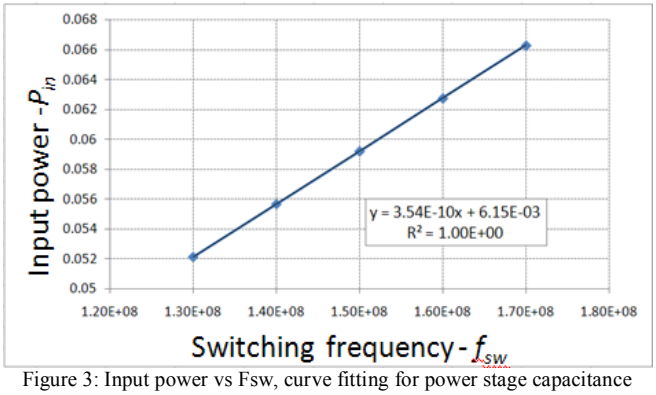

Figure 3: Input power vs Fsw, curve fitting for power stage capacitance

Equation (4) describes the ripple current related losses both in the driver and the inductor. Previous work ignored the skin effect in the inductor [7] or assumed a constant R_{ac} [8]. In this paper, the skin effect is modeled as a frequency dependent resistance,

$$R(f) = R_i + R_{ac}\sqrt{\frac{f}{f_0}}. \quad (7)$$

The air-core package embedded inductor structure is described in the Ansoft Q3D field solver. R_i, R_{ac}, and L_{ac} are extracted where f_o is chosen within the range of the projected switching frequency. The frequency dependent resistance of the air-core inductor is shown in Fig. 4. The resistance at 150 MHz is 150 mΩ while R_i at DC is only 25 mΩ. This dramatic difference results in the skin effect being the dominant factor in the inductor resistance. Note in Fig. 4 that using R_{ac} to describe the skin effect may not be sufficiently accurate. An *RL* multi-branch ladder model is therefore used [9] to capture the frequency dependence in SPICE. A fit of the analytic, Ansoft Q3D based, and *RL* ladder models is shown at Fig. 4 with a maximum error of the model of 8%.

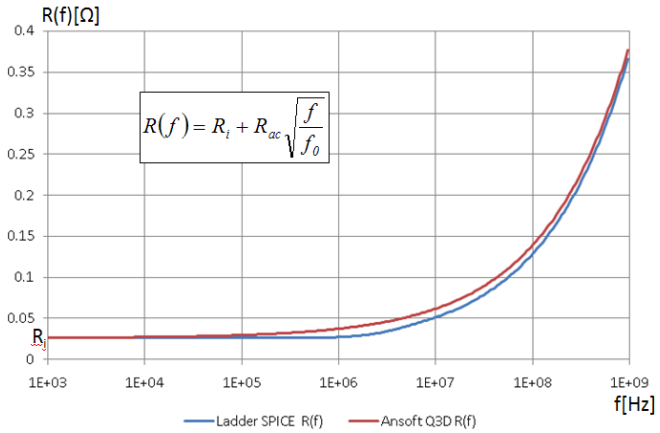

Figure 4: Frequency dependent inductor resistance, Ansoft Q3D solution and SPICE ladder circuit

III. Optimization of Switching Frequency

The switching frequency can be optimized independent of the load current using only P_{cvf} and P_{ripple} (See (2), (4), and (5)). Differentiating P_{cvf} and P_{ripple} with respect to f_{sw}, marked *f*, and equating to zero results in

$$f^3 + f^{1/2}\frac{R_{ac}A^2}{8C_bV_{in}^2\sqrt{f_0}} = \frac{A^2(R_i + R_{ds})}{6C_bV_{in}^2}, \quad (8)$$

$$A = \frac{V_{in}}{L_{ac}}\frac{V_{out}}{V_{in}}\left(1 - \frac{V_{out}}{V_{in}}\right). \quad (9)$$

Equation (8) is intractable in *f*. If the skin effect is neglected, $R_{ac} = 0$, making the solution of (8) the same as in [4],

$$f = \left(\frac{R_i + R_{ds}}{6}\frac{A^2}{V_{in}^2C_b}\right)^{1/3}. \quad (10)$$

If the switching frequency is high (hundreds of MHz), the power path resistance is dominated by the skin effect,

$$R_{ac}\sqrt{\frac{f}{f_0}} >> (R_{ds} + R_i). \quad (11)$$

In this case, the solution of (8) is

$$f = \left(\frac{R_{ac}A^2}{8C_bV_{in}^2\sqrt{f_0}}\right)^{2/5}. \quad (12)$$

In Fig. 5, a numerical solution of (8) is shown for an inductance of 3 nH. The asymptotes of P_{cvf} and P_{ripple} are also shown. The minimum loss is graphically found at approximately 120 MHz. The analytic solution without the skin effect in (10) results in the minimum loss occurring at 80 MHz. The skin effect dominated solution in (12) results in a 100 MHz optimal switching frequency. A solution that includes both effects is higher than each case since the ripple current is reduced to compensate both the DC and AC resistances. The intuitive analogy for this model is two resistors connected in parallel. The equivalent resistor is therefore always smaller than the smallest resistor. Similarly, the numerical solution is higher than each partial solution. Considering frequency dependent losses of the inductor results in a choice of optimal switching frequency that reduces losses by 15% as compared to the case where the skin effect is ignored.

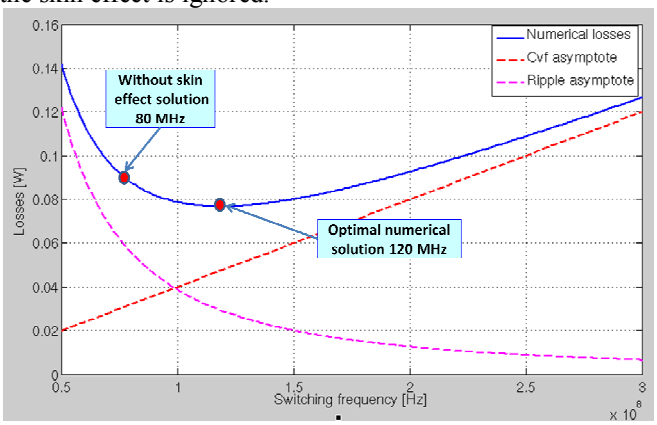

Figure 5: Frequency dependent losses vs f_{sw}

IV. Optimization for Light Load

One of the major drawbacks of switching DC-DC converters is inherent losses, *i.e.*, P_{cvf} and P_{ripple}, do not scale with the load current. Therefore, at light loads, the efficiency of the converter significantly drops and may fall below an acceptable range. Area scaling methods to improve the efficiency at light loads are proposed in [4] and [10]. Modern integrated circuits, such as microprocessors or chipsets, exhibit high dynamic range of the load current from 50 mA to 1.5 A, so optimization for light loads is critical.

A known method to increase efficiency at light loads is to scale the area of the bridge transistors. The area scaling parameter r is defined as the ratio of the active bridge width to the total width. The optimal width for a given load current can be derived from [10] and decreases linearly with smaller load currents. Area scaling is performed by disabling portions of the power stage. In [4], the switching frequency remains constant when area scaling is performed. Based on the switching frequency optimization method illustrated in Fig. 5, the optimal switching frequency is recalculated for each r between 0 and 1. This procedure results in an increased switching frequency within a smaller area, as depicted in Fig. 6. An intuitive explanation for this surprising result is that P_{cvf} rises linearly with frequency

whereas P_{ripple} decreases as $n^{1.5}$ and the losses are heavily dominated by P_{ripple}. This effect occurs despite the additional resistance due to the skin effect with rising switching frequency. The optimal frequency increases while maintaining a balance between the two types of losses.

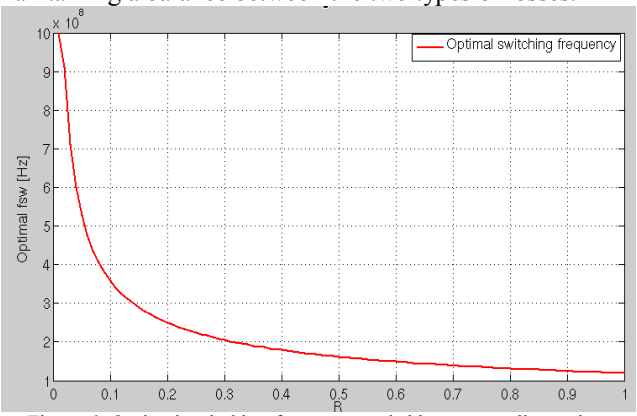

Figure 6: Optimal switching frequency vs bridge area scaling ratio r

The effect of this rise in overall efficiency is dramatic. For example, when the bridge area is scaled to one tenth of the maximum size (r = 0.1), the efficiency improves by 25% (from 60% to 85%) while the switching frequency rises from 120 MHz to 350 MHz, as shown in Figs. 6 and 7. Most of this improvement is achieved due to increasing the switching frequency.

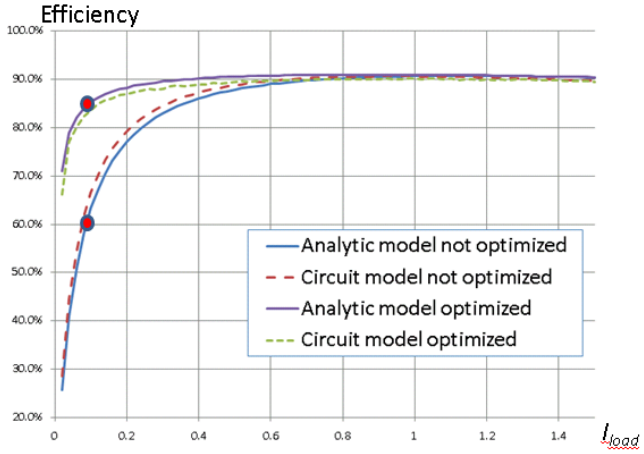

Figure 7: Optimized and non-optimized simulated vs analytic efficiency

SPICE simulation is used to characterize the DC-DC converter architecture [7] and to verify the analytic expressions. The power stage circuit is the same as shown in Fig. 2 and the parameters are based on a modern Intel process. The input voltage is 2 volts, the output voltage is 1 volt, and the inductance is 3 nH. The output capacitance is 0.4 uF. The control scheme is described by an ideal Laplace type 3 transfer function. In order to consider the skin effect the output filter inductor is modeled using *RL* ladder. Comparison of the simulated and analytic (as described by (1)) efficiency η as a function of load current is shown in Fig. 7 with a maximum error of the model of 7%. Note that the simulation data accurately match the analytic model for both the optimized and non-optimized operating modes of the buck converter.

V. Conclusions

A frequency dependent analytic model for the power losses in an on-chip DC-DC buck converter has been developed. The converter employs a small air-core in-package inductor and features high switching frequency (hundreds of MHz). Optimization of the switching frequency considers the skin effect of the inductor.

The proposed switching frequency optimization methodology is applied together with bridge width scaling for a specific load current [10] to further improve the converter efficiency. SPICE simulations are used to validate the analytic model and to extract the model parameters.

Note that in contrast to the pulse frequency modulation technique, which focuses on decreasing P_{cvf}, the proposed approach focuses on decreasing P_{ripple}. Upcoming research task will consider other types of losses that are neglected in the present work.

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