Design Methodology to Distribute On-Chip Power in Next Generation Integrated Circuits

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***Abstract*—The performance of an integrated circuit depends strongly upon the power delivery network. With the introduction of ultra-small on-chip voltage regulators, novel design methodologies are needed to determine the location of these on-chip power supplies and decoupling capacitors. In this paper, the optimal location of the power supplies and decoupling capacitors is determined for different size and number of components. Optimization algorithms widely used for facility location problems are applied in the proposed methodology. The effect of the size, number, and location of the power supplies and decoupling capacitors on the power noise is also discussed.**

I. Introduction

Power consumption has become one of the primary design constraints with the proliferation of mobile devices as well as server farms where the performance per watt is the primary benchmark [1], [2]. The power generated and regulated by the off-chip and on-chip voltage regulators is distributed to billions of load circuits throughout a power distribution system. Due to the parasitic impedances of the power distribution networks, voltage fluctuations in the supply voltage occur. These fluctuations depend on the characteristics of the load current demand and the behavior of the power distribution network. The power supplies are also supported by locally distributed decoupling capacitors which serve as a reservoir of charge to provide current to the load circuits [3].

The complexity of the high performance power delivery systems has increased significantly with the integration of diverse technologies on a single die, forming an heterogeneous system. The required supply voltage levels and the noise constraints vary significantly for different technologies. Novel voltage regulator topologies [4]–[10] have recently been proposed, enabling not only on-chip power supply integration but also multiple on-chip point-of-load power supplies [10], [11]. These on-chip point-of-load power supplies provide the required voltage close to the load circuits, greatly reducing the effective impedance between the load circuits and power supplies [12].

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Next generation power delivery networks for heterogeneous circuits will contain tens to hundreds of on-chip power supplies supported by thousands of on-chip decoupling capacitors to satisfy the current demand of billions of load circuits. The design of these complex systems would be enhanced if available resources such as the physical area, number of metal layers, and power budget were not severely limited. The continuous demand over the past decade for greater functionality within a small form factor has imposed tight resource constraints while achieving aggressive performance and noise targets [13].

Several techniques have been proposed for efficient power delivery systems, typically focusing on optimizing the power network [13], [14] and the placement of the decoupling capacitor [15], [16]. Recently, Zeng *et al.* [17] proposed an optimization technique for designing power networks with multiple on-chip voltage regulators. The design tradeoffs of on-chip voltage regulators and the effect of these regulators on high frequency voltage fluctuations and mid-frequency resonance have been analyzed. The interactions between the power supplies and the decoupling capacitors are, however, not considered, which can significantly affect the performance of an integrated circuit [17]. These interactions are quite critical in producing a robust power distribution network [10]. Decoupling capacitors and on-chip power supplies exhibit several distinct characteristics such as the response time, area requirements, and parasitic output impedance. Circuit models for these components should accurately capture these characteristics while being sufficiently simple to not overly complicate the optimization process.

In this paper, facility location optimization algorithms will be analyzed to determine the location, size, and number of power supplies and decoupling capacitors for different constraints [18]–[20]. The constraints of this power network co-design problem depend on the application and specifications of the performance objectives. The optimization goal can be to minimize the maximum voltage drop, average voltage drop, total area, response time for particular circuit blocks, or total power consumption. Multiple optimization goals can also be applied for smaller or mid-size integrated circuits.

The rest of the paper is organized as follows. A recently developed point-of-load voltage regulator is briefly described in Section II. The facility location problem is introduced

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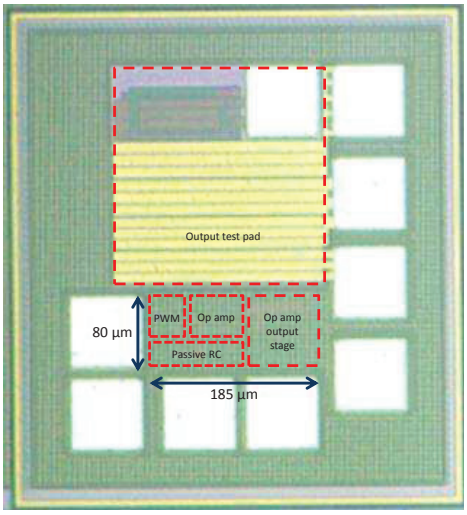

Fig. 1. Microphotograph of the hybrid voltage regulator [8].

with some exemplary applications in Section III. A proposed methodology to determine the optimum location of the power supplies and decoupling capacitors is described in Section IV. The optimum location of the power supplies and decoupling capacitors, determined for a sample circuit, is presented in Section V. The paper is concluded in Section VI.

II. Point-of-Load Voltage Regulators

Placing multiple point-of-load power supplies is challenging since the area occupied by a single power supply should be small and the efficiency sufficiently high. Guo *et al.* proposed an output capacitorless low-dropout regulator which occupies 0.019 mm^2 on-chip area [6]. The authors also recently proposed a hybrid point-of-load voltage regulator, occupying 0.015 mm^2 on-chip area [8]. A microphotograph of this hybrid point-of-load regulator is shown in Fig. 1. These area efficient voltage regulators provides a means for distributing multiple local power supplies across an integrated circuit, while maintaining high current efficiency and small area. With the proposed voltage regulator, on-chip signal and power integrity is significantly enhanced while providing the capability for distributing multiple power supplies. Design methodologies are therefore required to determine the location, size, and number of these power supplies and decoupling capacitors.

III. Facility Location Problem

Every complex system is composed of small components, typically with simple structures. The interactions and aggregation of these components form a highly complex system. The efficiency of this system strongly depends upon the physical location of these components, which significantly affects the interactions. In most systems, these components can be grouped into two categories; (1) facilities, and (2) customers. The location, size, and number of facilities that minimize the cost of providing a high quality service to the customers are the design objectives [18].

Mathematical models of the location have been used to determine the optimal number, location, and size of the facilities as well as allocate facility resources to the customers that minimize or maximize the objective function [18]–[20]. The problem can be categorized depending upon the network (discrete or continuous) and the input (static or dynamic). The objective is to minimize the average (or maximum) distance from the facilities to the customers, determine the minimum number of facilities that serve a particular number of customers at fixed locations, or maximize the minimum distance from a facility to the customers.

The design of on-chip power delivery networks for heterogeneous circuits exhibits significant similarities to the design of electrical distribution networks in larger scale systems, such as the electric power distribution grid of a city. The electricity generated at a power plant is downconverted and distributed to substation transformers, typically outside a city. The output voltage of these substation transformers is further downconverted and regulated by the local power supplies. This voltage can be either delivered to industrial customers at a high voltage level or further downconverted and regulated at smaller substations and distributed to the local city power grid. Large capacitors are integrated within this electrical distribution system to reduce voltage fluctuations. Alternatively, in an heterogeneous integrated circuit, the on-board voltage regulators downconvert the output voltage of the board level power supply unit. This voltage is delivered to the on-chip voltage regulators or directly to the on-chip power grid which provides current to the load circuits. The required voltage levels and noise constraints are technology and design dependent. The on-chip power delivery system is designed to deliver different voltage levels within noise constraints. Decoupling capacitors are distributed throughout the on-chip power delivery network to support the power distribution system. A parallel can be drawn between the transformers and off-chip voltage regulators, the small substations and on-chip voltage regulators, and the large capacitors and on-chip decoupling capacitors. Additionally, the voltage requirements of different technologies within an heterogeneous integrated circuit vary in a similar manner as the voltage requirements of industrial and residential regions within a city.

Several optimization algorithms have been proposed which consider possible constraints to provide an optimal solution to this problem. Due to the similarity between the electrical distribution network of a city and the power distribution network of a heterogeneous circuit, analogous algorithms can be applied to the design of these systems. Since facility location algorithms are widely used to design electrical distribution networks, these city planning algorithms are leveraged in designing on-chip power networks within heterogeneous circuits.

IV. Proposed Optimization Methodology

These existing optimization techniques and methodologies provide a near optimal solution for the location of the on-chip power supplies and decoupling capacitors that minimize the average (or maximum) power noise. The focus of this paper is to determine the optimal number and location of

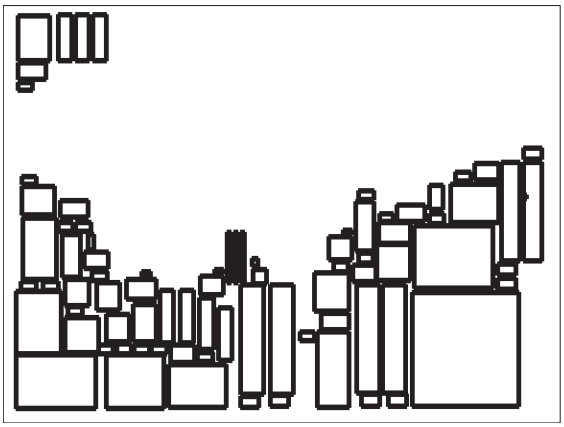

Fig. 2. Floorplan of benchmark circuit, superblue18. To reduce the complexity of the problem, only the large blocks (a total of 83 blocks), which occupy more than 95% of the total active area, are considered.

the on-chip power supplies and decoupling capacitors that minimize the average power noise. A closed-form model of the impedance, proposed in [12], is utilized to determine the effective resistance from the power supplies and decoupling capacitors to the load circuits. The constraints of the problem are as follows,

- The total area of the power supplies and decoupling capacitors is maintained constant
- All power supplies must be larger than the minimum sized power supply
- All decoupling capacitors must be larger than the minimum sized decoupling capacitor

An objective function $F(n, m, k)$ is proposed that reduces the power noise from the parasitic impedance between a power source and load circuit [2]. $F(n, m, k)$ characterizes the sum of the weighted effective resistance from the power supplies and decoupling capacitors to the load as follows,

$$Objective function = \sum_{j=1}^{m}\sum_{i=1}^{n} w_{L_j} C_{P_{ij}} R_{eff}(P_i, L_j) + \sum_{j=1}^{m}\sum_{i=1}^{k} w_{L_j} C_{D_{ij}} R_{eff}(D_i, L_j), \quad (1)$$

where P_i, L_j, and D_i are, respectively, the i^{th} power supply, j^{th} load block, and i^{th} decoupling capacitor. $R_{eff}(P_i, L_j)$ is the effective resistance between the i^{th} power supply and j^{th} current block. The parameters n, m, and k, are, respectively, the total number of power supplies, load blocks, and decoupling capacitors within a circuit. w_{L_j} is a weighting parameter for the j^{th} circuit block and is proportional to the size of the circuit block. Intuitively, these parameters are used in the model to place the power supplies and decoupling capacitors close to those circuit blocks with greater current demand. $C_{P_{ij}}$ and $C_{D_{ij}}$ are, respectively, the contribution of the i^{th} power supply and i^{th} decoupling capacitor to the j^{th} circuit block. The ratio of the current contribution from each individual power supply and decoupling capacitor to the total current consumption of the j^{th} circuit block is, respectively,

$$C_{P_{ij}} = \frac{1/(R_{eff}(P_i, L_j))}{\sum_{i=1}^{n} 1/(R_{eff}(P_i, L_j)) + \sum_{i=1}^{k} 1/(K * R_{eff}(D_i, L_j))}, \quad (2)$$

and

$$C_{D_{ij}} = \frac{1/(K * R_{eff}(D_i, L_j))}{\sum_{i=1}^{n} 1/(R_{eff}(P_i, L_j)) + \sum_{i=1}^{k} 1/(K * R_{eff}(D_i, L_j))}, \quad (3)$$

where K is the ratio that characterizes the response time of the decoupling capacitor as compared to the response time of the power supply. The total contribution of current from the power supplies and decoupling capacitors to a particular circuit block, in this case the j^{th} circuit block, is equal to one,

$$\sum_{i=1}^{n} C_{P_{ij}} + \sum_{i=1}^{k} C_{D_{ij}} = 1. \quad (4)$$

K is a design and technology dependent parameter that depends upon the operating frequency, slew rate of the circuit blocks, output impedance of the power supplies, and effective series resistance (ESR) of the decoupling capacitors. In heterogeneous systems, where the slew rate, operating frequency, and supply voltage vary significantly over different portions of a circuit, K provides the flexibility to optimize the power distribution system for different technologies. Without loss of generality, K is set equal to ten, which assumes that the power supplies are ten times larger than the decoupling capacitors.

TABLE I
ISPD BENCHMARK CIRCUIT: SUPERBLUE18

# of blocks	Reduced # of blocks	Power grid size	# of nodes in the power grid
41,047	83	381 X 404	153,924

V. CASE STUDY

The optimal location of the power supplies and decoupling capacitors for one of the ISPD'11 placement benchmark suite circuits, superblue18, is evaluated by the proposed power delivery co-design methodology for different number of power supplies and decoupling capacitors [21]. The circuit floorplan of superblue18 is illustrated in Fig. 2.

41,047 individual circuit blocks exist in superblue18. 83 individual blocks occupy more than 95% of the total area covered by all of the circuit blocks. To reduce the complexity of the proposed optimization problem, these 83 circuit blocks are considered in the proposed co-design methodology. The properties of superblue18 are listed in Table I.

The power distribution network of superblue18 consists of 381 vertical and 404 horizontal metal lines. Each circuit block is modeled as a single current load where the maximum current is proportional to the size of the circuit block. Each current load representing a circuit block is connected to the power grid from the node which is physically closest to the center of that particular circuit block.

TABLE II
OPTIMUM LOCATION OF POWER SUPPLIES AND DECOUPLING CAPACITORS THAT MINIMIZE THE AVERAGE VOLTAGE DROP FOR SUPERBLUE18.

# of power supplies	# decoupling capacitors	Power supply location (x,y)	Decoupling capacitor location (x,y)
1	1	(207,44)	(105,67)
1	10	(347,15)	(112,48), (1,2), (1,2), (147,51), (2,1), (2,1), (1,2), (1,2), (2,2), (2,2)
3	5	(163,15), (285,3), (133,59)	(113,48), (133,59), (104,66), (65,67), (65,2)
5	10	(148,51), (1,2), (65,2), (184,16), (165,15)	(1,2), (1,2), (1,2), (1,2) (1,2), (2,2), (2,2) (2,1), (2,1), (2,1)

The general algebraic modeling system (GAMS) is used as the optimization tool [22]. The proposed optimization methodology is modeled as a mixed integer nonlinear programming problem. The location of the power supplies and decoupling capacitors that minimizes the objective function is determined for different number of power supplies and decoupling capacitors. These results are listed in Table II. The total area of the power supplies and decoupling capacitors is maintained the same for all of the test cases to provide a fair comparison.

The optimal locations are physically far from each other to minimize the objective function when there is a single power supply and decoupling capacitor within the power distribution network. When the number of decoupling capacitors increases, the optimal location for different capacitors can be at the same node, as listed in Table II. The optimal location of the power supplies is, however, scattered throughout the power grid even for multiple power supply systems. The reason for this behavior is that a power supply can provide sufficient current to those large circuit blocks which are spatially close to the power supply. Alternatively, decoupling capacitors cannot provide sufficient current to the neighboring circuit blocks, and multiple decoupling capacitors are required near the large circuit blocks to minimize the voltage drop, as listed in Table II.

VI. CONCLUSIONS

The similarity between the facility location problem and the design of heterogeneous integrated circuits is exploited. An objective function based on the effective resistance between the power supplies, decoupling capacitors, and load circuits is proposed that minimizes the average voltage drop throughout a heterogeneous integrated circuit. This objective function considers the contribution of current from different power supplies and decoupling capacitors to a circuit block as well as the size of the individual circuit blocks. The optimal location of the on-chip power supplies and decoupling capacitors is determined for an ISPD'11 benchmark suite circuit, superblue18. In a system with multiple power supplies and decoupling capacitors, the power supplies are scattered throughout the distribution network whereas the decoupling capacitors may concentrate around a large circuit block to minimize local voltage fluctuations.

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