Physical Design for Reduced Delay Uncertainty in High Performance Clock Distribution Networks

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***Abstract*—Controlling the clock signal delay in the presence of various noise sources, process parameter variations, and environmental effects represents a fundamental problem in the design of high speed synchronous circuits. A methodology for enhancing the layout of the clock tree to reduce the uncertainty of the clock signal is presented in this paper. The primary objective of the proposed methodology is to satisfy the timing constraints of the most critical data paths in a circuit. Two different design approaches are described to reduce the delay uncertainty of the clock signal. The first approach determines the size of the clock buffers to reduce variations in the clock delay. The second approach exploits the common portion among the clock paths that drive the registers of the most critical data paths. The application of these techniques to a set of benchmark circuits demonstrates some interesting tradeoffs among the aggregate clock buffer size, the total wire length of the clock tree, and the power dissipation.**

I. Introduction

The continuous quest for higher circuit performance has pushed clock frequencies deep into the gigahertz frequencies range, reducing the period of the clock signal well below a nanosecond. Accurate control over the delay and quality of the clock signal is required in order to achieve correct operation of a circuit under tight timing constraints. Deviations of the clock signal from a target delay can cause incorrect data to be latched within a register, resulting in a system malfunctioning. These deviations of the delay of a signal from a target value are described as delay uncertainty.

The important task of distributing the clock signal within an integrated circuit is performed by the clock distribution network. Due to the large number of clocked elements in a circuit and the tight timing constraints, the design of a clock distribution network represents one of the most challenging tasks in the integrated circuit design process. Reducing uncertainty in the clock signal delay is one of the primary issues in the design of a high performance clock distribution network [1].

The uncertainty of the clock signal delay is caused by a number of factors that affect a clock distribution network, examples of which include process and environmental parameter variations (PEPV) [2], [3]. The sensitivity of a clock distribution network to these variation effects has become an issue of fundamental importance to the design of high performance synchronous systems.

Significant research effort has therefore been focused on characterizing and reducing delay uncertainty. A primary research target is the statistical characterization [4] of process parameter variations and delay uncertainty in order to specify a minimum time for synchronizing high speed circuits [5]. Furthermore, design methodologies for clock distribution networks [6] have been developed to reduce uncertainty in the clock signal delay [1], [7], [8]. Additionally, noise effects due to crosstalk among interconnect lines have been investigated [9], [10].

In this paper, a methodology for reducing the uncertainty in the clock signal delay is presented. The objective of this methodology is to satisfy delay uncertainty constraints of the most critical data paths of a circuit. The primary design concepts of the proposed methodology are described in Section II. These concepts are implemented into two different design strategies, as described in Section III. The application of these design strategies to a set of benchmark circuits produces interesting tradeoffs between the power dissipated by a clock tree and the clock tree area, as demonstrated in Section IV. Finally, some conclusions are presented in Section V.

II. Design methodology concept

The most crucial effect of parameter variations on the clock signal delay is the delay uncertainty introduced between the arrival time of different clock signals at sequentially-adjacent registers connected by a combinational path. The more strict the setup and hold time constraints of a combinational data path, the more sensitive the timing of a data path is to delay uncertainty. Reducing the delay uncertainty of the critical data paths is the primary objective of the design methodology presented in this paper. This objective can be achieved by changing the size of the clock buffers along the clock paths that drive the critical registers, as described in section II-A. In addition, decreasing the non-common portion of the clock tree among those paths can also reduce the uncertainty between the clock signal arrival times, as described in section II-B.

A. Effect of clock buffer size on delay uncertainty

The strict constraints upon the delay and quality of the clock signal require the insertion of clock buffers along a clock distribution network. In addition, inserting buffers along

an interconnect line alleviates the quadratic dependence of the signal propagation delay on the line length. However, buffer insertion also introduces uncertainty in the signal delay. Variations of the device parameters affect the current flow within a buffer, thereby introducing uncertainty in the buffer delay. Furthermore, crosstalk among interconnect lines causes variations in the effective load of a buffer, introducing additional uncertainty in the signal propagation delay.

The delay of a signal propagating along a buffer depends upon the amount of current that flows from the buffer to drive an interconnect line. Device parameter variations as well as interconnect crosstalk effects are simulated using Spectre® simulator* for different buffer sizes and the results are shown in Figures 1 and 2 respectively. As shown in Figures 1 and 2, the delay uncertainty caused by these effects decreases as the size of the interconnect buffer is increased.

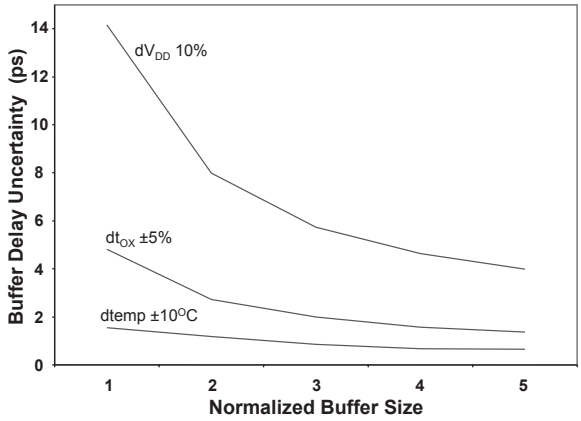

Fig. 1. Uncertainty in the inverter delay due to process, environmental, and system parameter variations

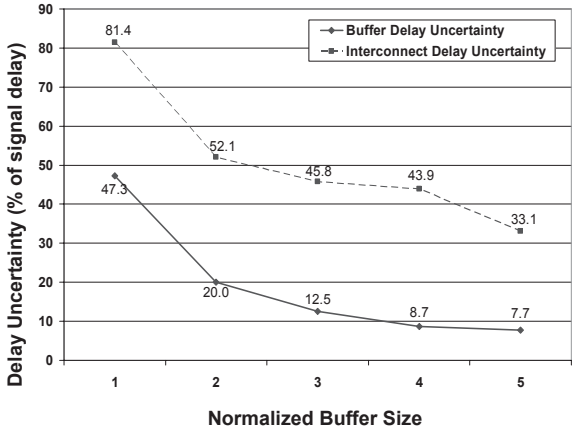

Fig. 2. Reduction in delay uncertainty due to interconnect crosstalk with increasing buffer size

B. Exploiting the common portion among clock paths

The clock signal is distributed to sequentially-adjacent registers along different paths within a clock tree. These paths share a *common part* of the clock tree from the source of the clock signal to a branch node, as shown in Figure 3. At a branch node, the paths split and the clock signal propagates along different, *non-common parts* of the tree to arrive at the individual registers. As shown in Figure 3, the effects of process and environmental parameter variations on the common part of the clock tree introduce the identical delay to those clock signals driving sequentially-adjacent registers [1]. Alternatively, along the non-common part of the clock tree, the effects of process and environmental parameter variations may introduce different clock delays and thereby cause a violation of the strict timing constraints of the critical data paths.

The topology of a clock tree that specifies the hierarchy of the branch nodes within a tree can greatly affect the delay uncertainty introduced along the clock paths [11]. In particular, as the common portion of two paths in a clock tree increases, the delay uncertainty between the leaves of these paths is likely to decrease. The common portion of the two paths can be increased by separating these paths from a branch node *deeper* within the clock tree (closer to the leaf registers).

III. Clock tree layout design

In this section, the proposed methodology is applied to the clock tree layout design process. The primary focus is on reducing the uncertainty in the delay of the clock signal arriving at the most critical data paths within a circuit. A strategy that reduces the delay uncertainty by increasing the size of the buffers along the most critical clock paths is described in section III-A. An alternative approach that increases the common portion of the clock tree among the paths that drive the critical registers is presented in section III-B.

A. Buffer insertion and sizing

To investigate the effect of increasing buffer size on the delay uncertainty of a clock signal, a buffer insertion and sizing tool has been developed. Buffers are inserted along a clock tree. The location of these buffers depends upon the combined load of the clocked nodes and the wire capacitance. The size of the inserted buffers is determined by the delay uncertainty constraints of the clock signal along the clock paths driven by each buffer.

The input to the buffer insertion tool is a minimal rectilinear Steiner tree that represents the layout of a clock tree. An

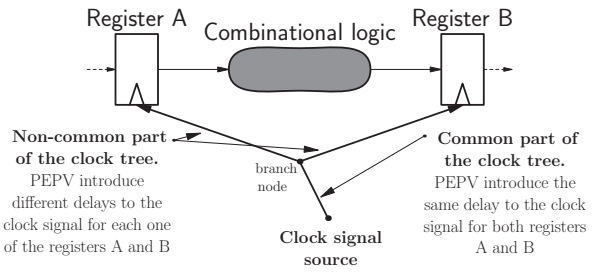

Fig. 3. Introduction of different clock signal delays to the non-common portions of the clock tree.

*Spectre® is a registered trademark of Cadence Design Systems Incorporated.

example of such a tree is shown in Figure 4. The source of the clock signal is located at the center of the tree plane. The numbered nodes shown in Figure 4 represent the location of the clock registers within the circuit.

The first step of this tool is to insert buffers within the clock tree. Clock buffers are inserted in a bottom-up fashion, starting from the tree leaves (*i.e.* the clocked elements) at the lowest level and advancing towards the root of the tree. When an intermediate node in the tree is reached, the total load from that node to the bottom of the tree is the summation of the capacitive load of the interconnect lines and the clocked elements. A clock buffer is inserted at a node when the downstream capacitive load of that node exceeds a threshold value. The magnitude of the downstream load determines the size of the inserted buffer.

The position of the inserted buffers within the clock tree shown in Figure 4 are represented by the dots labeled A, B, C, D, E, and F. Each buffer is the root to a *subtree* within the clock tree. A subtree is a part of the clock tree, having root at a buffer and terminated either at a clocked element or another clock buffer. Six subtrees are identified in the clock tree shown in Figure 4. Each subtree has its root at one of the buffers, A, B, C, D, E, and F.

The second step of the buffer insertion tool determines the clock signal delay uncertainty between sequentially-adjacent registers of the critical data paths. The delay uncertainty between the arrival time of the clock signals at those registers is dependent with the non-common portions of the clock tree. The uncertainty in the signal delay is determined for each of the subtrees along the signal path. In each subtree, the following three components of delay uncertainty are considered:

i) *Interconnect delay uncertainty due to crosstalk*. It is proportional to the wire length of the clock path and inversely proportional to the size of the buffer driving the subtree.

ii) *Buffer delay uncertainty due to crosstalk*, that increases with line-to-line crosstalk. Therefore it is proportional to the total wire length of the subtree driven by a buffer. It is inversely proportional to the size of the buffer driving the subtree.

iii) *Buffer delay uncertainty due to device parameter variations* is inversely proportional to the size of the buffer.

The total delay uncertainty of a signal propagating along a clock path is composed of the aforementioned terms, given the wire length of a path, the wire length of the subtrees, and the size of the buffers driving those subtrees. If the resulting delay uncertainty is greater than the delay uncertainty constraints for a particular pair of clock registers, the size of the buffers located along the non-common clock paths are increased to reduce the delay uncertainty. This process is applied iteratively until the delay uncertainty constraints are satisfied.

In the example shown in Figure 4, the critical data paths are those paths between the nodes $2 \rightarrow 19$ and $2 \rightarrow 7$. To satisfy the delay uncertainty constraints for the data path $2 \rightarrow 19$, the size of the buffers, A, B, D, and E, along the non-common clock paths from the source of the clock signal to registers 2 and 19 are increased. Similarly, to satisfy the delay uncertainty constraints for the data path $2 \rightarrow 7$, the size of the buffers A, B, D, and F are also increased. The relative size of each dot in Figure 4 represents the relative size of the corresponding buffer.

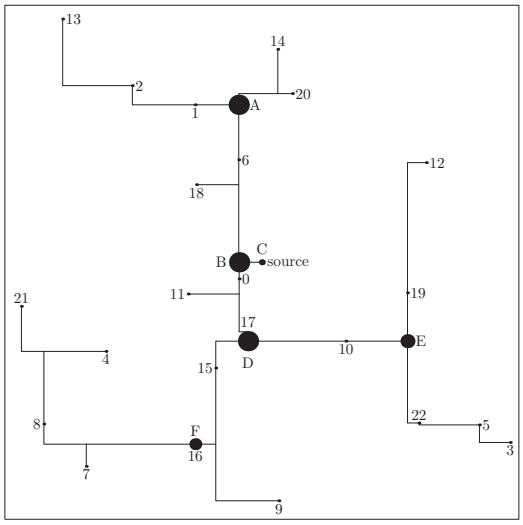

Fig. 4. Example of a minimal rectilinear Steiner clock tree. The labeled dots correspond to the positions of the inserted buffers within the tree. The dot size specifies the relative buffer size.

B. Dedicated minimal clock tree driving the registers of the critical paths

An alternative approach for reducing delay uncertainty among the clock paths that drive the most critical registers focuses on increasing the common portion of these paths. This approach utilizes a dedicated minimal clock tree to distribute the clock signal to these critical registers. The delay uncertainty can be further reduced to satisfy the design constraints by increasing the size of the buffers that drive this dedicated clock tree. The dedicated tree is developed through the following steps. Initially, the registers of the critical data paths are identified. A minimal rectilinear Steiner tree is used to distribute the clock signal to *only* those registers. The root of this dedicated tree is located where the coordinates are equal to the arithmetic mean of the corresponding coordinates of the critical registers. To satisfy the delay uncertainty constraints among the registers, a buffer is inserted at the root of the dedicated tree. The size of this buffer is iteratively increased until all of the delay uncertainty constraints are satisfied. Once the delay uncertainty constraints at the critical data paths are satisfied, the clock signal is distributed to the remaining registers within the circuit and the root of the dedicated tree through a minimal wire length clock tree.

An example of a dedicated minimal clock tree driving the critical registers of a circuit is shown in Figure 5 for the circuit example illustrated in Figure 4. The dedicated minimal tree is driven by buffer E. Note that the aggregate size of the clock buffers shown in Figure 5 is smaller than the aggregate size of

TABLE I
TRADEOFF BETWEEN THE INCREASE IN CLOCK TREE AREA AND THE REDUCTION IN POWER DISSIPATION

Circuit	Number of Registers	Aggregate buffer size			Clock tree area (μm)			Power dissipation (μW)		
		Buffer Sizing	Dedicated Tree	Reduction (%)	Buffer Sizing	Dedicated Tree	Increase (%)	Buffer Sizing	Dedicated Tree	Reduction (%)
1	11	21	10	52	3065	3930	28	499	438	2
2	12	18	5	72	2348	2706	15	425	356	16
3	17	29	7	75	3382	4167	23	638	531	16
4	23	34	8	76	3823	5005	31	763	656	14
5	28	30	9	70	4490	5403	20	825	737	10
6	36	25	10	60	4901	5911	20	882	851	3
7	42	15	9	40	4901	5167	5	923	831	10

the buffers in the circuit shown in Figure 4. The total area of the clock tree, however, is increased when a dedicated minimal clock tree for the critical nodes is used.

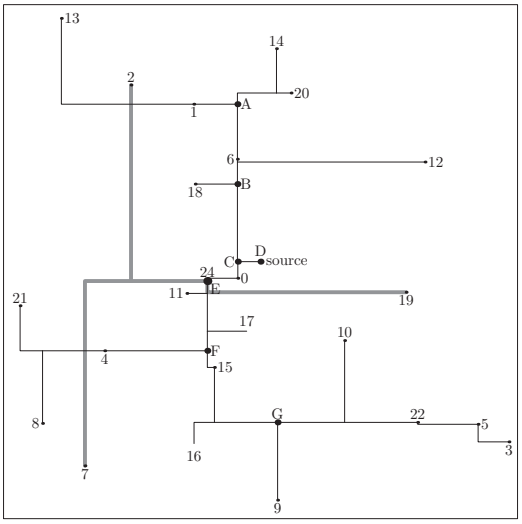

Fig. 5. Dedicated clock tree and buffers to drive the critical registers in the circuit shown in Figure 4

IV. POWER AND AREA TRADEOFFS

Two different design strategies have been proposed for reducing the delay uncertainty among the clock signals that drive the registers of the most critical data paths. The primary design cost for both of these strategies is an increase in the capacitive load of the clock distribution network. This larger load is the result of increasing either the size of the clock buffers or the total wire length of the clock tree. Both of these strategies therefore increase the power dissipated by a clock tree. This effect is demonstrated by the application of the proposed strategies on a set of benchmark circuits. The resulting aggregate buffer size, clock tree wire length and power dissipation are listed in Table I.

Note in Table I that the application of the dedicated clock tree strategy results in a lower power dissipation as compared with the buffer insertion approach, although the wire length of the corresponding clock tree is longer. The reduction in power dissipation is due to the reduced aggregate buffer size in the dedicated clock tree approach, when compared with the greater aggregate buffer size necessary for the buffer sizing approach.

V. CONCLUSIONS

A physical design methodology that satisfies the timing constraints of the most critical data paths in a circuit is presented in this paper. Two different layout design approaches are developed to reduce the uncertainty of the clock signal. One technique increases the size of the clock buffers inserted within a clock distribution network to reduce the delay uncertainty of the clock signal. The second technique exploits the common portion among the clock paths that drive the registers of the critical data paths. Simulation results from the application of these techniques to a set of benchmark circuits demonstrate useful tradeoffs among the aggregate size of the clock buffers, the total wire length of the clock tree, and the dissipated power.

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