A HIGH PRECISION CMOS CURRENT MIRROR / DIVIDER

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***Abstract*– A current mirror topology is proposed that provides very high precision, design insensitive up and down mirrored current, operation over a wide power supply range, straightforward design, and the possibility of conveniently obtaining a wide range of current divisions. This topology is appropriate for those applications in which precise current handling is necessary such as high accuracy A/D and D/A converters and reference cells.**

I. INTRODUCTION

Current mirrors are common circuits in analog and mixed-signal integrated circuits. Recently, current mode signal processing has attracted a great deal of interest due to the many advantages that current mode circuits offer, such as wide bandwidth. Many fundamental current mirror configurations have been developed in bipolar, MOS, and BiCMOS technologies [1, 2]. Improvements are numerous, *e.g.*, [3–8], each enhancement solving a problem specific to a certain application.

The proposed topology is useful in those high precision applications in which area and power dissipation are not of primary concern. The dissipated power can, however, be drastically reduced in converters if, after the conversion, a digital correction is applied [9, 10]. A reduction in area can also be achieved using this digital correction technique. Compared to other topologies, the proposed circuit topology offers several notable advantages. These advantages include ease of design, close to ideal up and down mirroring, insensitivity to the power supply variations of the up and down mirrored currents, and good operational insensitivity to process parameter variations, thereby requiring no trimming or self calibration.

A detailed discussion of the operation of this circuit topology is presented in Section II, followed by specific electrical and physical design considerations in Section III. Simulation results are described in Section IV. The performance of the current mirror is compared with a different high precision current mirror topology in Section V. Some conclusions are presented in Section VI.

II. BASIC ELEMENTS

A few terms should first be introduced. A simple example of an up and down current mirror is shown in Figure 1. In CMOS technology, the dependency of the output current (I_{out}) on V_{DS} strongly affects both current mirror configurations. Also, since the up/down mirror depends upon the P and N transistors respectively, due to the different characteristics of these two types of transistors, different performance characteristics for the two types of mirrors are achieved in practice. The proposed configuration effectively eliminates both problems, matching the performance of the two current mirror topologies. Since the same mirroring error is obtained for both the up and down current mirrors, the proposed circuit offers an ability to shift between the up and down current sources, herein called a *ping-pong facility*.

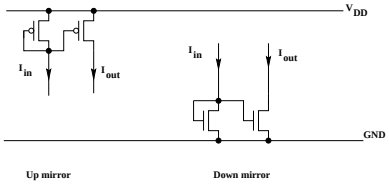

Fig. 1. Up and down current mirrors.

The topology of the proposed current mirror/divider, including the up mirror, down mirror, and divider, is shown in Figure 2.

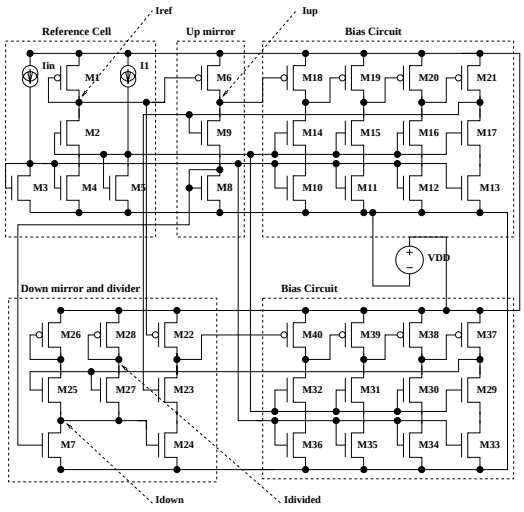

Fig. 2. Transistor-level schematic of CMOS current mirror/divider circuit

Several distinct functional blocks or cells can be distinguished. These blocks include the reference cell that provides the reference voltages and currents for the entire circuit, the up mirror cell that mirrors the current up, the down mirror and divider cell that mirrors the current down and properly divides the current according to the application, and the bias circuit cell, a fundamental block in this topology, which provides the close to ideal current mirroring. As shown, an identical bias circuit is used for the up mirror as well as for the down mirror. Since the bias circuit dictates the performance of the current mirror,

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matched performance for the up and down mirror is expected, eliminating the performance dependency on the transistor parameters.

M1, M2, M3, M4, and M5 constitute the reference cell. M3 and M5 provide the two reference voltages, V_{M3} and V_{M5}. I_{DSM1} is the initial reference current that is mirrored and divided. Designing this cell so that appropriate values for these voltages and currents are obtained constitutes the primary design challenge of this current mirror/divider circuit. As shown in Figure 2, M1 and M8 are the reference transistors, and M6 and M7 are the mirror transistors for the up mirror and down mirror, respectively. In order to obtain the same mirrored current, the mirror transistors must ideally have the same V_{GS}, V_{DS}, and W/L as the reference transistors, permitting both devices to satisfy the same basic I-V equation,

$$I_{DS} = K\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}), \qquad (1)$$

with $V_{GS} = V_{DS}$. In Figure 2, $V_{DSM1} = V_{GSM1} = V_{GSM6}$ and $V_{DSM8} = V_{GSM8} = V_{GSM7}$. In order to satisfy the above equation for the reference and mirror transistors, the conditions $V_{DSM6} = V_{GSM1}$ and $V_{DSM7} = V_{GSM8}$ must hold. These conditions are obtained for the up mirror as well as for the down mirror using the same technique, however, certain particularities exist in each case. For both mirrors, the $V_{GS} = V_{DS}$ condition for the mirror transistors is generated by a floating drain feedback configuration loop, provided by the bias circuit. The operation of the up mirror circuit is discussed in detail in this paper. Only the differences between the down mirror and the up mirror are described for the down mirror.

The feedback loop is between the gate of M9 and the drain of M9 through the bias circuit. For this circuit, the input corresponds to the gate of M9, and the output corresponds to the drain of M9. When the circuit operates in open loop, the drain of M9 is floating. When the circuit operates in closed loop, all of the transistors are properly biased and the required V_{DSM6} is obtained. In discussing the bias circuit, an important issue is the manner in which the loop is closed. Assume initially that $V_{GSM9} \Rightarrow 0$ ($V_{GSM9} < V_T$) such that the current through M6, M9, and M8 is zero. M10–M13 and M14–M17 are biased with V_{M3} and V_{M5}, respectively. The above bias situation forces $V_{DSM13} = V_{DSM17} = 0$ ($I_{DS} = 0$). Since $V_{DSM21} = V_{DD}$, V_{GSM21} must be smaller than the threshold voltage V_T. The bias on M12-M16-M20 forces a contradiction, since due to the M12-M16 bias, a large current must flow through M20, which is not possible with $V_{DSM20} \Rightarrow 0$ (M20 is in the linear region). However, it is possible for M20 to sink the required current if $V_{GSM20} \Rightarrow V_{DD}$. Applying the same approach, $V_{GSM19} \Rightarrow 0$ and $V_{GSM18} \Rightarrow V_{DD}$ are obtained, which forces $V_{DSM6} \Rightarrow V_{DD}$, biasing M6 to supply a large current. However, initially $I_{DSM6} \Rightarrow 0$ is considered. Note that a large I_{DSM6} is required to close the loop, creating a contradiction in the operation of the circuit. A complementary situation, starting with $V_{DSM9} \Rightarrow V_{DD}$, also creates a similar contradiction within the loop. The only possibility to remove this contradiction is for V_{GSM9}, the input to the bias circuit, to have a specific value between ground and V_{DD} such that the loop is properly closed and all the transistors are appropriately biased.

V_{out} reaches the required value, V_{GSM1}, due to the similarities in the biasing of the M1-M2-M4 and M10-M14-M18 type circuits and the feedback loop. By evaluating Figure 2 and considering the previous discussion of the loop, it can also be noted that once the equilibrium state is reached ($V_{DSM6} = V_{GSM1}$), an increase in I_{DSM6} increases V_{GSM9}, which decreases V_{DSM21}, increases V_{GSM21}, decreases V_{GSM20}, increases V_{GSM19}, decreases V_{GSM18}, which finally decreases I_{DSM6}, returning to the state of equilibrium. An initial decrease in I_{DSM6} will result in an increase in I_{DSM6}, again returning to the state of equilibrium. As described, an oscillation is expected around the equilibrium point, $V_{DSM6} = V_{GSM1}$.

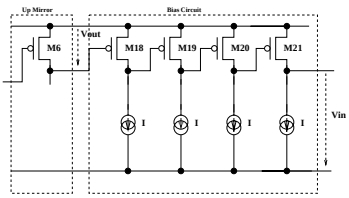

Fig. 3. Equivalent schematic of the bias circuit

A simplified equivalent schematic of the bias circuit is presented in Figure 3. Each current source depicted in Figure 3 consists, noting Figure 2, of M10-M14 ... M13-M17, respectively, M10 ...M13 being biased by V_{M3} and M14 ...M17 by V_{M5}. Each current source is implemented as shown in Figure 2 by a cascode current mirror. A small signal analysis of the bias circuit allows the derivation of the output voltage and output impedance of the current source,

$$V_{out} = V_{gs18} \qquad (2)$$

where

$$V_{out} = \frac{-Vin}{gm_{18}ro_{18}gm_{19}ro_{19}gm_{20}ro_{20}gm_{21}ro_{21}} \qquad (3)$$

and

$$R_o = ro_6gm_{18}ro_{18}gm_{19}ro_{19}gm_{20}ro_{20}gm_{21}ro_{21}. \qquad (4)$$

The bias circuit requires the following three groups of transistors to be identical: M4 and M10-M13, M2 and M14-M17, and M1, M6, and M18-M21. The above analysis and (2) – (4) demonstrate that V_{GSM18} converges to V_{GSM1}, forcing $V_{DSM6} \Rightarrow V_{GSM1}$. As shown by (3), the effect of V_{in} on the output is diminished by the magnitude of the transconductance and output resistance of each transistor along the feedback path (see Figure 3). Thus $V_{out} \Rightarrow 0$, which is equivalent to $R_o \Rightarrow$ infinity, as shown by (3) and (4). These formulae confirm the aforementioned qualitative analysis of the feedback loop.

A minimal oscillation is expected around the equilibrium point due to the influence of V_{in} through the feedback loop. Another influence to be noted, albeit minimal, is due to the nonidealities of the current sources *I*. To reduce the oscillation, a larger W/L ratio for the bias circuit transistors is necessary. Also, the bias circuit may require frequency compensation.

For the down mirror, a similar loop exists through an identically dedicated bias circuit. Here, M22 (see Figure 2) is similar to the mirror transistor M6 of the up mirror, giving $I_{DSM22} = I_{DSM1}$. This current biases the M22-M23-M24 column such that $V_{GSM24} = V_{DSM7} = V_{GSM8}$, making $I_{DSM7} = I_{DSM1} = I_{DSM6}$.

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The down mirror can be terminated with a current divider (division by two in Figure 2). Using two identical paths, namely M25 to M26 and M27 to M28, an accurate division is obtained. The resulting half current, I_{DSM28}, can be repeatedly divided using the same methodology. As described by (1), in order to use the same bias circuit for the following mirroring and divisions, M26 and M28 must be sized by W/2. By subsequently dividing the current, a series of reference currents is obtained, appropriate for high precision A/D and D/A converters.

III. Design Considerations

The design process consists of properly designing the reference cell according to the specific requirements of the application, and in satisfying simple rules in sizing the transistors within the circuit. In the reference cell (see Figure 2), I_{DSM3} is the reference input current. Proper reference voltages V_{M3} and V_{M5} are assumed to be provided. Typically, $V_{M5} = 2V_{M3}$ or higher. M2 is a buffer transistor, and all the power supply variations affect V_{DSM2}. Considering a constant I_{DSM3}, the V_{DD} variations reflected on V_{DSM2} result in a variable I_{DSM1}, which is the initial reference current for the circuit. If a relative value for I_{DSM1} is appropriate for the application, then no modifications are necessary. If a constant I_{DSM1} is needed, however, a current source for I_{DSM3} must be designed that will consider variations in I_{DSM1} due to variations in V_{DSM2}. However, even in high precision converters, a constant I_{DSM3} can be used if the voltage to current converter of the input signal is designed such that the input current varies with V_{DD} over an equivalent V_{DSM2}.

In order to satisfy these design goals, $M1 = M6 = M18 = M19 = M20 = M21 = M22$, $M2 = M14 = M15 = M16 = M17$, $M23 = M9$, and $M4 = M10 = M11 = M12 = M13 = M8 = M7 = M24$ must be satisfied. In the initial cell, large sizes are recommended in order to permit high precision and tolerance to process parameter variations. For the circuit to function properly, all transistors must operate in saturation all the time.

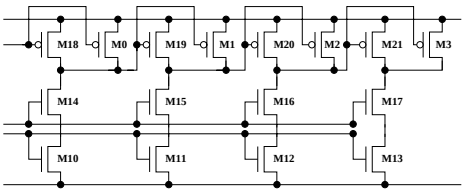

Fig. 4. The bias circuit used after a division

After a division, the reference current for the second current mirror divider is $I_{DS}/2$. M28 replaces M1 as the reference transistor, and the transistor sizes of this cell are referenced accordingly. As mentioned previously, the larger the transistor sizes in the bias circuit, the higher the precision obtained. The proper relative sizing depends on the specific performance requirements of the application.

Due to short-channel effects such as velocity saturation and mobility degradation as well as short-width effects, (1) does not hold for high precision applications. In order to provide the highest precision after a division, the circuit shown in Figure 4 is used for the bias circuits of the following cell. Instead of the M18-M21 group of transistors of size W, each transistor is replaced by a group of two transistors in parallel, each sized W/2, with each group of two transistors sinking the same current as the initial single transistor while providing the correct bias.

Every up mirror, down mirror, or division requires a bias circuit which uses large transistor sizes. This requirement means large area and dissipated power, since the bias circuits operate with a high initial reference current (I_{DSM1}), no matter what current is mirrored or divided. A bias circuit operating at small currents with small transistors will require a constant correction factor applied to the mirrored current, the advantage being smaller area and power, the disadvantage being the aforementioned problems and imperfections. In the case of a converter, these corrections can be implemented by a digital post processing of the converted sample, saving power and area. However, special care must be given to the aforementioned oscillation, which increases with smaller size transistors.

IV. Simulation Results

Circuit simulations based on Cadence-Spectre and a 1.2 μm CMOS technology are described in this section. In order to observe the aforementioned oscillation, minimum size transistors are used. M5 is 1.8 μm/1.2 μm and the remaining transistor ratios, except for M26 and M28, are 19.2 μm/1.2 μm. M26 and M28 are 9.6 μm/1.2 μm. $I_1 = 200$ μA and I_{DSM1} for $V_{DD} = 10$ V is 512 μA, a 2^n value in view of the subsequent divisions by 2.

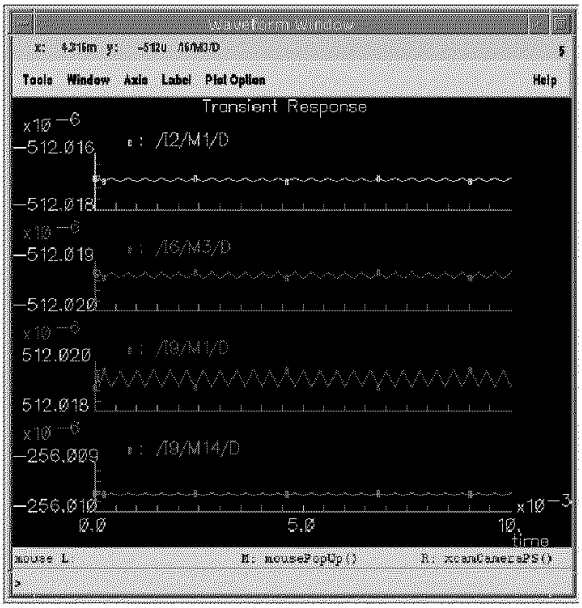

Fig. 5. Transient waveforms for the reference, up, down, and divided currents, respectively.

The reference, up, down, and divided current values, respectively, are shown in Figure 5. The current values are, as shown, $I_{ref} = 512.017$ μA, $I_{up} = 512.019$ μA, $I_{down} = 512.019$ μA, and $I_{divided} = 256.009$ μA. Note the excellent precision of the mirroring and the oscillation, which in the worst case (for the down mirror) is 0.001 μA in magnitude. The bias circuit is compensated with capacitors at the drain of M6, gate of M9, drain of M8, and gate of M25, and practically no oscillation is observed. Decreasing the size of the transistors, however, requires the capacitors to have a value of up to 1.5 pF for a 9.6

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μm/1.2 μm transistor to remove any oscillation. A higher accuracy is obtained by increasing the size of the transistors. The same currents as shown in Figure 5 are observed when V_{DD} is swept from a minimum value for which all transistors are still saturated to an arbitrarily larger value. No circuit related upper limit exists, however, a technological limit exists, such as the breakdown voltage. The expected I_{DSM1} variation due to the V_{DSM2} variation assuming a constant I_{DSM3} is noted. The excellent equality and division among the currents over the entire sweep range is also noted. In the aforementioned order of currents, all in μA, values of 505, 505, 505, 252.5 for $V_{DD} = 5$ V to 525, 525, 525, 262.5 for $V_{DD} = 20$ V are observed.

Differences exist from using a standard bias circuit after a division as compared to using the recommended bias circuit shown in Figure 4. For the two circuits, differences in the up mirrored divided current as compared to the divided current of 256.01 μA are observed. The improvement is from 255.85 μA for the case where the standard bias circuit is used to the same current as the reference current of 256.01 μA for the case where the balanced bias circuit is used. The improvement in accuracy due to the use of the bias circuit from Figure 4 can be explained by observing the operating point of M6. According to (1), $I_{DS}/2$ is expected since a W/2L transistor ratio is used. Due to short channel and short width effects, the normal bias circuit produces a slightly different output voltage (V_{GSM18}). In the two cases analyzed under the same bias and sizing conditions, M6 has a bias of $V_{GS} = V_{GSref} = 2.532$ V, $V_{DS} = 2.522$ V, and $I_{DS} = 255.85$ μA for the standard bias circuit. While using the balanced bias circuit shown in Figure 4, the equilibrium is reestablished and M6 has a bias of $V_{GS} = V_{GSref} = 2.532$ V, $V_{DS} = 2.532$ V, and $I_{DS} = 256.01$ μA.

V. Performance Comparison

A comparison with previous work may be useful, though difficult, due to the individuality of the current mirror topology. However, a comparison with a high precision current mirror, reported in [5], is described here. In [5], comparison with previous related work was also made. The work described in [5] was shown to have notable advantages.

TABLE I
UP MIRROR PERFORMANCE COMPARISON WITH IAFCCM [5]

Issue	Up Mirror	IAFCCM [5]
Mirroring error	<0.00022%	<0.02%
Supply voltage dependency	0	<0.015%
Mirroring accuracy dependency on I_{in}	NO	YES
Largest transistor width	19.2 μm	300 μm
Number of transist.	15	9
Total width of all transistors	288 μm L=1.2 μm	1650 μm L=3,9 μm
Dissipated power (500 μA)	$\approx$ 30mW	< 20mW
R_o (qualitative)	$\propto (g_m r_o)^4$	$\propto (g_m r_o)^2$

The ping-pong facility of the topology proposed in this paper should also be noted, in which the up and down current can be repeatedly mirrored with almost no error. This capability permits the development of a series of reference currents useful in high speed converters. In Table I, the up mirror of the present topology is compared to the circuit described in [5], IAFCCM. Note the difference in the sizes of the transistors between the two circuits, which is disadvantageous for the topology introduced here. Larger sizes, as mentioned, would further improve the performance of the proposed circuit. Note in Table I the minimum two orders of magnitude higher accuracy and no measurable mirroring supply voltage dependency and mirroring accuracy dependency on I_{in}.

VI. Conclusions

The CMOS current mirror/divider circuit topology presented in this paper provides improved performance and offers an added capability for switching the up and down current (the ping-pong facility), applicable to certain high precision analog and mixed signal circuits. The current mirror circuit offers a high design precision in up and down mirroring and in division, and no measurable supply voltage dependency and mirroring accuracy dependency on the input current, I_{in}. However, to obtain the predicted accuracy, transistor matching is required. As mentioned, the larger the transistor sizes, the better the matching, minimizing the sensitivity to process variations and increasing the circuit accuracy. Another advantage of the proposed circuit is that the transistor matching can be made in standard, well defined sizes. The cost of this circuit is an increase in power dissipation, and possibly, an increase in area. Another possible advantage is the capability of obtaining a series of four reference currents, each half of the previous current, by reducing the size of all the transistors (see Figure 2) from W to only W/2. This capability eliminates, even in high precision converters, any aspect ratio problems. In summary, this current mirror topology provides an important enhancement in performance and capability for application to higher precision, lower cost converters.

References

[1] A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*. John Wiley & Sons, Inc., 1984.

[2] C. Toumazou, F. Lidgey, and D. Haigh, eds., *Analogue IC Design, the Current-Mode Approach*. Peter Peregrinus Ltd., London, 1990.

[3] T. Itakura and Z. Czarnul, "High Output Resistance CMOS Current Mirrors for Low-Voltage Applications," *IEICE Transactions on Fundamentals of Electronics, Communications And Computer Sciences*, Vol. E80-A, No. 1, pp. 230–232, January 1997.

[4] H. Wasaki and Y. Horio, "Current Multiplier / Divider Circuit," *Electronics Letters*, Vol. 27, No. 6, pp. 504–506, March 1991.

[5] A. Zeki and H. Kuntman, "Accurate and High Output Impedance Current Mirror Suitable for CMOS Current Output Stages," *Electronics Letters*, Vol. 33, No. 12, pp. 1042–1043, June 1997.

[6] J. Mulder and A. C. V. der Woerd, "High Swing Cascode MOS Current Mirror," *Electronics Letters*, Vol. 32, No. 14, pp. 1251–1252, July 1996.

[7] M. Akiya and S. Nakashima, "High Precision MOS Current Mirror," *IEE Proceedings I*, Vol. 131, No. 5, pp. 170–175, October 1984.

[8] T. Serrano and B. Linares-Barranco, "The Active-Input Regulated-Cascode Current Mirror," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. CAS I-41, No. 6, pp. 464–467, June 1994.

[9] H. Lee, D. Hodges, and P. Gray, "A Self-Calibrating 15b CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, Vol. SC-19, No. 6, pp. 813–819, December 1984.

[10] Y. Lin, B. Kim, and P. Gray, "A 13 bit, 2.5 Mhz Self-Calibrated Pipelined A/D Converter in 3-um CMOS," *Proceedings of the IEEE Symposium on VLSI Circuits*, pp. 33–34, June 1990.